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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c71-20-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C71X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C710	512 x 14	0000h-01FFh
PIC16C71	1K x 14	0000h-03FFh
PIC16C711	1K x 14	0000h-03FFh
PIC16C715	2K x 14	0000h-07FFh

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C710 PROGRAM MEMORY MAP AND STACK



FIGURE 4-2: PIC16C71/711 PROGRAM MEMORY MAP AND STACK



FIGURE 4-3: PIC16C715 PROGRAM MEMORY MAP AND STACK



4.2.2.6 PCON REGISTER

Applicable Devices71071711715

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external MCLR Reset or WDT Reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset (BOR) condition from a Power-on Reset condition. For the PIC16C715 the PCON register also contains status bits MPEEN and PER. MPEEN reflects the value of the MPEEN bit in the configuration word. PER indicates a parity error reset has occurred. Note: BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if BOR is clear, indicating a brown-out has occurred. The BOR status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 4-12: PCON REGISTER (ADDRESS 8Eh), PIC16C710/711



FIGURE 4-13: PCON REGISTER (ADDRESS 8Eh), PIC16C715

R-U	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-q		
MPEEN		—	—	—	PER	POR	BOR ⁽¹⁾	R = Readable bit	
bit7	bit0 W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset								
bit 7:	bit 7: MPEEN: Memory Parity Error Circuitry Status bit Reflects the value of configuration word bit, MPEEN								
bit 6-3:	3: Unimplemented: Read as '0'								
bit 2:	 PER: Memory Parity Error Reset Status bit 1 = No Error occurred 0 = Program Memory Fetch Parity Error occurred (must be set in software after a Parity Error Reset) 								
bit 1:	 it 1: POR: Power-on Reset Status bit 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) 								
bit 0:	BOR: Brown-out Reset Status bit 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)								



FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

FIGURE 6-4: TIMER0 INTERRUPT TIMING



7.9 <u>Transfer Function</u>

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is Analog VREF/256 (Figure 7-6).

7.10 <u>References</u>

A very good reference for understanding A/D converters is the "Analog-Digital Conversion Handbook" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).



ADON = 0Yes ADON = 0 No Acquire Selected Channel Yes GO = 0? No Start of A/D onversion Delaye Instruction Cycle Yes A/D Clock = RC? /es SLEEP Finish Conversior Inst uction GO = 0 ADIF = 1 No No Yes Abort Conversion Yes Wake-up From Sleep inish Conversio Device in SLEEP? Wait 2 TAD GO = 0ADIF = 0 GO = 0 ADIF = 1 No No SLEEP Power-down A/D Finish Conversion Stay in Sleep Power-down A/D Wait 2 TAD GO = 0 ADIF = 1 Wait 2 TAD

FIGURE 7-7: FLOWCHART OF A/D OPERATION

8.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 8.8 for details on SLEEP mode.

8.5.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 6.0)

8.5.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 5.2)

For the PIC16C71 Note: if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
OSC1 /					
CLKOUT ③	(4)			/	
INT pin		1	1 1 1 1		1 1 1 1 1 1 1 1
INTF flag (INTCON<1>)			Interrupt Latency (2)		
GIE bit (INTCON<7>)					
INSTRUCTION	FLOW		, , , , , , , , , , , , , , , , , , , ,		· · · · · · · · · · · · · · · · · · ·
PC	PC	PC+1	PC+1	X 0004h	X 0005h
Instruction (fetched	Inst (PC)	Inst (PC+1)	_	Inst (0004h)	Inst (0005h)
Instruction {	Inst (PC-1)	Inst (PC)	Dummy Cycle	Dummy Cycle	Inst (0004h)

FIGURE 8-19: INT PIN INTERRUPT TIMING

Note 1: INTF flag is sampled here (every Q1).

2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in RC oscillator mode. 4: For minimum width of INT pulse, refer to AC specs.

5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

8.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (STATUS<3>) is cleared, the \overline{TO} (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level (VIHMC).

8.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. External reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External $\overline{\text{MCLR}}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{\text{TO}}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. A/D conversion (when A/D clock source is RC).

Other peripherals cannot generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the subset (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

8.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

9.1 Instruction Descriptions

ADDLW	Add Literal and W					
Syntax:	[<i>label</i>] Al	DDLW	k			
Operands:	$0 \le k \le 25$	55				
Operation:	(W) + k –	→ (W)				
Status Affected:	C, DC, Z					
Encoding:	11	111x	kkkk	kkkk		
Description:	The conter added to the result is pla	nts of the he eight b aced in th	W register it literal 'k' e W regist	are and the er.		
Words:	1					
Cycles:	1					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
	Decode	Read literal 'k'	Process data	Write to W		
Example:	ADDLW	0x15				
	Before In	Before Instruction				
	After Inst	W =	0x10			
		W =	0x25			
		a al f				
			£ -1			
Syntax:			f,d			
Operands:	$0 \le f \le 12$ $d \in [0,1]$.7				
Operation:	(W) + (f)	ightarrow (dest)				
Status Affected:	C, DC, Z					
Encoding:	00	0111	dfff	ffff		
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register If 'd' is 1 the					

Encoding:	00	0111	dfff	ffff			
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write to Dest			
Example	ADDWF	FSR,	0				
	Before Instruction						
		W =	0x17				
		FSR =	0xC2				
	After Inst	ruction					
		VV =	UXD9				
		⊦SR =	0xC2				

ANDLW	AND Literal with W					
Syntax:	[<i>label</i>] A	[<i>label</i>] ANDLW k				
Operands:	$0 \le k \le 255$					
Operation:	(W) .AND	D. (k) \rightarrow (W)			
Status Affected:	Z					
Encoding:	11 1001 kkkk kkkk					
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.					
Words:	1					
Cycles:	1					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
	Decode	Read literal "k"	Process data	Write to W		
Example	ANDLW	0x5F				
	Before In	struction	0.10			
	After Inst	vv = ruction W =	0x03			

ANDWF	AND W with f				
Syntax:	[<i>label</i>] A	NDWF	f,d		
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1 \right] \end{array}$				
Operation:	(W) .AND. (f) \rightarrow (dest)				
Status Affected:	Z				
Encoding:	00	0101	dfff	ffff	
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
	Decode	Read register 'f'	Process data	Write to Dest	
Example	ANDWF	FSR,	1		
	Before In	struction	1		
		W =	0x17		
	After Inst	ruction	0.02		
		W =	0x17		
		FSR =	0x02		

GOTO	Unconditional Branch					
Syntax:	[label]	GOTO	k			
Operands:	$0 \le k \le 20$	047				
Operation:	$k \rightarrow PC<10:0>$ PCLATH<4:3> \rightarrow PC<12:11>					
Status Affected:	None					
Encoding:	10	1kkk	kkkk	kkkk		
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.					
Words:	1					
Cycles:	2					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
1st Cycle	Decode	Read literal 'k'	Process data	Write to PC		
2nd Cycle	NOP	NOP	NOP	NOP		
Example	GOTO TI After Inst	HERE ruction PC =	Address	THERE		

INCF	Increment f					
Syntax:	[label]	INCF f	,d			
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$					
Operation:	(f) + 1 \rightarrow	(dest)				
Status Affected:	Z					
Encoding:	00	1010	dfff	ffff		
Description:	The conter mented. If in the W re placed bac	nts of reg 'd' is 0 the egister. If ' ck in regis	ister 'f' are e result is d' is 1 the ster 'f'.	incre- placed result is		
Words:	1					
Cycles:	1					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
	Decode	Read register 'f'	Process data	Write to dest		
Example	INCF	CNT,	1			
	Before In	struction CNT Z	= 0xFl = 0	=		
	After Inst	ruction				
		CNT 7	= 0x00)		

10.0 DEVELOPMENT SUPPORT

10.1 <u>Development Tools</u>

The PICmicro[™] microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE[®] II Universal Programmer
- PICSTART[®] Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB[™] SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH[®]–MP)

10.2 <u>PICMASTER: High Performance</u> <u>Universal In-Circuit Emulator with</u> <u>MPLAB IDE</u>

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB[™] Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows[®] 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

10.3 ICEPIC: Low-Cost PIC16CXXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT[®] through Pentium[™] based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In standalone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

10.5 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, lowcost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket. MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/ output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.12 <u>C Compiler (MPLAB-C)</u>

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of micro-controllers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

10.13 <u>Fuzzy Logic Development System</u> (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB[™] demonstration board for hands-on experience with fuzzy logic systems implementation.

10.14 <u>MP-DriveWay™ – Application Code</u> <u>Generator</u>

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

10.15 <u>SEEVAL[®] Evaluation and</u> <u>Programming System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in tradeoff analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

10.16 <u>KEELOQ[®] Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

Appli	cable Devices	710 71	711 715
11.1	DC Character	ristics:	PIC16C710-04 (Commercial, Industrial, Extended) PIC16C711-04 (Commercial, Industrial, Extended) PIC16C710-10 (Commercial, Industrial, Extended) PIC16C711-10 (Commercial, Industrial, Extended) PIC16C710-20 (Commercial, Industrial, Extended)
			PIC16C711-20 (Commercial, Industrial, Extended)

DC CHA	DC CHARACTERISTICS				p erati mpera	n g Con ture (-	ditions (unless otherwise stated) $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ (commercial) $\cdot40^{\circ}C$ $\leq TA \leq +85^{\circ}C$ (industrial) $\cdot40^{\circ}C$ $\leq TA \leq +125^{\circ}C$ (extended)
Param. No.	Characteristic	Sym	Min	Тур†	Мах	Units	Conditions
D001 D001A	Supply Voltage	Vdd	4.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power- on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN configuration bit is enabled
			3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2)	IDD	-	2.7	5	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V
D020	Power-down Current	IPD	-	10.5	42	μA	$VDD = 4.0V$, WDT enabled, $-40^{\circ}C$ to $+85^{\circ}C$
D021	(Note 3)		-	1.5	21	μΑ	VDD = $4.0V$, WDT disabled, $-0^{\circ}C$ to $+70^{\circ}C$
D021A D021B			-	1.5	30	μΑ μΑ	$VDD = 4.0V$, VDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$ $VDD = 4.0V$, WDT disabled, $-40^{\circ}C$ to $+125^{\circ}C$
D023	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDDMCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

Applicable Devices 710 71 711 715

11.5 <u>Timing Diagrams and Specifications</u>



FIGURE 11-2: EXTERNAL CLOCK TIMING

TABLE 11-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency	DC	_	4	MHz	XT osc mode
		(Note 1)	DC	_	4	MHz	HS osc mode (-04)
			DC	_	10	MHz	HS osc mode (-10)
			DC	_	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency	DC	—	4	MHz	RC osc mode
		(Note 1)	0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	-	-	ns	XT osc mode
		(Note 1)	250	—	-	ns	HS osc mode (-04)
			100	—	-	ns	HS osc mode (-10)
			50	—	-	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		Oscillator Period	250	-	-	ns	RC osc mode
		(Note 1)	250	-	10,000	ns	XT osc mode
			250	-	250	ns	HS osc mode (-04)
			100	_	250	ns	HS osc mode (-10)
			50	-	250	ns	HS osc mode (-20)
			5			μs	LP osc mode
2	TCY	Instruction Cycle Time (Note 1)	200		DC	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1) High	50	—	-	ns	XT oscillator
	TosH	or Low Time	2.5	—	-	μs	LP oscillator
			10	—		ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise	_	—	25	ns	XT oscillator
	TosF	or Fall Time	—	-	50	ns	LP oscillator
			_	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C710/711.

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FIGURE 12-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)



FIGURE 12-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)



TABLE 12-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2	
LP	32 kHz	33 pF	33 pF	
	200 kHz	15 pF	15 pF	
XT	200 kHz	47-68 pF	47-68 pF	
	1 MHz	15 pF	15 pF	
	4 MHz	15 pF	15 pF	
HS	4 MHz	15 pF	15 pF	
	8 MHz	15-33 pF	15-33 pF	
	20 MHz	15-33 pF	15-33 pF	
		•		
Crystals Used				
32 kHz	Epson C-00	01R32.768K-A	± 20 PPM	
200 kHz	STD XTL 2	± 20 PPM		
1 MHz	ECS ECS-	± 50 PPM		
4 MHz	ECS ECS-4	40-20-1	± 50 PPM	
8 MHz	EPSON CA	-301 8.000M-C	± 30 PPM	
20 MHz	EPSON CA	EPSON CA-301 20.000M-C		

FIGURE 12-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)







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FIGURE 12-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)



FIGURE 12-28: MAXIMUM IDD vs. FREQUENCY (XT MODE, -40°C TO 85°C)



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15.0 ELECTRICAL CHARACTERISTICS FOR PIC16C71

Absolute Maximum Ratings †

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	0 to +14V
Total power dissipation (Note 1)	
Maximum current out of Vss pin	150 mA
Maximum current into Vod pin	100 mA
Input clamp current, Iк (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA	50 mA
Maximum current sunk by PORTB	150 mA
Maximum current sourced by PORTB	100 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ	$\{(VDD-VOH) \times IOH\} + \sum (VOI \times IOL)$

Note 2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR} pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C71-04	PIC16C71-20	PIC16LC71-04	JW Devices
RC	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 μA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq:4 MHz max.
хт	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μA typ. at 4V Freq: 4 MHz max.	VDD: 3.0V to 6.0V IDD: 1.4 mA typ. at 3.0V IPD: 0.6 μA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 3.3 mA max. at 5.5V IPD: 14 μA max. at 4V Freq: 4 MHz max.
нѕ	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.0 μA typ. at 4.5V	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 μA typ. at 4.5V	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.0 μA typ. at 4.5V
LP	VDD: 4.0V to 6.0V IDD: 15 μA typ. at 32 kHz, 4.0V IPD: 0.6 μA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	VDD: 3.0V to 6.0V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V Freq: 200 kHz max.	VDD: 3.0V to 6.0V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C71

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE



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FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



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FIGURE 16-12: TYPICAL IDD vs. FREQ (EXT CLOCK, 25°C)



Data based on matrix samples. See first page of this section for details.

17.2 <u>18-Lead Plastic Dual In-line (300 mil) (P)</u>



Package Group: Plastic Dual In-Line (PLA)						
		Millimeters				
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	_	4.064		_	0.160	
A1	0.381	-		0.015	_	
A2	3.048	3.810		0.120	0.150	
В	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
С	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	_		0.035	_	
S1	0.127	-		0.005	_	





Package Group: Plastic SOIC (SO)						
		Millimeters				
Symbol	Min	Max	Notes	Min	Мах	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
В	0.355	0.483		0.014	0.019	
С	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
е	1.270	1.270	Reference	0.050	0.050	Reference
Н	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	18	18		18	18	
CP	_	0.102		_	0.004	

TO bit	
TOSE bit	
TRISA Register	
TRISB Register	
Two's Complement	7
U	

0	
Upward Compatibility	
UV Erasable Devices	

W

W Register	
ALU	7
Wake-up from SLEEP	
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WDTE bit	
Z	

Z bit .		
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