



Welcome to [E-XFL.COM](http://E-XFL.COM)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-04-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-04-ss</a>

# PIC16C71X

---

---

NOTES:

# PIC16C71X

## 3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

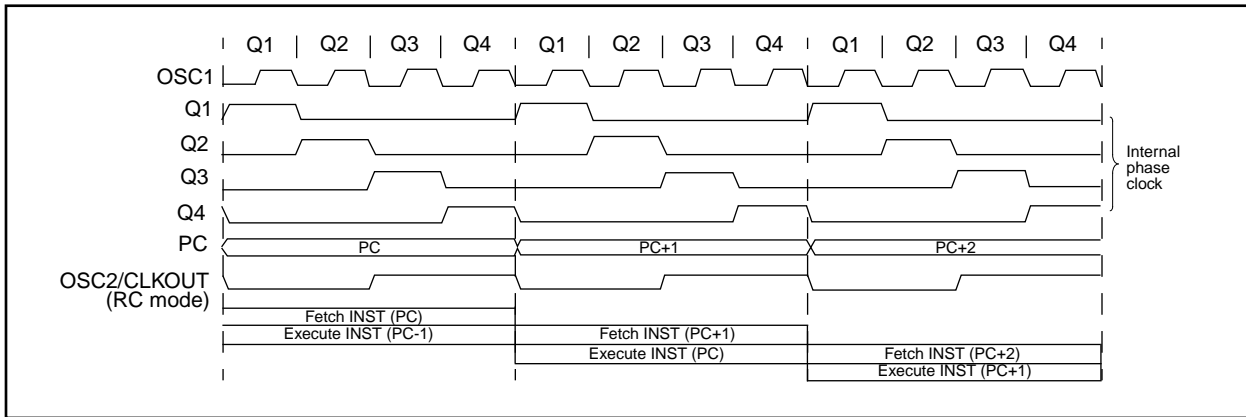
## 3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

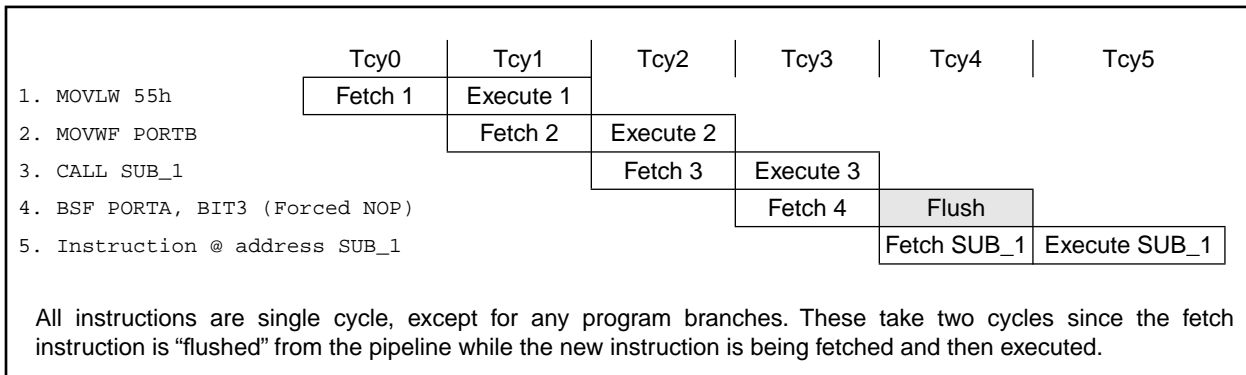
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

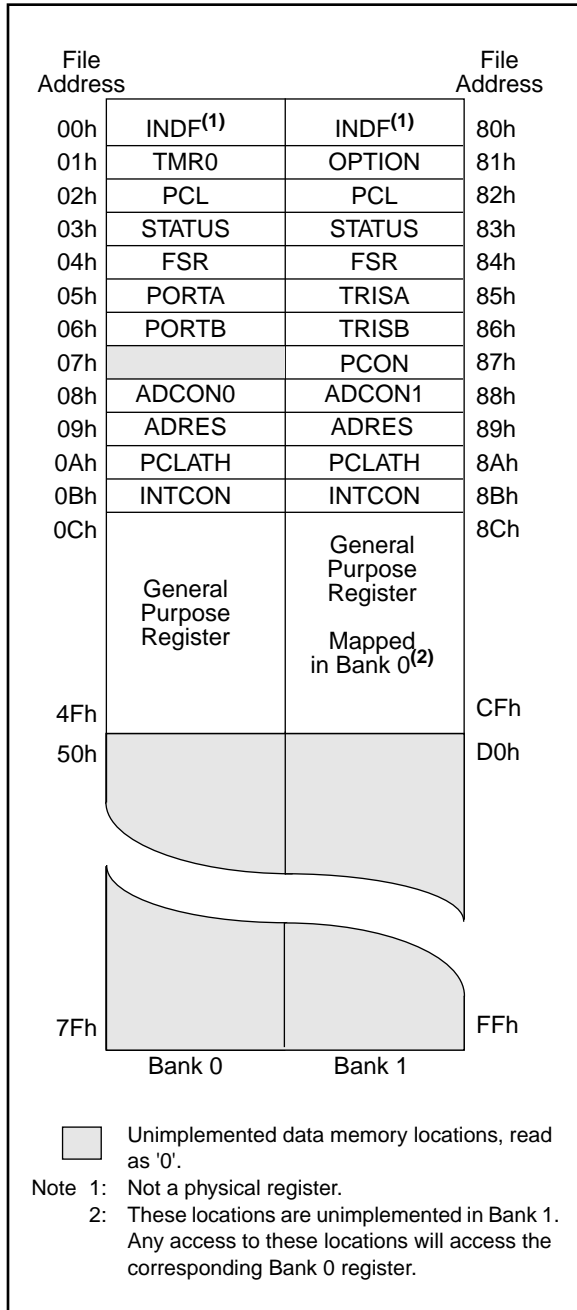
**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**



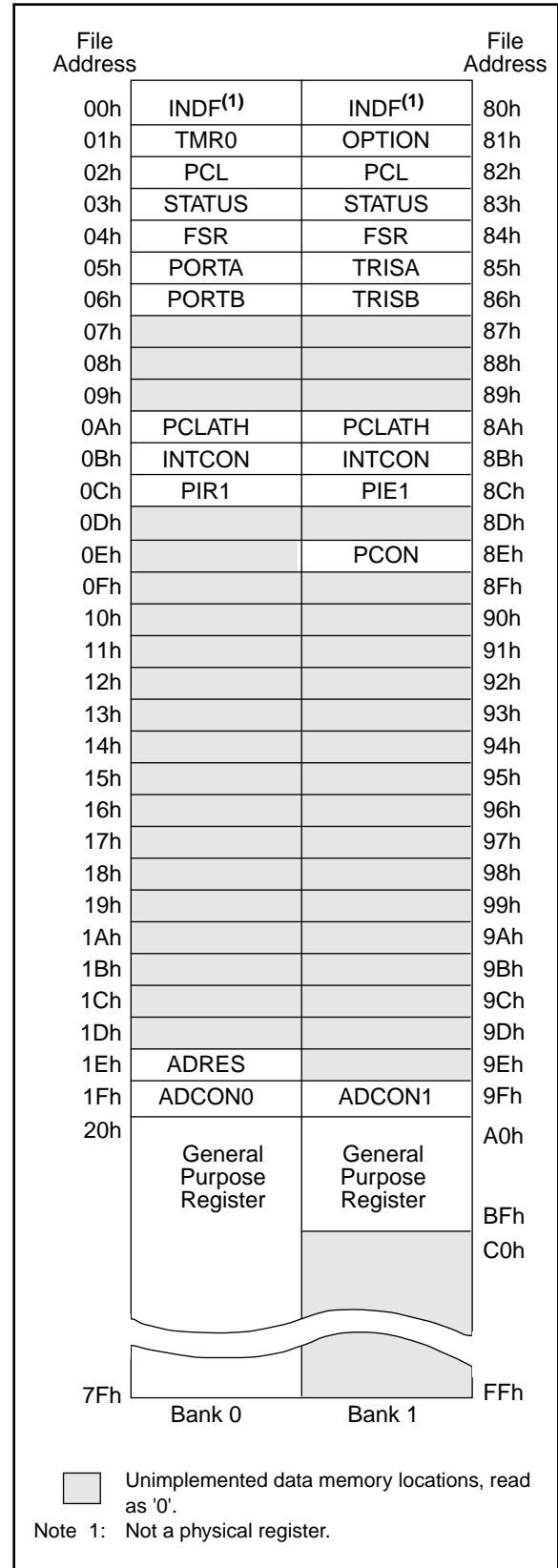
**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**



**FIGURE 4-5: PIC16C711 REGISTER FILE MAP**



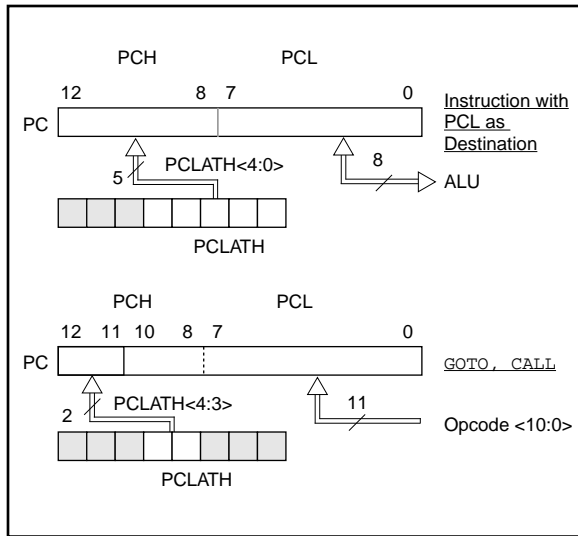
**FIGURE 4-6: PIC16C715 REGISTER FILE MAP**



## 4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The upper bits (PC<12:8>) are not readable, but are indirectly writable through the PCLATH register. On any reset, the upper bits of the PC will be cleared. Figure 4-14 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

**FIGURE 4-14: LOADING OF PC IN DIFFERENT SITUATIONS**



### 4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (`ADDWF PCL`). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Implementing a Table Read" (AN556).

### 4.3.2 STACK

The PIC16CXX family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

**Note 1:** There are no status bits to indicate stack overflow or stack underflow conditions.

**Note 2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

## 4.4 Program Memory Paging

The PIC16C71X devices ignore both paging bits (PCLATH<4:3>, which are used to access program memory when more than one page is available. The use of PCLATH<4:3> as general purpose read/write bits for the PIC16C71X is not recommended since this may affect upward compatibility with future products.

# PIC16C71X

**TABLE 5-1: PORTA FUNCTIONS**

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input/VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type

Legend: TTL = TTL input, ST = Schmitt Trigger input

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
9Fh	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

# PIC16C71X

---

## 7.4 A/D Conversions

Example 7-2 shows how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 pin (channel 0).

**Note:** The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

### EXAMPLE 7-2: A/D CONVERSION

```
BSF    STATUS, RP0           ; Select Bank 1
CLRF   ADCON1                ; Configure A/D inputs
BCF    STATUS, RP0           ; Select Bank 0
MOVLW  0xC1                  ; RC Clock, A/D is on, Channel 0 is selected
MOVWF  ADCON0                ;
BSF    INTCON, ADIE          ; Enable A/D Interrupt
BSF    INTCON, GIE           ; Enable all interrupts
;
; Ensure that the required sampling time for the selected input channel has elapsed.
; Then the conversion may be started.
;
BSF    ADCON0, GO            ; Start A/D Conversion
      :                      ; The ADIF bit will be set and the GO/DONE bit
      :                      ; is cleared upon completion of the A/D Conversion.
```

## INCFSZ Increment f, Skip if 0

**Syntax:** [ *label* ] INCFSZ *f*,*d*

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) + 1 \rightarrow (\text{dest})$ , skip if result = 0

**Status Affected:** None

**Encoding:**

00	1111	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2TCY instruction.

**Words:** 1

**Cycles:** 1(2)

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

**If Skip:** (2nd Cycle)

Q1	Q2	Q3	Q4
NOP	NOP	NOP	NOP

**Example**

```

HERE      INCFSZ    CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
  
```

**Before Instruction**  
PC = address HERE

**After Instruction**  
CNT = CNT + 1  
if CNT= 0,  
PC = address CONTINUE  
if CNT≠ 0,  
PC = address HERE +1

## IORLW Inclusive OR Literal with W

**Syntax:** [ *label* ] IORLW *k*

**Operands:**  $0 \leq k \leq 255$

**Operation:**  $(W) .OR. k \rightarrow (W)$

**Status Affected:** Z

**Encoding:**

11	1000	kkkk	kkkk
----	------	------	------

**Description:** The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

**Example**

```

IORLW    0x35
  
```

**Before Instruction**  
W = 0x9A

**After Instruction**  
W = 0xBF  
Z = 1



# PIC16C71X

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C75X	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
<b>Emulator Products</b>												
PICMASTER® / PICMASTER-CE In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	Available 3097		
ICEPIC Low-Cost In-Circuit Emulator	✓		✓	✓	✓	✓	✓					
<b>Software Tools</b>												
MPLAB™ Integrated Development Environment			✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ C Compiler	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓			
MP-DriveWay™ Applications Code Generator			✓	✓	✓	✓	✓		✓			
Total Endurance™ Software Model											✓	
<b>Programmers</b>												
PICSTART® Lite Ultra Low-Cost Dev. Kit			✓		✓	✓	✓					
PICSTART® Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEELOQ® Programmer												
SEEVAL® Designers Kit											✓	
<b>Demo Boards</b>												
PICDEM-1		✓		✓			✓		✓			
PICDEM-2					✓							
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓

# PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 11-6: TIMER0 EXTERNAL CLOCK TIMINGS



TABLE 11-5: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	Must also meet parameter 42
			With Prescaler	$10^*$	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	Must also meet parameter 42
			With Prescaler	$10^*$	—	—	ns	
42	Tt0P	T0CKI Period	Greater of: $20 \text{ ns or } \frac{T_{CY} + 40^*}{N}$		—	—	ns	N = prescale value (2, 4, ..., 256)
48	Tcke2tmr1	Delay from external clock edge to timer increment	$2T_{osc}$	—	$7T_{osc}$	—		

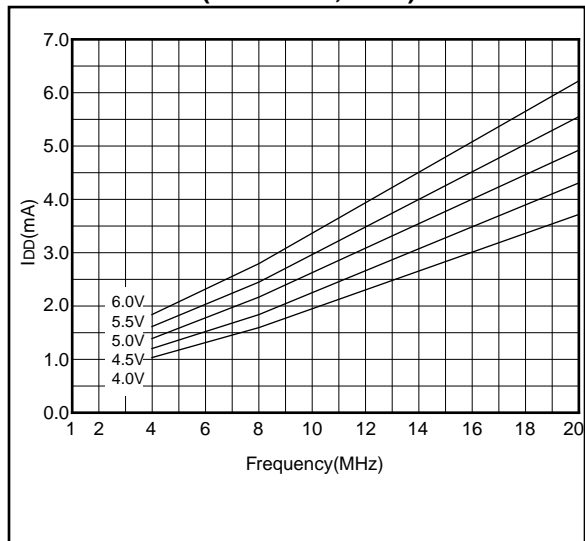
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

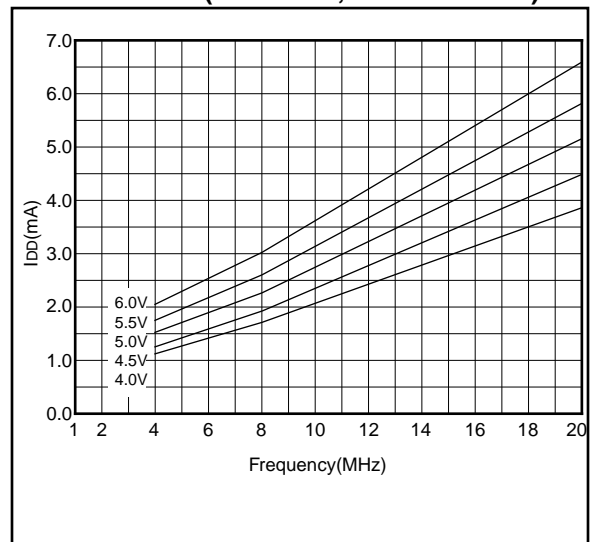
# PIC16C71X

Applicable Devices 710 71 711 715

**FIGURE 12-29: TYPICAL  $I_{DD}$  vs. FREQUENCY  
(HS MODE, 25°C)**



**FIGURE 12-30: MAXIMUM  $I_{DD}$  vs.  
FREQUENCY  
(HS MODE, -40°C TO 85°C)**



# PIC16C71X

Applicable Devices 710 71 711 715

## 13.5 Timing Diagrams and Specifications

FIGURE 13-2: EXTERNAL CLOCK TIMING

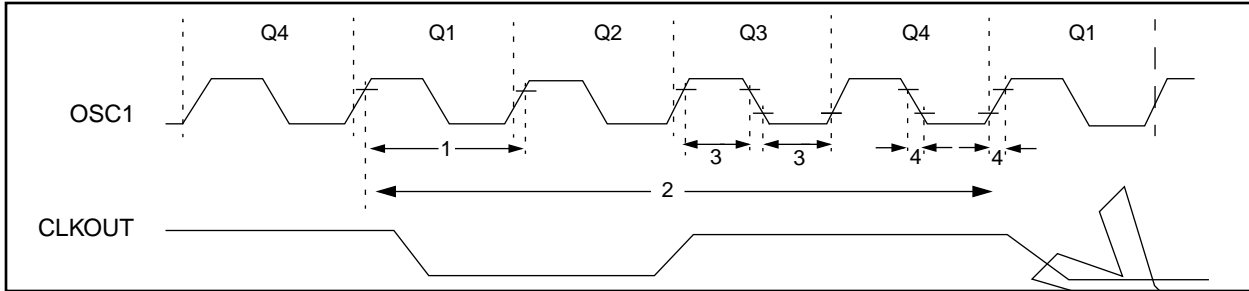


TABLE 13-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fos	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT osc mode
			DC	—	4	MHz	HS osc mode (PIC16C715-04)
			DC	—	20	MHz	HS osc mode (PIC16C715-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	4	MHz	HS osc mode (PIC16C715-04)
			4	—	10	MHz	HS osc mode (PIC16C715-10)
			4	—	20	MHz	HS osc mode (PIC16C715-20)
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (PIC16C715-04)
			100	—	—	ns	HS osc mode (PIC16C715-10)
			50	—	—	ns	HS osc mode (PIC16C715-20)
			5	—	—	μs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C715-04)
			100	—	250	ns	HS osc mode (PIC16C715-10)
			50	—	250	ns	HS osc mode (PIC16C715-20)
5	—	—	μs	LP osc mode			
2	Tcy	Instruction Cycle Time (Note 1)	200	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	50	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

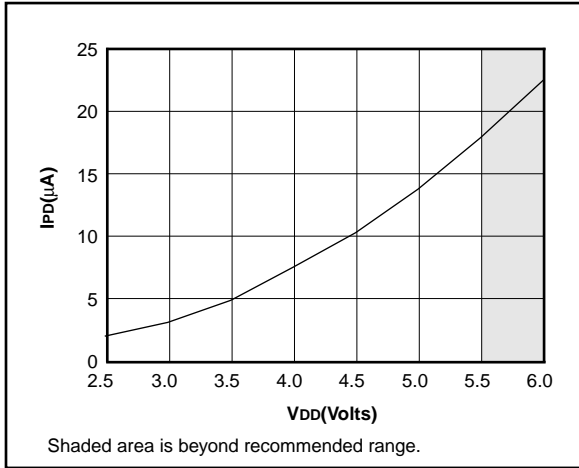
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C715.

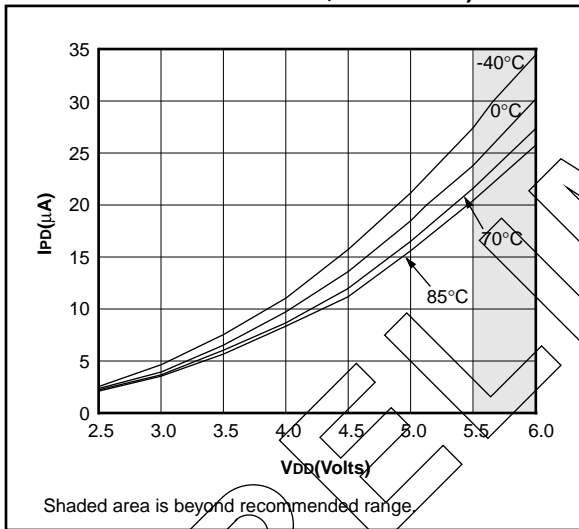
# PIC16C71X

Applicable Devices 710 71 711 715

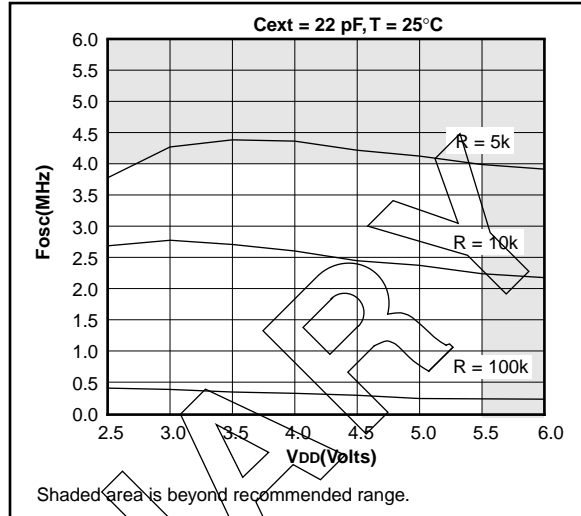
**FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)**



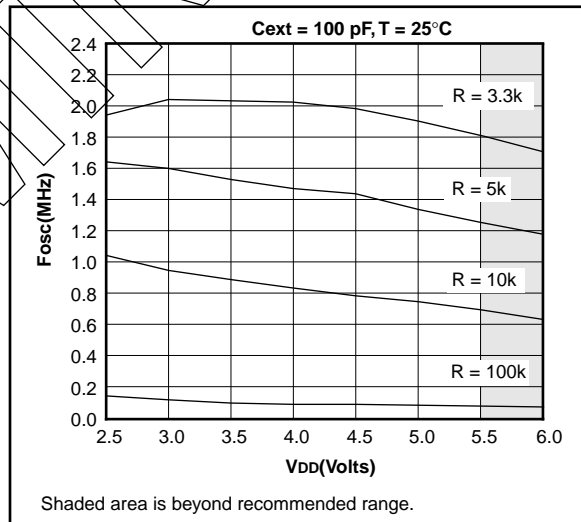
**FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)**



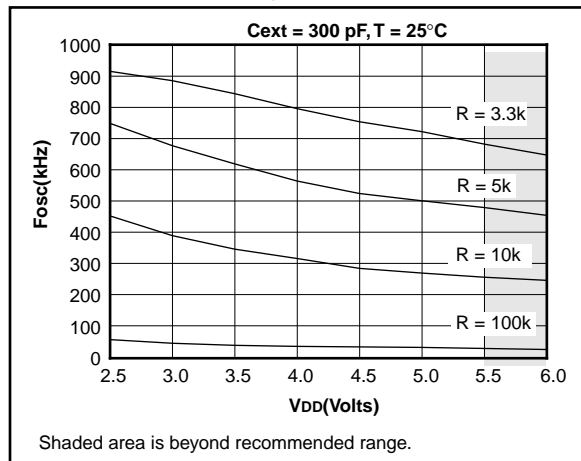
**FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



**FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



**FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



# PIC16C71X

Applicable Devices 710 71 711 715

## 15.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	- -	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010  D013	Supply Current (Note 2)	IDD	- -	1.8 13.5	3.3 30	mA mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)  HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3)	IPD	- - -	7 1.0 1.0	28 14 16	μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = VDD/2R_{ext}$  (mA) with Rext in kOhm.

**FIGURE 16-12: TYPICAL  $I_{DD}$  vs. FREQ (EXT CLOCK, 25°C)**

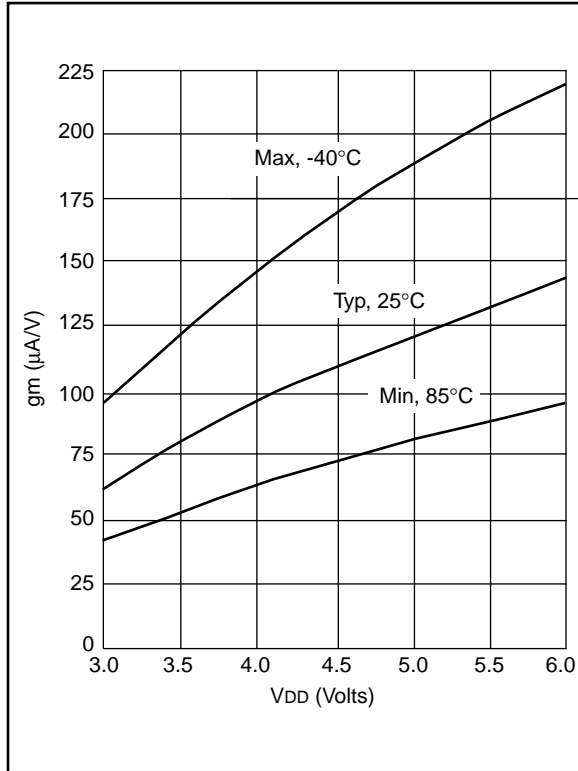


**FIGURE 16-13: MAXIMUM,  $I_{DD}$  vs. FREQ (EXT CLOCK, -40° TO +85°C)**

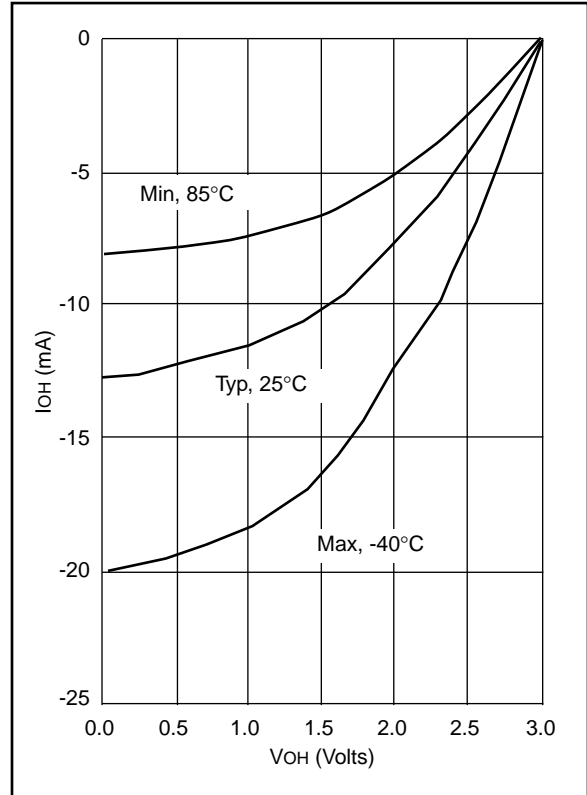


Data based on matrix samples. See first page of this section for details.

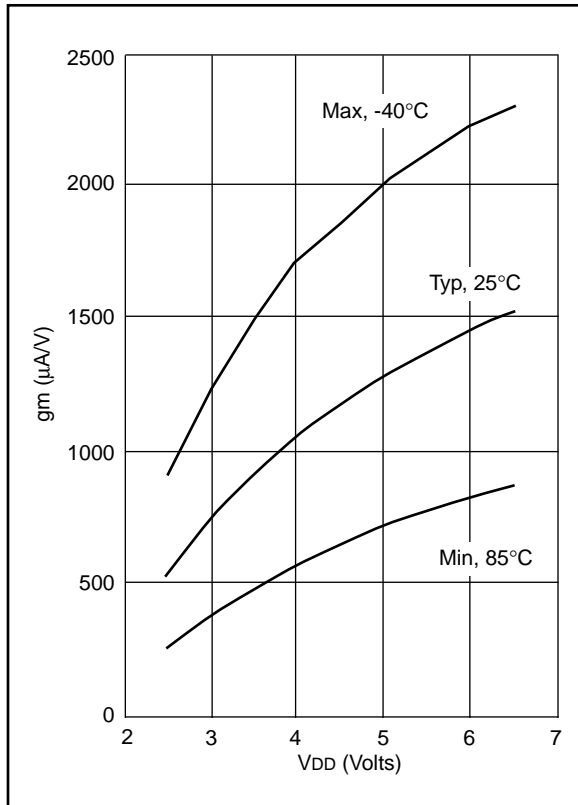
**FIGURE 16-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**



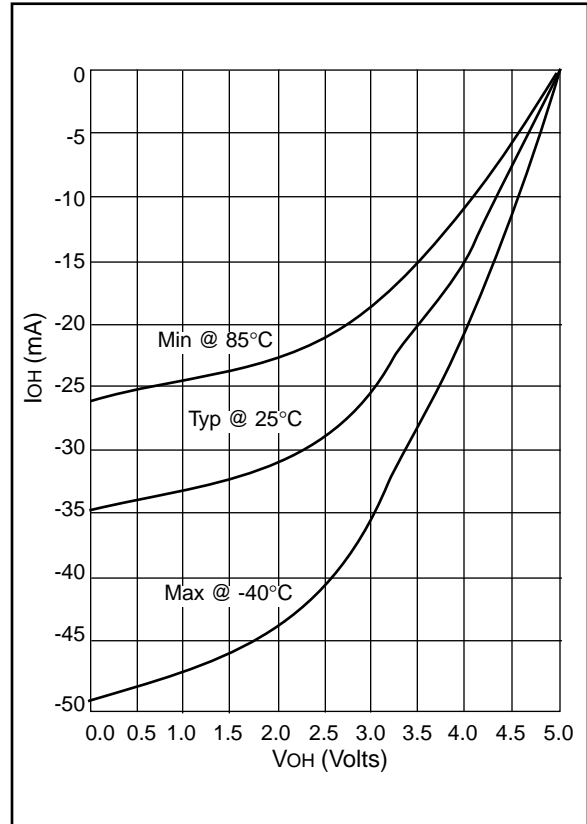
**FIGURE 16-19: I<sub>OH</sub> vs. V<sub>OH</sub>, VDD = 3V**



**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**



**FIGURE 16-20: I<sub>OH</sub> vs. V<sub>OH</sub>, VDD = 5V**



Data based on matrix samples. See first page of this section for details.



# PIC16C71X

---

## APPENDIX C: WHAT'S NEW

1. Consolidated all pin compatible 18-pin A/D based devices into one data sheet.

## APPENDIX D: WHAT'S CHANGED

1. Minor changes, spelling and grammatical changes.
2. Low voltage operation on the PIC16LC710/711/715 has been reduced from 3.0V to 2.5V.
3. Part numbers of the PIC16C70 and PIC16C71A have changed to PIC16C710 and PIC16C711, respectively.

## INDEX

### A

#### A/D

Accuracy/Error	44
ADIF bit	39
Analog Input Model Block Diagram	40
Analog-to-Digital Converter	37
Configuring Analog Port Pins	41
Configuring the Interrupt	39
Configuring the Module	39
Connection Considerations	44
Conversion Clock	41
Conversion Time	43
Conversions	42
Converter Characteristics	99, 122, 145
Delays	40
Effects of a Reset	44
Equations	40
Faster Conversion - Lower Resolution Trade-off	43
Flowchart of A/D Operation	45
GO/DONE bit	39
Internal Sampling Switch (Rss) Impedence	40
Minimum Charging Time	40
Operation During Sleep	44
Sampling Requirements	40
Source Impedence	40
Time Delays	40
Transfer Function	45
Absolute Maximum Ratings	89, 111, 135

#### AC Characteristics

PIC16C710	101
PIC16C711	101
PIC16C715	125

ADCON0 Register	37
ADCON1	37
ADCON1 Register	14, 37
ADCS0 bit	37
ADCS1 bit	37
ADIE bit	19, 20
ADIF bit	21, 37
ADON bit	37
ADRES Register	15, 37, 39
ALU	7

#### Application Notes

AN546	37
AN552	27
AN556	23
AN607, Power-up Trouble Shooting	53

#### Architecture

Harvard	7
Overview	7
von Neumann	7

#### Assembler

MPASM Assembler	86
-----------------	----

### B

#### Block Diagrams

Analog Input Model	40
On-Chip Reset Circuit	52
PIC16C71X	8
RA3/RA0 Port Pins	25
RA4/T0CKI Pin	25
RB3:RB0 Port Pins	27
RB7:RB4 Pins	28

RB7:RB4 Port Pins	28
Timer0	31
Timer0/WDT Prescaler	34
Watchdog Timer	65
BODEN bit	48
BOR bit	22, 54
Brown-out Reset (BOR)	53

### C

C bit	17
C16C71	47
Carry bit	7
CHS0 bit	37
CHS1 bit	37
Clocking Scheme	10
Code Examples	
Call of a Subroutine in Page 1 from Page 0	24
Changing Prescaler (Timer0 to WDT)	35
Changing Prescaler (WDT to Timer0)	35
Doing an A/D Conversion	42
I/O Programming	30
Indirect Addressing	24
Initializing PORTA	25
Initializing PORTB	27
Saving STATUS and W Registers in RAM	64
Code Protection	47, 67
Computed GOTO	23
Configuration Bits	47
CP0 bit	47, 48
CP1 bit	48

### D

DC bit	17
DC Characteristics	147
PIC16C71	136
PIC16C710	90, 101
PIC16C711	90, 101
PIC16C715	113, 125
Development Support	3, 85
Development Tools	85
Diagrams - See Block Diagrams	
Digit Carry bit	7
Direct Addressing	24

### E

#### Electrical Characteristics

PIC16C71	135
PIC16C710	89
PIC16C711	89
PIC16C715	111
External Brown-out Protection Circuit	60
External Power-on Reset Circuit	60

### F

#### Family of Devices

PIC16C71X	4
FOSC0 bit	47, 48
FOSC1 bit	47, 48
FSR Register	15, 16, 24
Fuzzy Logic Dev. System (fuzzyTECH <sup>®</sup> -MP)	87

### G

General Description	3
GIE bit	19, 61
GO/DONE bit	37

# PIC16C71X

RA2/AN2 .....	9	PIC16C711 .....	13
RA3/AN3/VREF .....	9	PIC16C715 .....	13
RA4/T0CKI .....	9	Reset Conditions .....	56
RB0/INT .....	9	Summary .....	14-??
RB1 .....	9	Reset .....	47, 52
RB2 .....	9	Reset Conditions for Special Registers .....	56
RB3 .....	9	RP0 bit .....	12, 17
RB4 .....	9	RP1 bit .....	17
RB5 .....	9	<b>S</b>	
RB6 .....	9	SEEVAL <sup>®</sup> Evaluation and Programming System .....	87
RB7 .....	9	Services	
VDD .....	9	One-Time-Programmable (OTP) Devices .....	5
Vss .....	9	Quick-Turnaround-Production (QTP) Devices .....	5
Pinout Descriptions		Serialized Quick-Turnaround Production (SQTP) Devices .....	5
PIC16C71 .....	9	SLEEP .....	47, 52
PIC16C710 .....	9	Software Simulator (MPLAB <sup>™</sup> SIM) .....	87
PIC16C711 .....	9	Special Features of the CPU .....	47
PIC16C715 .....	9	Special Function Registers	
PIR1 Register .....	21	PIC16C71 .....	14
POP .....	23	PIC16C710 .....	14
POR .....	53, 54	PIC16C711 .....	14
Oscillator Start-up Timer (OST) .....	47, 53	Special Function Registers, Section .....	14
Power Control Register (PCON) .....	54	Stack .....	23
Power-on Reset (POR) .....	47, 53, 57, 58	Overflows .....	23
Power-up Timer (PWRT) .....	47, 53	Underflow .....	23
Time-out Sequence .....	54	STATUS Register .....	17
Time-out Sequence on Power-up .....	59	<b>T</b>	
T0 .....	52, 55	T0CS bit .....	18
POR bit .....	22, 54	T0IE bit .....	19
Port RB Interrupt .....	63	T0IF bit .....	19
PORTA .....	57, 58	TAD .....	41
PORTA Register .....	14, 15, 25	Timer0	
PORTB .....	57, 58	RTCC .....	57, 58
PORTB Register .....	14, 15, 27	Timers	
Power-down Mode (SLEEP) .....	66	Timer0	
Prescaler, Switching Between Timer0 and WDT .....	35	Block Diagram .....	31
PRO MATE <sup>®</sup> II Universal Programmer .....	85	External Clock .....	33
Program Branches .....	7	External Clock Timing .....	33
Program Memory		Increment Delay .....	33
Paging .....	23	Interrupt .....	31
Program Memory Maps		Interrupt Timing .....	32
PIC16C71 .....	11	Prescaler .....	34
PIC16C710 .....	11	Prescaler Block Diagram .....	34
PIC16C711 .....	11	Section .....	31
PIC16C715 .....	11	Switching Prescaler Assignment .....	35
Program Verification .....	67	Synchronization .....	33
PS0 bit .....	18	T0CKI .....	33
PS1 bit .....	18	T0IF .....	63
PS2 bit .....	18	Timing .....	31
PSA bit .....	18	TMR0 Interrupt .....	63
PUSH .....	23	Timing Diagrams	
PWRT		A/D Conversion .....	100, 124, 146
Power-up Timer (PWRT) .....	53	Brown-out Reset .....	53, 97
PWRTE bit .....	47, 48	CLKOUT and I/O .....	96, 119, 142
<b>R</b>		External Clock Timing .....	95, 118, 141
RBIE bit .....	19	Power-up Timer .....	97, 143
RBIF bit .....	19, 27, 63	Reset .....	97, 143
RBPU bit .....	18	Start-up Timer .....	97, 143
RC .....	54	Time-out Sequence .....	59
RC Oscillator .....	51, 54	Timer0 .....	31, 98, 121, 144
Read-Modify-Write .....	30	Timer0 Interrupt Timing .....	32
Register File .....	12	Timer0 with External Clock .....	33
Registers		Wake-up from SLEEP through Interrupt .....	67
Maps		Watchdog Timer .....	97, 143
PIC16C71 .....	12		
PIC16C710 .....	12		

# PIC16C71X

Figure 14-6:	Typical RC Oscillator Frequency vs. VDD.....	126	Figure 16-4:	Typical RC Oscillator Frequency vs. VDD .....	148
Figure 14-7:	Typical RC Oscillator Frequency vs. VDD.....	126	Figure 16-5:	Typical I <sub>pd</sub> vs. VDD Watchdog Timer Disabled 25°C.....	148
Figure 14-8:	Typical I <sub>PD</sub> vs. VDD Brown-out Detect Enabled (RC Mode) .....	127	Figure 16-6:	Typical I <sub>pd</sub> vs. VDD Watchdog Timer Enabled 25°C.....	148
Figure 14-9:	Maximum I <sub>PD</sub> vs. VDD Brown-out Detect Enabled (85°C to -40°C, RC Mode) .....	127	Figure 16-7:	Maximum I <sub>pd</sub> vs. VDD Watchdog Disabled .....	149
Figure 14-10:	Typical I <sub>PD</sub> vs. Timer1 Enabled (32 kHz, RC0/RC1 = 33 pF/33 pF, RC Mode) .....	127	Figure 16-8:	Maximum I <sub>pd</sub> vs. VDD Watchdog Enabled.....	149
Figure 14-11:	Maximum I <sub>PD</sub> vs. Timer1 Enabled (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C to -40°C, RC Mode).....	127	Figure 16-9:	V <sub>th</sub> (Input Threshold Voltage) of I/O Pins vs. VDD.....	149
Figure 14-12:	Typical I <sub>DD</sub> vs. Frequency (RC Mode @ 22 pF, 25°C).....	128	Figure 16-10:	V <sub>IH</sub> , V <sub>IL</sub> of MCLR, T0CKI and OSC1 (in RC Mode) vs. VDD .....	150
Figure 14-13:	Maximum I <sub>DD</sub> vs. Frequency (RC Mode @ 22 pF, -40°C to 85°C).....	128	Figure 16-11:	V <sub>TH</sub> (Input Threshold Voltage) of OSC1 Input (in XT, HS, and LP Modes) vs. VDD .....	150
Figure 14-14:	Typical I <sub>DD</sub> vs. Frequency (RC Mode @ 100 pF, 25°C).....	129	Figure 16-12:	Typical I <sub>DD</sub> vs. Freq (Ext Clock, 25°C)....	151
Figure 14-15:	Maximum I <sub>DD</sub> vs. Frequency (RC Mode @ 100 pF, -40°C to 85°C).....	129	Figure 16-13:	Maximum, I <sub>DD</sub> vs. Freq (Ext Clock, -40° to +85°C).....	151
Figure 14-16:	Typical I <sub>DD</sub> vs. Frequency (RC Mode @ 300 pF, 25°C).....	130	Figure 16-14:	Maximum I <sub>DD</sub> vs. Freq with A/D Off (Ext Clock, -55° to +125°C) .....	152
Figure 14-17:	Maximum I <sub>DD</sub> vs. Frequency (RC Mode @ 300 pF, -40°C to 85°C).....	130	Figure 16-15:	WDT Timer Time-out Period vs. VDD.....	152
Figure 14-18:	Typical I <sub>DD</sub> vs. Capacitance @ 500 kHz (RC Mode).....	131	Figure 16-16:	Transconductance (gm) of HS Oscillator vs. VDD.....	152
Figure 14-19:	Transconductance(gm) of HS Oscillator vs. VDD .....	131	Figure 16-17:	Transconductance (gm) of LP Oscillator vs. VDD .....	153
Figure 14-20:	Transconductance(gm) of LP Oscillator vs. VDD.....	131	Figure 16-18:	Transconductance (gm) of XT Oscillator vs. VDD .....	153
Figure 14-21:	Transconductance(gm) of XT Oscillator vs. VDD .....	131	Figure 16-19:	I <sub>OH</sub> vs. V <sub>OH</sub> , VDD = 3V .....	153
Figure 14-22:	Typical XTAL Startup Time vs. VDD (LP Mode, 25°C).....	132	Figure 16-20:	I <sub>OH</sub> vs. V <sub>OH</sub> , VDD = 5V .....	153
Figure 14-23:	Typical XTAL Startup Time vs. VDD (HS Mode, 25°C) .....	132	Figure 16-21:	I <sub>OL</sub> vs. V <sub>OL</sub> , VDD = 3V .....	154
Figure 14-24:	Typical XTAL Startup Time vs. VDD (XT Mode, 25°C).....	132	Figure 16-22:	I <sub>OL</sub> vs. V <sub>OL</sub> , VDD = 5V .....	154
Figure 14-25:	Typical I <sub>DD</sub> vs. Frequency (LP Mode, 25°C) .....	133			
Figure 14-26:	Maximum I <sub>DD</sub> vs. Frequency (LP Mode, 85°C to -40°C) .....	133			
Figure 14-27:	Typical I <sub>DD</sub> vs. Frequency (XT Mode, 25°C) .....	133			
Figure 14-28:	Maximum I <sub>DD</sub> vs. Frequency (XT Mode, -40°C to 85°C).....	133			
Figure 14-29:	Typical I <sub>DD</sub> vs. Frequency (HS Mode, 25°C).....	134			
Figure 14-30:	Maximum I <sub>DD</sub> vs. Frequency (HS Mode, -40°C to 85°C).....	134			
Figure 15-1:	Load Conditions .....	140			
Figure 15-2:	External Clock Timing .....	141			
Figure 15-3:	CLKOUT and I/O Timing .....	142			
Figure 15-4:	Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing .....	143			
Figure 15-5:	Timer0 External Clock Timings .....	144			
Figure 15-6:	A/D Conversion Timing .....	146			
Figure 16-1:	Typical RC Oscillator Frequency vs. Temperature.....	147			
Figure 16-2:	Typical RC Oscillator Frequency vs. VDD.....	147			
Figure 16-3:	Typical RC Oscillator Frequency vs. VDD.....	147			

---

---

**Note the following details of the code protection feature on PICmicro® MCUs.**

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### **Trademarks**


The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

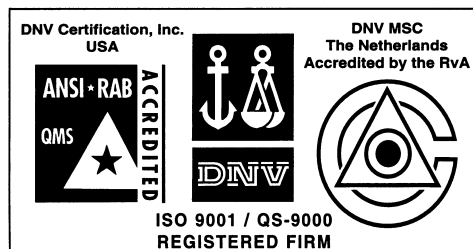
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*