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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 × 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-04e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 <sup>(1)</sup>
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	512	1K	1K	2K	2К	—
Memory	ROM Program Memory (14K words)	_	_	_	_	_	2K
	Data Memory (bytes)	36	36	68	128	128	128
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Module(s)		—	_		1	1
	Serial Port(s) (SPI/I <sup>2</sup> C, USART)	_		_	_	SPI/I <sup>2</sup> C	SPI/I <sup>2</sup> C
	Parallel Slave Port	_	—	—	_	—	—
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	2.5-6.0	3.0-6.0	2.5-6.0	2.5-5.5	2.5-6.0	3.0-5.5
Features	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

# TABLE 1-1: PIC16C71X FAMILY OF DEVICES

		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
Memory	EPROM Program Memory (x14 words)	4K	4K	8K	8K
	Data Memory (bytes)	192	192	376	376
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Module(s)	2	2	2	2
	Serial Port(s) (SPI/I <sup>2</sup> C, USART)	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART	SPI/I <sup>2</sup> C, USART
	Parallel Slave Port	—	Yes	—	Yes
	A/D Converter (8-bit) Channels	5	8	5	8
	Interrupt Sources	11	12	11	12
	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
Features	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
- calures	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

Pin Name	DIP Pin#	SSOP Pin# <sup>(4)</sup>	SOIC Pin#	I/O/P Type	Buffer Type	Description			
OSC1/CLKIN	16	18	16	I	ST/CMOS <sup>(3)</sup>	Oscillator crystal input/external clock source input.			
OSC2/CLKOUT	15	17	15	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.			
MCLR/Vpp	4	4	4	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.			
						PORTA is a bi-directional I/O port.			
RA0/AN0	17	19	17	I/O	TTL	RA0 can also be analog input0			
RA1/AN1	18	20	18	I/O	TTL	RA1 can also be analog input1			
RA2/AN2	1	1	1	I/O	TTL	RA2 can also be analog input2			
RA3/AN3/VREF	2	2	2	I/O	TTL	RA3 can also be analog input3 or analog reference voltage			
RA4/T0CKI	3	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.			
						PORTB is a bi-directional I/O port. PORTB can be software pro- grammed for internal weak pull-up on all inputs.			
RB0/INT	6	7	6	I/O	TTL/ST <sup>(1)</sup>	RB0 can also be the external interrupt pin.			
RB1	7	8	7	I/O	TTL				
RB2	8	9	8	I/O	TTL				
RB3	9	10	9	I/O	TTL				
RB4	10	11	10	I/O	TTL	Interrupt on change pin.			
RB5	11	12	11	I/O	TTL	Interrupt on change pin.			
RB6	12	13	12	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming clock.			
RB7	13	14	13	I/O	TTL/ST(2)	Interrupt on change pin. Serial programming data.			
Vss	5	4, 6	5	Р	-	Ground reference for logic and I/O pins.			
Vdd	14	15, 16	14	Р	-	Positive supply for logic and I/O pins.			
Legend: I = inp	ut	O = outp	ut .	I	/O = input/out	put P = power			
		— = Not	used	-	IIL = TTL inp	ut SI = Schmitt Trigger input			

TABLE 3-1:	PIC16C710/71/711/715 PINOUT DESCRIPTION

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: The PIC16C71 is not available in SSOP package.

# FIGURE 4-5: PIC16C711 REGISTER FILE MAP



# FIGURE 4-6: PIC16C715 REGISTER FILE MAP

File Address	3		File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	
02h	PCL	PCL	
03h	STATUS	STATUS	83h
04h	FSR	FSR	
05h	PORTA	TRISA	
06h	PORTB	TRISB	
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			
11h			
12h			
13h			 93h
14h			
15h			95h
16h			96h
17h			97h
18h			
19h			
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh	ADRES		9Eh
1Fh	ADCON0	ADCON1	
20h	General Purpose	General Purpose	A0h
	Register	Register	BFh
			Con
7Fh	Bank 0	Bank 1	_ FFh
Note 1: N	Jnimplemented dat as '0'. Not a physical regis	a memory locatio	ons, read

#### 4.2.2.2 OPTION REGISTER

# Applicable Devices 710 71 711 715

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

## FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1 F	R/W-1 R/W-1	R/W-1	R/W-1	R/W-1	
RBPU bit7	INTEDG	TOCS	TOSE   PSA	PS2	PS1	PS0 bit0	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
bit 7:	<b>RBPU:</b> PO 1 = PORTE 0 = PORTE	RTB Pull-up 3 pull-ups ai 3 pull-ups ai	o Enable bit re disabled re enabled by inc	lividual port	latch value	es	
bit 6:	INTEDG: In 1 = Interrup 0 = Interrup	nterrupt Edg ot on rising ot on falling	ge Select bit edge of RB0/INT edge of RB0/INT	<sup>∙</sup> pin Γpin			
bit 5:	<b>TOCS:</b> TMF 1 = Transiti 0 = Interna	R0 Clock Sc on on RA4/ I instruction	ource Select bit T0CKI pin cycle clock (CLł	(OUT)			
bit 4:	<b>TOSE:</b> TMF 1 = Increm 0 = Increm	R0 Source E ent on high- ent on low-t	Edge Select bit to-low transition o-high transition	on RA4/T0 on RA4/T0	CKI pin CKI pin		
bit 3:	<b>PSA:</b> Prese 1 = Presca 0 = Presca	caler Assigr ler is assigr ler is assigr	nment bit ned to the WDT ned to the Timer(	) module			
bit 2-0:	PS2:PS0:	Prescaler R	ate Select bits				
	Bit Value	TMR0 Rate	WDT Rate				
	000 001 010 011 100 101 110 111	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128				

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

#### 7.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-5. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), Figure 7-5. The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 10 k** $\Omega$ . After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

#### EQUATION 7-1: A/D MINIMUM CHARGING TIME

 $\mathsf{VHOLD} = (\mathsf{VREF} - (\mathsf{VREF}/\mathsf{512})) \bullet (1 - e^{(\mathsf{-TCAP/CHOLD}(\mathsf{Ric} + \mathsf{Rss} + \mathsf{Rs}))})$ 

Given: VHOLD = (VREF/512), for 1/2 LSb resolution

The above equation reduces to:

 $TCAP = -(51.2 \text{ pF})(1 \text{ k}\Omega + \text{Rss} + \text{Rs}) \ln(1/511)$ 

Example 7-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

 $Rs = 10 \ k\Omega$ 

1/2 LSb error

 $V\text{DD} = 5\text{V} \rightarrow \text{Rss} = 7 \text{ k}\Omega$ 

Temp (application system max.) = 50°C

 $\mathsf{VHOLD}=0 @ t=0$ 



#### FIGURE 7-5: ANALOG INPUT MODEL

- Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.
- Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- Note 3: The maximum recommended impedance for analog sources is 10 k $\Omega$ . This is required to meet the pin leakage specification.
- Note 4: After a conversion has completed, a 2.0TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

## EXAMPLE 7-1: CALCULATING THE MINIMUM REQUIRED AQUISITION TIME

TACQ = Amplifier Settling Time +

Holding Capacitor Charging Time + Temperature Coefficient

- TACQ =  $5 \,\mu s + TCAP + [(Temp 25^{\circ}C)(0.05 \,\mu s/^{\circ}C)]$
- TCAP = -CHOLD (RIC + RSS + RS) ln(1/511)
  - -51.2 pF (1 kΩ + 7 kΩ + 10 kΩ) ln(0.0020) -51.2 pF (18 kΩ) ln(0.0020) -0.921 μs (-6.2364)

5.747 μs

TACQ = 5 μs + 5.747 μs + [(50°C - 25°C)(0.05 μs/°C)] 10.747 μs + 1.25 μs 11.997 μs

#### 7.4 <u>A/D Conversions</u>

Example 7-2 shows how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 pin (channel 0). **Note:** The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

# EXAMPLE 7-2: A/D CONVERSION

	BSF	STATUS,	RP0	;	Select	Banł	c 1					
	CLRF	ADCON1		;	Config	ure A	A/D i	nputs				
	BCF	STATUS,	RP0	;	Select	Banł	c 0					
	MOVLW	0xC1		;	RC Clo	ck, A	A/D i	s on, Cha	annel (	0 is sel	ected	d
	MOVWF	ADCON0		;								
	BSF	INTCON,	ADIE	;	Enable	A/D	Inte	errupt				
	BSF	INTCON,	GIE	;	Enable	all	inte	errupts				
En	sure tha	at the re	equired	samplin	g time	for	the	selected	input	channel	has	elapsed.

Then the conversion may be started.

;

;;

;

BSF	ADCON0, GO	; Start A/D Conversion
:		; The ADIF bit will be set and the GO/DONE bit
:		; is cleared upon completion of the A/D Conversion.

## 7.9 <u>Transfer Function</u>

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is Analog VREF/256 (Figure 7-6).

## 7.10 <u>References</u>

A very good reference for understanding A/D converters is the "Analog-Digital Conversion Handbook" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).



ADON = 0Yes ADON = 0 No Acquire Selected Channel Yes GO = 0? No Start of A/D onversion Delaye Instruction Cycle Yes A/D Clock = RC? /es SLEEP Finish Conversior Inst uction GO = 0 ADIF = 1 No No Yes Abort Conversion Yes Wake-up From Sleep inish Conversio Device in SLEEP? Wait 2 TAD GO = 0ADIF = 0 GO = 0 ADIF = 1 No No SLEEP Power-down A/D Finish Conversion Stay in Sleep Power-down A/D Wait 2 TAD GO = 0 ADIF = 1 Wait 2 TAD

FIGURE 7-7: FLOWCHART OF A/D OPERATION

#### FIGURE 8-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
  - R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
  - 3:  $R1 = 100\Omega$  to  $1 k\Omega$  will limit any current flowing into  $\overline{MCLR}$  from external capacitor C in the event of  $\overline{MCLR}/VPP$  pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

#### FIGURE 8-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

## FIGURE 8-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

#### 11.2 **DC Characteristics:** PIC16LC710-04 (Commercial, Industrial, Extended) PIC16LC711-04 (Commercial, Industrial, Extended)

DC CHAR	ACTERISTICS		<b>Standa</b> Operat	ard Ope ing tem	erating peratu	<b>g Cond</b> i ire 0° -4	itions (unless otherwise stated) $C \leq T_A \leq +70^{\circ}C$ (commercial) $0^{\circ}C \leq T_A \leq +85^{\circ}C$ (industrial) $0^{\circ}C \leq T_A \leq +125^{\circ}C$ (extended)
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001	Supply Voltage Commercial/Industrial Extended	Vdd Vdd	2.5 3.0	-	6.0 6.0	V V	LP, XT, RC osc configuration (DC - 4 MHz) LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power- on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	Svdd	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled
D015	Brown-out Reset Current (Note 5)	$\Delta$ IBOR	-	300*	500	μA	BOR enabled VDD = 5.0V
D020 D021 D021A D021B D023	Power-down Current (Note 3) Brown-out Reset Current (Note 5)	IPD ΔIBOR		7.5 0.9 0.9 0.9 300*	30 5 5 10 500	μΑ μΑ μΑ μΑ μΑ	$VDD = 3.0V, WDT enabled, -40^{\circ}C to +85^{\circ}C$ $VDD = 3.0V, WDT disabled, 0^{\circ}C to +70^{\circ}C$ $VDD = 3.0V, WDT disabled, -40^{\circ}C to +85^{\circ}C$ $VDD = 3.0V, WDT disabled, -40^{\circ}C to +125^{\circ}C$ $BOR enabled VDD = 5.0V$

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only † and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD  $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

## FIGURE 11-3: CLKOUT AND I/O TIMING



# TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
	<b>T</b> 110 11							
10*	TosH2ckL	OSC1 <sup>T</sup> to CLKOUT↓			15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time			5	15	ns	Note 1
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid	b		_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOL	JT ↑	0.25Tcy + 25	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT	0	_	—	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to	—	—	80 - 100	ns		
		Port out valid						
18*	TosH2iol	OSC1 <sup>↑</sup> (Q2 cycle) to		TBD	—	—	ns	
		Port input invalid (I/O in ho	ld time)					
19*	TioV2osH	Port input valid to OSC11	(I/O in setup time)	TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 710/711		10	25	ns	
			PIC16LC710/711	—	—	60	ns	
21*	TioF	Port output fall time	Port output fall time PIC16 <b>C</b> 710/711		10	25	ns	
			—	—	60	ns		
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high	or low time	20	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

tt These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.



# FIGURE 11-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

#### FIGURE 11-5: BROWN-OUT RESET TIMING



# TABLE 11-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER,<br/>AND BROWN-OUT RESET REQUIREMENTS

Parameter	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
No.							
30	TmcL	MCLR Pulse Width (low)	1	_	—	μs	VDD = 5V, -40°C to +125°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	_	1024Tosc	—	-	Tosc = OSC1 period
33	Tpwrt	Power up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +125°C
34	Tıoz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	_	_	1.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—	—	μs	$3.8V \leq VDD \leq 4.2V$

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

# TABLE 11-6:A/D CONVERTER CHARACTERISTICS:<br/>PIC16C710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16C710/711-10 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16LC710/711-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16LC710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Param	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
NO.							
A01	Nr	Resolution	—	—	8-bits	bit	$VREF=VDD,VSS\leqAIN\leqVREF$
A02	Eabs	Absolute error	—	—	<±1	LSb	$VREF=VDD,VSS\leqAIN\leqVREF$
A03	EIL	Integral linearity error	—	—	<±1	LSb	$VREF=VDD,VSS\leqAIN\leqVREF$
A04	Edl	Differential linearity error	_	_	< ± 1	LSb	$VREF=VDD,VSS\leqAIN\leqVREF$
A05	Efs	Full scale error	—	—	< ± 1	LSb	$VREF = VDD,  VSS \le AIN \le VREF$
A06	EOFF	Offset error	—	—	< ± 1	LSb	$VREF = VDD,  VSS \le AIN \le VREF$
A10	—	Monotonicity	—	guaranteed		—	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference voltage	2.5V	_	Vdd + 0.3	V	
A25	VAIN	Analog input voltage	Vss - 0.3	_	Vref + 0.3	V	
A30	Zain	Recommended impedance of analog voltage source		_	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	_	180	_	μA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	_	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1.
			-	-	10	μΑ	During A/D Conversion cycle

These parameters are characterized but not tested.

\*

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current.

The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.









#### FIGURE 12-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



## FIGURE 12-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD







# Applicable Devices71071711715

#### 13.2 DC Characteristics: PIC16LC715-04 (Commercial, Industrial)

DC CHAF	ACTERISTICS	Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C$ $\leq TA \leq +85^{\circ}C$ (industrial)						
Param No.	Characteristic	Sym	Min	Тур†	Мах	Units	Conditions	
D001	Supply Voltage	Vdd	2.5	-	5.5	V	LP, XT, RC osc configuration (DC - 4 MHz)	
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	Device in SLEEP mode	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details	
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Rower-on Reset for details	
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN configuration bit is enabled	
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)	
D010A			-	22.5	48	βıΑ	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled	
D015	Brown-out Reset Current (Note 5)	$\Delta$ IBOR	-	300*	500	μÀ	BOR enabled VDD = 5.0V	
D020 D021 D021A	Power-down Current (Note 3)	IPD		7.5 0.9 0.9	35 5	μ <b>Α</b> μΑ μΑ	$VDD = 3.0V, WDT enabled, -40^{\circ}C to +85^{\circ}C$ $VDD = 3.0V, WDT disabled, 0^{\circ}C to +70^{\circ}C$ $VDD = 3.0V, WDT disabled, -40^{\circ}C to +85^{\circ}C$	
D023	Brown-out Reset Current (Note 5)		- `	300*	500	μA	BOR enabled VDD = 5.0V	

These parameters are characterized but pot tested.

+ Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, escillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

ØSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

 $\overline{MCLR} = VDR; WDT$  enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

# PIC16C71X

# Applicable Devices 710 71 711 715





## TABLE 13-5: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20*		_	ns	
			With Prescaler	10*	[ —	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20*	-	_	ns	
			With Prescaler	10*	-	_	ns	
42	Tt0P	T0CKI Period		Greater of: 20µs or <u>Tcy + 40</u> * N	_	_	ns	N = prescale value (1, 2, 4,, 256)
48	Tcke2tmrl	Delay from external clock edge	to timer increment	2Tosc	—	7Tosc	—	

- \* These parameters are characterized but not tested.  $\checkmark$
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)OOperating temperature $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C$ $\leq TA \leq +85^{\circ}C$ (industrial)Operating voltage VDD range as described in DC spec Section 15.1and Section 15.2.						
Param	Characteristic	Sym	Min	Typ +	Мах	Units	Conditions		
NO.	Conscitive Londing Space on								
	Output Pins								
D100	OSC2 pin	Cosc2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Сю			50	pF			
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only									

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 3: Negative current is defined as current sourced by the pin.

3: Negative current is defined as current sourced by the pin.

4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.



# FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

# TABLE 15-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP<br/>TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	200	_	_	ns	VDD = 5V, -40°C to +85°C
31	Twdt	Watchdog Timer Time-out Period	7*	18	33*	ms	VDD = 5V, -40°C to +85°C
		(No Prescaler)					
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_	—	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5V, -40°C to +85°C
34	Tıoz	I/O High Impedance from MCLR	—	_	100	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 16-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS VS. VDD



NOTES:



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Microchip Technology Inc. 2107 North First Street, Suite 590 San Jose, CA 95131 Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108 Mississauga, Ontario L4V 1X5, Canada Tel: 905-673-0699 Fax: 905-673-6509

#### ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd Suite 22, 41 Rawson Street Epping 2121, NSW Australia

Tel: 61-2-9868-6733 Fax: 61-2-9868-6755 China - Beijing

Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office Unit 915 Bei Hai Wan Tai Bldg. No. 6 Chaoyangmen Beidajie Beijing, 100027, No. China Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office Rm. 2401, 24th Floor, Ming Xing Financial Tower No. 88 TIDU Street Chengdu 610016, China Tel: 86-28-6766200 Fax: 86-28-6766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office Unit 28F, World Trade Plaza No. 71 Wusi Road Fuzhou 350001, China Tel: 86-591-7503506 Fax: 86-591-7503521 China - Shanghai

Microchip Technology Consulting (Shanghai) Co., Ltd. Room 701, Bldg. B Far East International Plaza No. 317 Xian Xia Road Shanghai, 200051 Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

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Microchip Technology Inc. India Liaison Office **Divvasree Chambers** 1 Floor, Wing A (A3/A4) No. 11, O'Shaugnessey Road Bangalore, 560 025, India Tel: 91-80-2290061 Fax: 91-80-2290062

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Microchip Technology Japan K.K. Benex S-1 6F 3-18-20, Shinyokohama Kohoku-Ku, Yokohama-shi Kanagawa, 222-0033, Japan Tel: 81-45-471- 6166 Fax: 81-45-471-6122 Korea Microchip Technology Korea 168-1, Youngbo Bldg. 3 Floor Samsung-Dong, Kangnam-Ku Seoul, Korea 135-882 Tel: 82-2-554-7200 Fax: 82-2-558-5934 Singapore Microchip Technology Singapore Pte Ltd. 200 Middle Road #07-02 Prime Centre Singapore, 188980 Tel: 65-334-8870 Fax: 65-334-8850 Taiwan Microchip Technology Taiwan 11F-3, No. 207 Tung Hua North Road Taipei, 105, Taiwan Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

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