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Applications of "<u>Embedded - Microcontrollers</u>"

Dataila	
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-20-p

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C71X device.

Device	Program Memory	Data Memory		
PIC16C710	512 x 14	36 x 8		
PIC16C71	1K x 14	36 x 8		
PIC16C711	1K x 14	68 x 8		
PIC16C715	2K x 14	128 x 8		

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow bit and a digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. The special function registers can be classified into two sets (core and peripheral). Those registers associated with the "core" functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: PIC16C710/71/711 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (1)
Bank 0											
00h ⁽³⁾	INDF	Addressing	this location	uses conter	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
01h	TMR0	Timer0 mod	lule's registe	r						xxxx xxxx	uuuu uuuu
02h ⁽³⁾	PCL	Program Co	ounter's (PC)	Least Signif	ficant Byte					0000 0000	0000 0000
03h ⁽³⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h ⁽³⁾	FSR	Indirect data	a memory ac	Idress pointe	er					xxxx xxxx	uuuu uuuu
05h	PORTA	_	_	_	PORTA Dat	a Latch whe	n written: PO	RTA pins wh	en read	x 0000	u 0000
06h	PORTB	PORTB Dat	a Latch whe	n written: PC	RTB pins wl	nen read				xxxx xxxx	uuuu uuuu
07h	_	Unimpleme	nted							_	_
08h	ADCON0	ADCS1	ADCS0	(6)	CHS1	CHS0	GO/DONE	ADIF	ADON	00-0 0000	00-0 0000
09h ⁽³⁾	ADRES	A/D Result	Register							xxxx xxxx	uuuu uuuu
0Ah ^(2,3)	PCLATH	_	_	_	Write Buffer	for the uppe	er 5 bits of the	e Program C	ounter	0 0000	0 0000
0Bh ⁽³⁾	INTCON	GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h ⁽³⁾	INDF	Addressing	this location	uses conter	ts of FSR to	address data	a memory (n	ot a physical	register)	0000 0000	0000 0000
81h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽³⁾	PCL	Program Co	ounter's (PC)	Least Signif	ficant Byte					0000 0000	0000 0000
83h ⁽³⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h ⁽³⁾	FSR	Indirect data	a memory ac	ldress pointe	er					xxxx xxxx	uuuu uuuu
85h	TRISA	_	_	_	PORTA Dat	a Direction F	Register			1 1111	1 1111
86h	TRISB	PORTB Dat	a Direction (Control Regis	ster					1111 1111	1111 1111
87h ⁽⁴⁾	PCON	_	_	_	_	_	_	POR	BOR	qq	uu
88h	ADCON1	_	_	_	_	_	_	PCFG1	PCFG0	00	00
89h ⁽³⁾	ADRES	A/D Result	A/D Result Register								uuuu uuuu
8Ah(2,3)	PCLATH	_	_	_	Write Buffer	for the uppe	er 5 bits of the	e Program C	ounter	0 0000	0 0000
8Bh ⁽³⁾	INTCON	GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

- Note 1: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.
 - 2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
 - 3: These registers can be addressed from either bank.
 - 4: The PCON register is not physically implemented in the PIC16C71, read as '0'.
 - 5: The IRP and RP1 bits are reserved on the PIC16C710/71/711, always maintain these bits clear.
 - 6: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

7.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-5. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), Figure 7-5. The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is $10~\text{k}\Omega$. After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

EQUATION 7-1: A/D MINIMUM CHARGING TIME

 $VHOLD = (VREF - (VREF/512)) \bullet (1 - e^{(-TCAP/CHOLD(RIC + RSS + RS))})$

Given: VHOLD = (VREF/512), for 1/2 LSb resolution

The above equation reduces to:

 $TCAP = -(51.2 pF)(1 k\Omega + Rss + Rs) ln(1/511)$

Example 7-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

 $Rs = 10 k\Omega$

1/2 LSb error

 $\text{Vdd} = 5\text{V} \rightarrow \text{Rss} = 7 \text{ k}\Omega$

Temp (application system max.) = 50°C

VHOLD = 0 @ t = 0

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 7-1: CALCULATING THE MINIMUM REQUIRED AQUISITION TIME

TACQ = Amplifier Settling Time +

Holding Capacitor Charging Time +

Temperature Coefficient

TACQ = $5 \mu s + TCAP + [(Temp - 25°C)(0.05 \mu s/°C)]$

TCAP = -CHOLD (Ric + Rss + Rs) In(1/511)

-51.2 pF (1 kΩ + 7 kΩ + 10 kΩ) ln(0.0020)

-51.2 pF (18 k Ω) ln(0.0020)

-0.921 μs (-6.2364)

 $5.747 \mu s$

TACQ = $5 \mu s + 5.747 \mu s + [(50^{\circ}C - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$

 $10.747 \,\mu s + 1.25 \,\mu s$

 $11.997 \mu s$

FIGURE 7-5: ANALOG INPUT MODEL

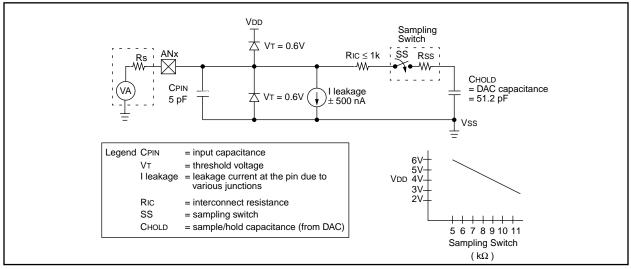


TABLE 8-3: CERAMIC RESONATORS, PIC16C710/711/715

Ranges Tested:								
Mode	Freq	OSC2						
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF					
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF					
	se values are to set at bottom of p	or design guidar page.	nce only. See					
Resonato	rs Used:							
455 kHz	Panasonic E	FO-A455K04B	± 0.3%					
2.0 MHz	Murata Erie	CSA2.00MG	± 0.5%					
4.0 MHz	Murata Erie CSA4.00MG ± 0.5%							
8.0 MHz	Murata Erie CSA8.00MT ± 0.5%							
16.0 MHz	16.0 MHz Murata Erie CSA16.00MX ± 0.5%							
All reso	All resonators used did not have built-in capacitors.							

TABLE 8-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16C710/711/715

Osc Type	Crystal Cap. Range Freq C1		Cap. Range C2		
LP	32 kHz	33 pF	33 pF		
	200 kHz	15 pF	15 pF		
XT	200 kHz	47-68 pF	47-68 pF		
	1 MHz	15 pF	15 pF		
	4 MHz	15 pF	15 pF		
HS	4 MHz	15 pF	15 pF		
	8 MHz	15-33 pF	15-33 pF		
	20 MHz	15-33 pF	15-33 pF		
These	values are	for design guida	nce only. See		
notes a	at bottom of	page.			
	Crys	tals Used			
32 kHz	Epson C-00	01R32.768K-A	± 20 PPM		
200 kHz	STD XTL 2	STD XTL 200.000KHz			
1 MHz	ECS ECS-	± 50 PPM			
4 MHz	ECS ECS-4	± 50 PPM			
8 MHz	EPSON CA	-301 8.000M-C	± 30 PPM		
20 MHz	EPSON CA	A-301 20.000M-C	± 30 PPM		

- Note 1: Recommended values of C1 and C2 are identical to the ranges tested table.
 - 2: Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

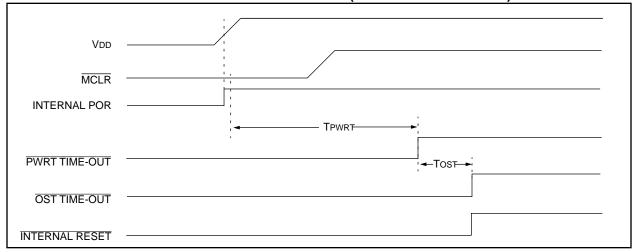


FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

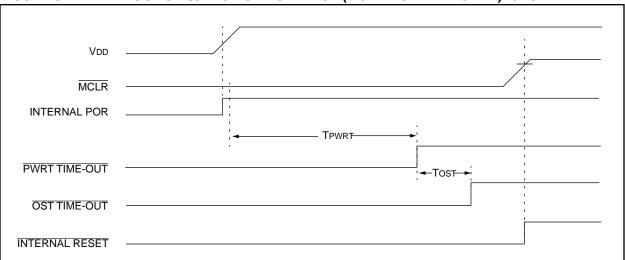


FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

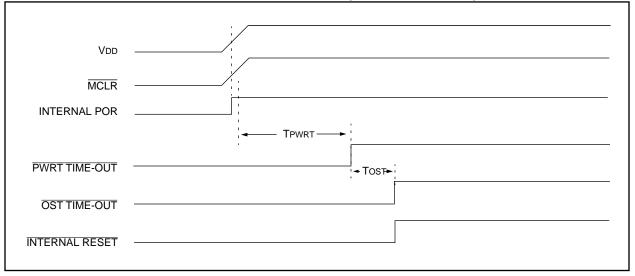


FIGURE 8-17: INTERRUPT LOGIC, PIC16C710, 71, 711

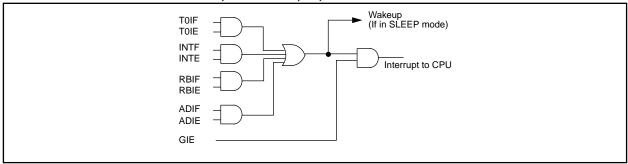
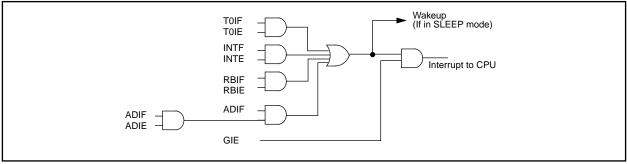


FIGURE 8-18: INTERRUPT LOGIC, PIC16C715



8.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (STATUS<3>) is cleared, the \overline{TO} (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or Vss, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

8.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. External reset input on MCLR pin.
- Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External \overline{MCLR} Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The \overline{TO} and \overline{PD} bits in the STATUS register can be used to determine the cause of device reset. The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. A/D conversion (when A/D clock source is RC).

Other peripherals cannot generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

8.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

CLRF	Clear f								
Syntax:	[label] C	[label] CLRF f							
Operands:	$0 \le f \le 12$	$0 \le f \le 127$							
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$								
Status Affected:	Z								
Encoding:	00 0001 lfff ffff								
Description:	The contents of register 'f' are cleared and the Z bit is set.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write register 'f'					
Example	CLRF	FLAC	E_REG						
	Before In	struction FLAG_RE		0x5A					
	After Inst	ruction							

FLAG_REG = 0x00

CLRW	Clear W					
Syntax:	[label]	CLRW				
Operands:	None					
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$					
Status Affected:	Z					
Encoding:	00	0001	0xxx	xxxx		
Description:	W register set.	is cleare	d. Zero bit	(Z) is		
Words:	1					
Cycles:	1					
Q Cycle Activity:	Q1	Q2	Q3	Q4		
	Decode	NOP	Process data	Write to W		
Example	CLRW					
	Before Instruction					
	W = 0x5A After Instruction					
		W = Z =	0x00 1			

CLRWDT	Clear Wa	tchdog	Timer					
Syntax:	[label] CLRWDT							
Operands:	None							
Operation:	00h → WDT 0 → WDT prescaler, 1 → \overline{TO} 1 → \overline{PD}							
Status Affected:	\overline{TO} , \overline{PD}							
Encoding:	00	0000	0110	0100				
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	NOP	Process data	Clear WDT Counter				
Example	CLRWDT							
	Before Instruction WDT counter = ? After Instruction							
	WDT counter = 0x00							
		WDT pres	scaler= =	0				
		PD	=	1				

SLEEP

Syntax: [label] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$,

 $0 \to WDT \ prescaler,$

 $1 \to \overline{TO}, \\ 0 \to \overline{PD}$

Status Affected: TO, PD

Encoding: 00 0000 0110 0011

Description: The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is

set. Watchdog Timer and its pres-

caler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See Section 8.8 for more details.

Words: 1 Cycles: 1

Q Cycle Activity: Q1 Q2 Q3 Q4

Decode NOP NOP Go to Sleep

Example: SLEEP

SUBLW Subtract W from Literal

Syntax: [label] SUBLW k

 $\label{eq:continuous} \begin{array}{ll} \text{Operands:} & 0 \leq k \leq 255 \\ \\ \text{Operation:} & k \text{-} (W) \rightarrow (W) \end{array}$

Status Affected: C, DC, Z

Encoding: 11 110x kkkk kkkk

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'.

The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity: Q1 Q2 Q3 Q4

Decode Read Process Write to W

Example 1: SUBLW 0x02

Before Instruction

W = 1 C = ? Z = ?

After Instruction

W = 1

C = 1; result is positive

Z = 0

Example 2: Before Instruction

W = 2 C = ?

After Instruction

W = 0

C = 1; result is zero

Z = 1

Example 3: Before Instruction

W = 3 C = ? Z = ?

After Instruction

W = 0xFF

C = 0; result is nega-

tive

Z = 0

11.0 ELECTRICAL CHARACTERISTICS FOR PIC16C710 AND PIC16C711

Absolute Maximum Ratings †

Austication	55 to 1405°O
Ambient temperature under bias	
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3 to +7.5V
Voltage on MCLR with respect to Vss	
Voltage on RA4 with respect to Vss	0 to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, lik (Vi < 0 or Vi > VDD)	± 20 mA
Output clamp current, lok (Vo < 0 or Vo > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA	200 mA
Maximum current sourced by PORTA	200 mA
Maximum current sunk by PORTB	200 mA
Maximum current sourced by PORTB	200 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD -	VOH) x IOH} + Σ (VOI x IOL)

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

osc	PIC16C710-04 PIC16C711-04	PIC16C710-10 PIC16C711-10	PIC16C710-20 PIC16C711-20	PIC16LC710-04 PIC16LC711-04	PIC16C710/JW PIC16C711/JW
	VDD: 4.0V to 6.0V	VDD: 4.5V to 5.5V	VDD: 4.5V to 5.5V	VDD: 2.5V to 6.0V	VDD: 4.0V to 6.0V
RC	IDD: 5 mA max. at 5.5V	IDD: 2.7 mA typ. at 5.5V	IDD: 2.7 mA typ. at 5.5V	IDD: 3.8 mA typ. at 3.0V	IDD: 5 mA max. at 5.5V
	IPD: 21 μA max. at 4V	IPD: 1.5 μA typ. at 4V	IPD: 1.5 μA typ. at 4V	IPD: 5.0 μA typ. at 3V	IPD: 21 μA max. at 4V
	Freq:4 MHz max.	Freq: 4 MHz max.	Freq: 4 MHz max.	Freq: 4 MHz max.	Freq:4 MHz max.
	VDD: 4.0V to 6.0V	VDD: 4.5V to 5.5V	VDD: 4.5V to 5.5V	VDD: 2.5V to 6.0V	VDD: 4.0V to 6.0V
XT	IDD: 5 mA max. at 5.5V	IDD: 2.7 mA typ. at 5.5V	IDD: 2.7 mA typ. at 5.5V	IDD: 3.8 mA typ. at 3.0V	IDD: 5 mA max. at 5.5V
	IPD: 21 μA max. at 4V	IPD: 1.5 μA typ. at 4V	IPD: 1.5 μA typ. at 4V	IPD: 5.0 μA typ. at 3V	IPD: 21 μA max. at 4V
	Freq: 4 MHz max.	Freq: 4 MHz max.			
	VDD: 4.5V to 5.5V	VDD: 4.5V to 5.5V	VDD: 4.5V to 5.5V		VDD: 4.5V to 5.5V
	IDD: 13.5 mA typ. at	IDD: 30 mA max. at	IDD: 30 mA max. at	Not recommended for	IDD: 30 mA max. at
HS	5.5V	5.5V	5.5V	use in HS mode	5.5V
	IPD: 1.5 μA typ. at 4.5V	IPD: 1.5 μA typ. at 4.5V	IPD: 1.5 μA typ. at 4.5V	use iii i is iiiode	IPD: 1.5 μA typ. at 4.5V
	Freq: 4 MHz max.	Freq: 10 MHz max.	Freq:20 MHz max.		Freq: 10 MHz max.
	VDD: 4.0V to 6.0V			VDD: 2.5V to 6.0V	VDD: 2.5V to 6.0V
	IDD: 52.5 μA typ. at			IDD: 48 μA max. at	IDD: 48 μA max. at
LP	32 kHz, 4.0V	Not recommended for	Not recommended for	32 kHz, 3.0V	32 kHz, 3.0V
-	IPD: 0.9 μA typ. at 4.0V	use in LP mode	use in LP mode	IPD: 5.0 μA max. at 3.0V	IPD: 5.0 μA max. at
	Freq: 200 kHz max.			Freq: 200 kHz max.	3.0V
					Freq: 200 kHz max.

FIGURE 12-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

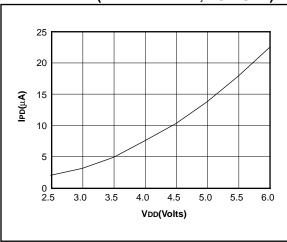


FIGURE 12-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

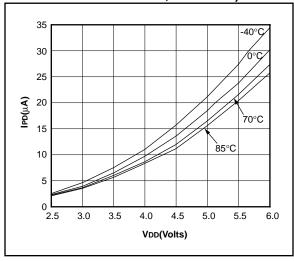


FIGURE 12-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

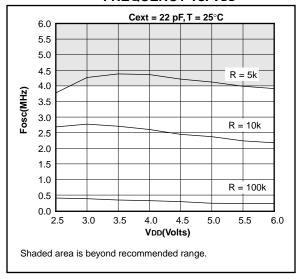


FIGURE 12-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

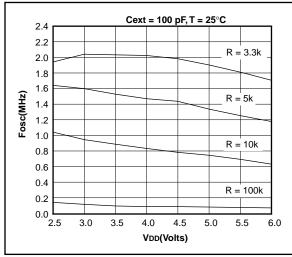


FIGURE 12-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

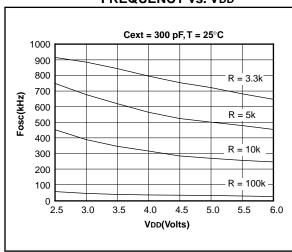


FIGURE 12-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)

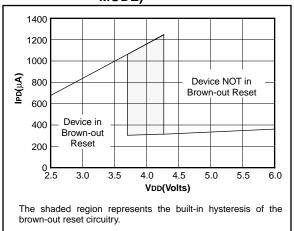


FIGURE 12-9: MAXIMUM IPD vs. VDD
BROWN-OUT DETECT
ENABLED
(85°C TO -40°C, RC MODE)

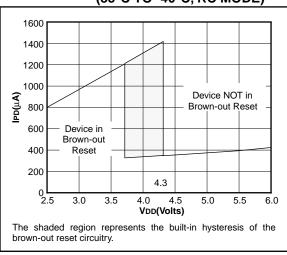


FIGURE 12-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

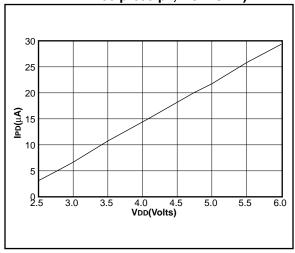


FIGURE 12-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

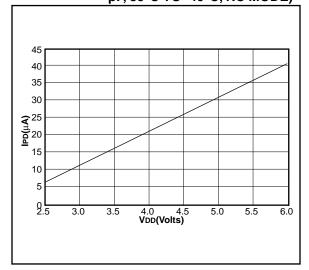
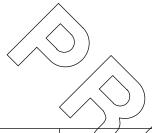


TABLE 13-1: **Applicable Devices** | 710 | 71 | 711 | 715

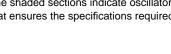
CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)



				(
osc		PIC16C715-04	ļ ·	PIC16C7/15-10		PIC16C715-20		PIC16LC715-04		PIC16C715/JW
	VDD:	4.0V to 5.5V	VDD:	4.5V to 5.5V	VDD:	4.5V to 5.5V	VDD:	2.5V to 5.5V	VDD:	4.0V to 5.5V
RC	IDD:	5 mA max. at 5.5V	IDD:	2.7 mA typ. at \$.5)	IDD:	2.7 mA typ. at 5.5V	IDD:	2.0 mA typ. at 3.0V	IDD:	5 mA max. at 5.5V
INC.	IPD:	21 μA max. at 4V	IPD:	1.5 μA typ. at 4V	IPD:	1.5 μA typ. at 4V	IPD:	0.9 μA typ. at 3V	IPD:	21 μA max. at 4V
	Freq:	4 MHz max.	Freq:	4 MHz max.	Freq:	4 MHz max.	Freq:	4 MHz max.	Freq:	4 MHz max.
	VDD:	4.0V to 5.5V	VDD:	4.5V to 5.5V /	VDD:	4.5V to 5.5V	VDD:	2.5V to 5.5V	VDD:	4.0V to 5.5V
XT	IDD:	5 mA max. at 5.5V	IDD:	2.7 mA typ. at 5.5V	IDD:	2.7 mA typ. at 5.5V	IDD:	2.0 mA typ. at 3.0V	IDD:	5 mA max. at 5.5V
^1	IPD:	21 μA max. at 4V	IPD:	1.5 μA typ. at 4V \	NPD:	1.5 μA typ at 4V	IPD:	0.9 μA typ. at 3V	IPD:	21 μA max. at 4V
	Freq:	4 MHz max.	Freq:	4 MHz max.	Freg.	4 MHz max,	Freq:	4 MHz max.	Freq:	4 MHz max.
	VDD:	4.5V to 5.5V	VDD:	4.5V to 5.5V	V&p:	4.51/to 5/5V/			VDD:	4.5V to 5.5V
HS	IDD:	13.5 mA typ. at 5.5V	IDD:	30 mA max. at 5.5V	IDD:	30 m/k max. at 5.5V	00.00	t use in HS mode	IDD:	30 mA max. at 5.5V
ПЭ	IPD:	1.5 μA typ. at 4.5V	IPD:	1.5 μA typ. at 4.5V	IPD:	1.5 μA typ. at 4.5V		it use in no mode	IPD:	1.5 μA typ. at 4.5V
	Freq:	4 MHz max.	Freq:	10 MHz max.	Freq:	20 MHz max.	/ >		Freq:	10 MHz max.
	VDD:	4.0V to 5.5V					YOD:	2:5V to 5.5V	VDD:	2.5V to 5.5V
IP	IDD:	52.5 μA typ. at 32 kHz, 4.0V	Do no	t use in LP mode	Dono	ot use in LP mode	IDD;/	48 μA max. at 32 kHz, 3.0V	IDD:	48 μA max. at 32 kHz, 3.0V
	IPD:	0.9 μA typ. at 4.0V	סוו טע	use iii Lr iiilode	סוו טם	it use iii LF 11100e	IPO: /	∕15.0 μA max. at 3.0V	IPD:	5.0 μA max. at 3.0V
	Freq:	200 kHz max.					1/ /	/ 200 kHz max.	Freq:	200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type

that ensures the specifications required.



13.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS

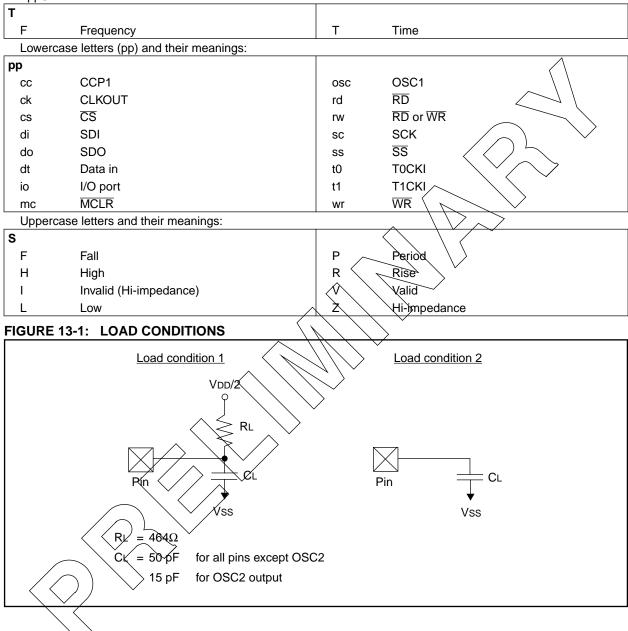


FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

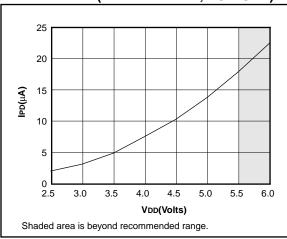


FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

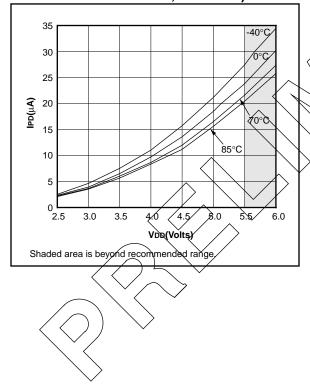


FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

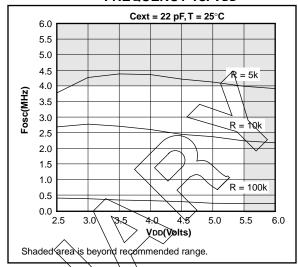


FIGURE 14-6: TYPICAL RC OSCILLATOR
FREQUENCY vs. VDD

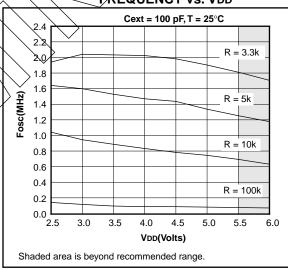


FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

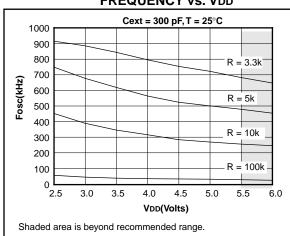


FIGURE 14-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

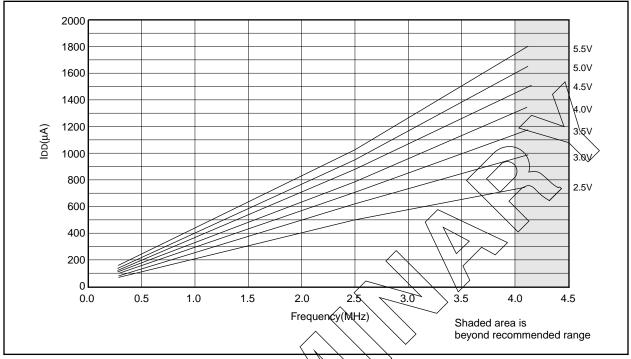


FIGURE 14-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)

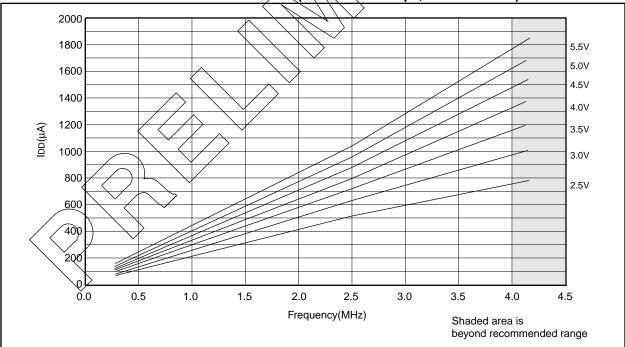


FIGURE 16-21: IOL VS. VOL, VDD = 3V

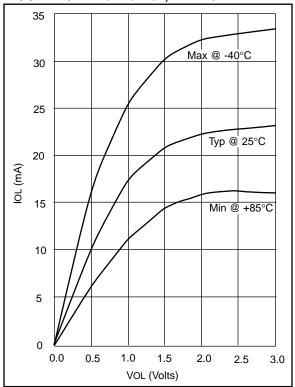
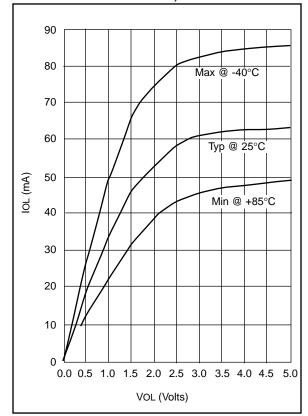


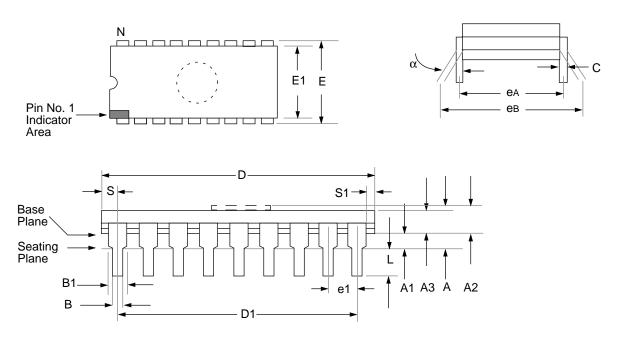
FIGURE 16-22: IOL VS. VOL, VDD = 5V



Data based on matrix samples. See first page of this section for details.

17.0 PACKAGING INFORMATION

17.1 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)



Package Group: Ceramic CERDIP Dual In-Line (CDP)									
	Millimeters Inches								
Symbol	Min	Max	Notes	Min	Max	Notes			
α	0°	10°		0°	10°				
Α	_	5.080		_	0.200				
A1	0.381	1.7780		0.015	0.070				
A2	3.810	4.699		0.150	0.185				
А3	3.810	4.445		0.150	0.175				
В	0.355	0.585		0.014	0.023				
B1	1.270	1.651	Typical	0.050	0.065	Typical			
С	0.203	0.381	Typical	0.008	0.015	Typical			
D	22.352	23.622		0.880	0.930				
D1	20.320	20.320	Reference	0.800	0.800	Reference			
E	7.620	8.382		0.300	0.330				
E1	5.588	7.874		0.220	0.310				
e1	2.540	2.540	Reference	0.100	0.100	Reference			
eA	7.366	8.128	Typical	0.290	0.320	Typical			
eB	7.620	10.160		0.300	0.400				
L	3.175	3.810		0.125	0.150				
N	18	18		18	18				
S	0.508	1.397		0.020	0.055				
S1	0.381	1.270		0.015	0.050				

RB7:RB4 Port Pins28 INDEX Timer031 Timer0/WDT Prescaler34 Α Watchdog Timer65 A/D BODEN bit48 Accuracy/Error44 ADIF bit39 Brown-out Reset (BOR)53 Analog Input Model Block Diagram40 Analog-to-Digital Converter37 Configuring Analog Port Pins41 Configuring the Interrupt39 C16C71 47 Configuring the Module39 Carry bit7 Connection Considerations44 Conversion Clock41 CHS1 bit37 Conversion Time43 Clocking Scheme10 Conversions42 Code Examples Call of a Subroutine in Page 1 from Page 024 Delays40 Changing Prescaler (Timer0 to WDT)35 Effects of a Reset44 Changing Prescaler (WDT to Timer0)35 Equations40 Doing an A/D Conversion42 Faster Conversion - Lower Resolution Trade-off 43 I/O Programming30 Flowchart of A/D Operation45 Indirect Addressing24 Initializing PORTA25 Internal Sampling Switch (Rss) Impedence40 Initializing PORTB27 Minimum Charging Time40 Saving STATUS and W Registers in RAM64 Operation During Sleep44 Sampling Requirements40 Computed GOTO23 Source Impedence40 Configuration Bits47 Time Delays40 Transfer Function45 CP1 bit48 Absolute Maximum Ratings89, 111, 135 **AC Characteristics** PIC16C710101 DC bit17 PIC16C711101 DC Characteristics 147 ADCON0 Register37 PIC16C710 90, 101 ADCON137 PIC16C711 90, 101 ADCON1 Register14, 37 PIC16C715 113, 125 ADCS0 bit37 Development Tools85 Diagrams - See Block Diagrams ADIF bit21, 37 Digit Carry bit7 Direct Addressing24 ADRES Register 15, 37, 39 Ε ALU7 Application Notes **Electrical Characteristics** AN55227 PIC16C71089 PIC16C71189 AN607, Power-up Trouble Shooting53 PIC16C715 111 External Brown-out Protection Circuit60 Architecture Harvard7 External Power-on Reset Circuit60 Overview 7 F von Neumann7 Family of Devices MPASM Assembler86 PIC16C71X4 В **Block Diagrams** FSR Register 15, 16, 24 Analog Input Model40 Fuzzy Logic Dev. System (fuzzyTECH®-MP)87 PIC16C71X8 RA4/T0CKI Pin25 RB3:RB0 Port Pins27 GO/DONE bit37

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