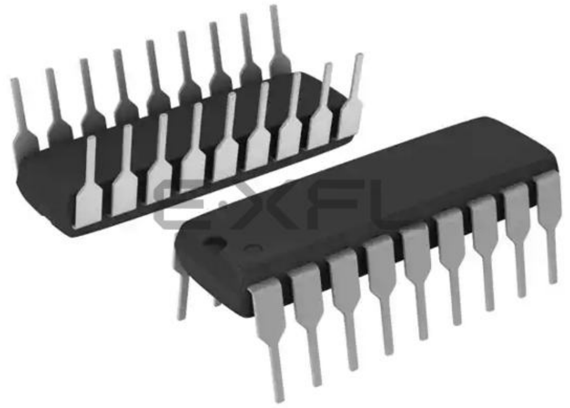





## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 13 |
| Program Memory Size | 896B (512 x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 36 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 6V |
| Data Converters | A/D 4x8b |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 18-DIP (0.300", 7.62mm) |
| Supplier Device Package | 18-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-20-p |

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C71X device.

| Device | Program Memory | Data Memory |
|---|---|---|
| PIC16C710 | 512 x 14 | 36 x 8 |
| PIC16C71 | 1K x 14 | 36 x 8 |
| PIC16C711 | 1K x 14 | 68 x 8 |
| PIC16C715 | 2K x 14 | 128 x 8 |

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ bit and a $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). Those registers associated with the “core” functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

**TABLE 4-1: PIC16C710/71/711 SPECIAL FUNCTION REGISTER SUMMARY**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 0** | | | | | | | | | | | |
| 00h(3) | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 01h | TMR0 | Timer0 module’s register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 02h(3) | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 03h(3) | STATUS | IRP(5) | RP1(5) | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 000q quuu |
| 04h(3) | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 05h | PORTA | — | — | — | PORTA Data Latch when written: PORTA pins when read | | | | | ---x 0000 | ---u 0000 |
| 06h | PORTB | PORTB Data Latch when written: PORTB pins when read | | | | | | | | xxxx xxxx | uuuu uuuu |
| 07h | — | Unimplemented | | | | | | | | — | — |
| 08h | ADCON0 | ADCS1 | ADCS0 | **(6)** | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADIF | ADON | 00-0 0000 | 00-0 0000 |
| 09h(3) | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Ah(2,3) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | ---0 0000 |
| 0Bh(3) | INTCON | GIE | ADIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| **Bank 1** | | | | | | | | | | | |
| 80h(3) | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 81h | OPTION | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 82h(3) | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 83h(3) | STATUS | IRP(5) | RP1(5) | RP0 | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C | 0001 1xxx | 000q quuu |
| 84h(3) | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 85h | TRISA | — | — | — | PORTA Data Direction Register | | | | | ---1 1111 | ---1 1111 |
| 86h | TRISB | PORTB Data Direction Control Register | | | | | | | | 1111 1111 | 1111 1111 |
| 87h(4) | PCON | — | — | — | — | — | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | ---- --qq | ---- --uu |
| 88h | ADCON1 | — | — | — | — | — | — | PCFG1 | PCFG0 | ---- --00 | ---- --00 |
| 89h(3) | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 8Ah(2,3) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | ---0 0000 |
| 8Bh(3) | INTCON | GIE | ADIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as ‘0’.

Note 1: Other (non power-up) resets include external reset through $\overline{\text{MCLR}}$ and Watchdog Timer Reset.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: These registers can be addressed from either bank.

4: The PCON register is not physically implemented in the PIC16C71, read as ’0’.

5: The IRP and RP1 bits are reserved on the PIC16C710/71/711, always maintain these bits clear.

6: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

## 7.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor ($C_{HOLD}$) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-5. The source impedance ($R_S$) and the internal sampling switch ($R_{SS}$) impedance directly affect the time required to charge the capacitor $C_{HOLD}$. The sampling switch ($R_{SS}$) impedance varies over the device voltage ($V_{DD}$), Figure 7-5. The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 10 kΩ**. After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

### EQUATION 7-1: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \bullet (1 - e^{(-T_{CAP}/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

Given: $V_{HOLD} = (V_{REF}/512)$, for 1/2 LSb resolution

The above equation reduces to:

$$T_{CAP} = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S)\ \ln(1/511)$$

Example 7-1 shows the calculation of the minimum required acquisition time $T_{ACQ}$. This calculation is based on the following system assumptions.

$C_{HOLD}$ = 51.2 pF

Rs = 10 kΩ

1/2 LSb error

$V_{DD}$ = 5V → Rss = 7 kΩ

Temp (application system max.) = 50°C

$V_{HOLD}$ = 0 @ t = 0

> **Note 1:** The reference voltage ($V_{REF}$) has no effect on the equation, since it cancels itself out.
>
> **Note 2:** The charge holding capacitor ($C_{HOLD}$) is not discharged after each conversion.
>
> **Note 3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
>
> **Note 4:** After a conversion has completed, a 2.0$T_{AD}$ delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

### EXAMPLE 7-1: CALCULATING THE MINIMUM REQUIRED AQUISITION TIME

$T_{ACQ}$ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient

$T_{ACQ}$ = 5 µs + $T_{CAP}$ + [(Temp - 25°C)(0.05 µs/°C)]

$T_{CAP}$ = $-C_{HOLD}$ ($R_{IC}$ + $R_{SS}$ + $R_S$) ln(1/511)

-51.2 pF (1 kΩ + 7 kΩ + 10 kΩ) ln(0.0020)

-51.2 pF (18 kΩ) ln(0.0020)

-0.921 µs (-6.2364)

5.747 µs

$T_{ACQ}$ = 5 µs + 5.747 µs + [(50°C - 25°C)(0.05 µs/°C)]

10.747 µs + 1.25 µs

11.997 µs

### FIGURE 7-5: ANALOG INPUT MODEL

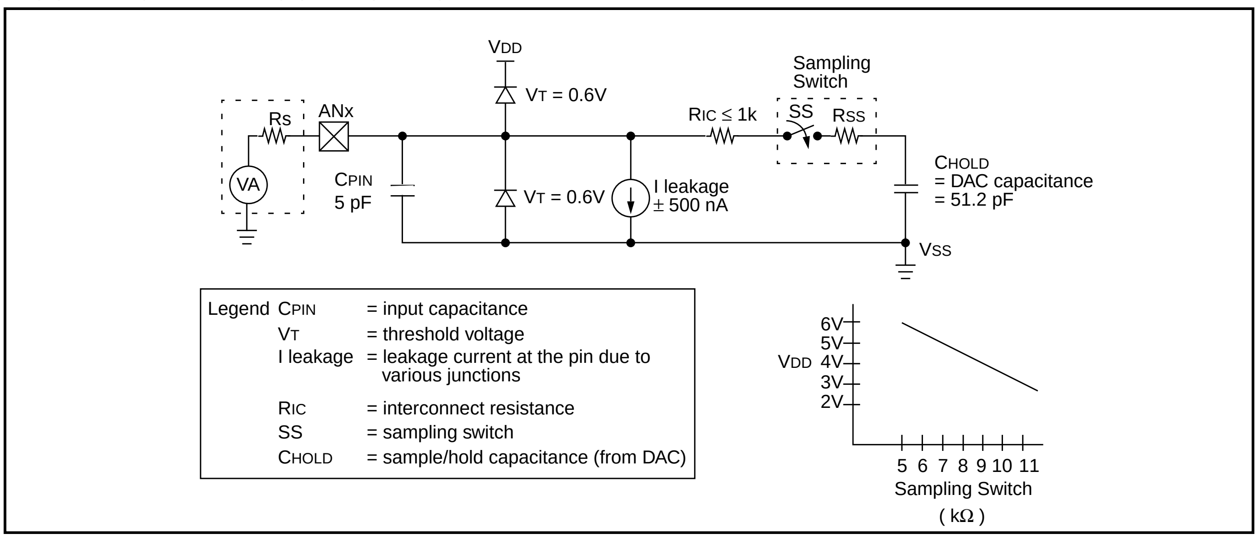


**TABLE 8-3: CERAMIC RESONATORS, PIC16C710/711/715**

| Ranges Tested: | | | |
|---|---|---|---|
| **Mode** | **Freq** | **OSC1** | **OSC2** |
| XT | 455 kHz<br>2.0 MHz<br>4.0 MHz | 68 - 100 pF<br>15 - 68 pF<br>15 - 68 pF | 68 - 100 pF<br>15 - 68 pF<br>15 - 68 pF |
| HS | 8.0 MHz<br>16.0 MHz | 10 - 68 pF<br>10 - 22 pF | 10 - 68 pF<br>10 - 22 pF |
| **These values are for design guidance only.** See notes at bottom of page. | | | |
| **Resonators Used:** | | | |
| 455 kHz | Panasonic EFO-A455K04B | ± 0.3% | |
| 2.0 MHz | Murata Erie CSA2.00MG | ± 0.5% | |
| 4.0 MHz | Murata Erie CSA4.00MG | ± 0.5% | |
| 8.0 MHz | Murata Erie CSA8.00MT | ± 0.5% | |
| 16.0 MHz | Murata Erie CSA16.00MX | ± 0.5% | |
| All resonators used did not have built-in capacitors. | | | |

**TABLE 8-4: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR, PIC16C710/711/715**

| Osc Type | Crystal Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15-33 pF | 15-33 pF |
| | 20 MHz | 15-33 pF | 15-33 pF |
| **These values are for design guidance only.** See notes at bottom of page. | | | |
| **Crystals Used** | | | |
| 32 kHz | Epson C-001R32.768K-A | ± 20 PPM | |
| 200 kHz | STD XTL 200.000KHz | ± 20 PPM | |
| 1 MHz | ECS ECS-10-13-1 | ± 50 PPM | |
| 4 MHz | ECS ECS-40-20-1 | ± 50 PPM | |
| 8 MHz | EPSON CA-301 8.000M-C | ± 30 PPM | |
| 20 MHz | EPSON CA-301 20.000M-C | ± 30 PPM | |

Note 1: Recommended values of C1 and C2 are identical to the ranges tested table.
2: Higher capacitance increases the stability of oscillator but also increases the start-up time.
3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

**FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1**

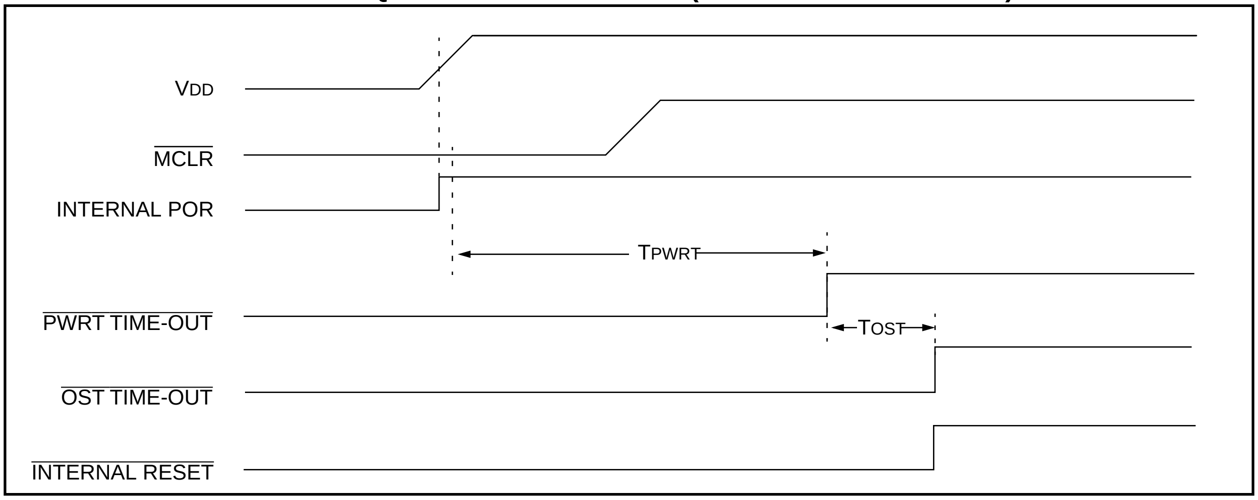



**FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2**

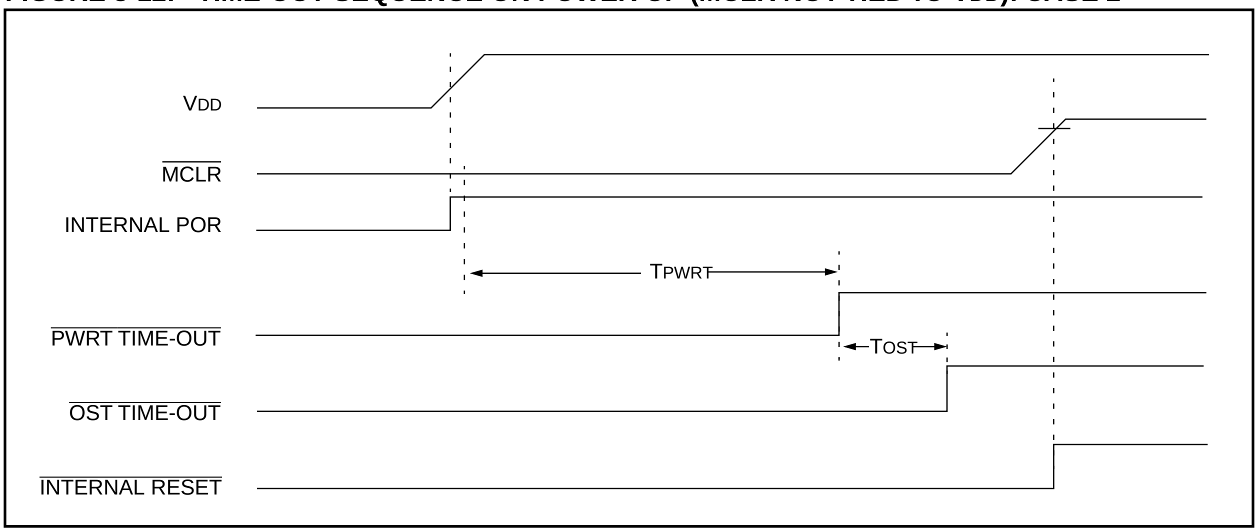



**FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)**

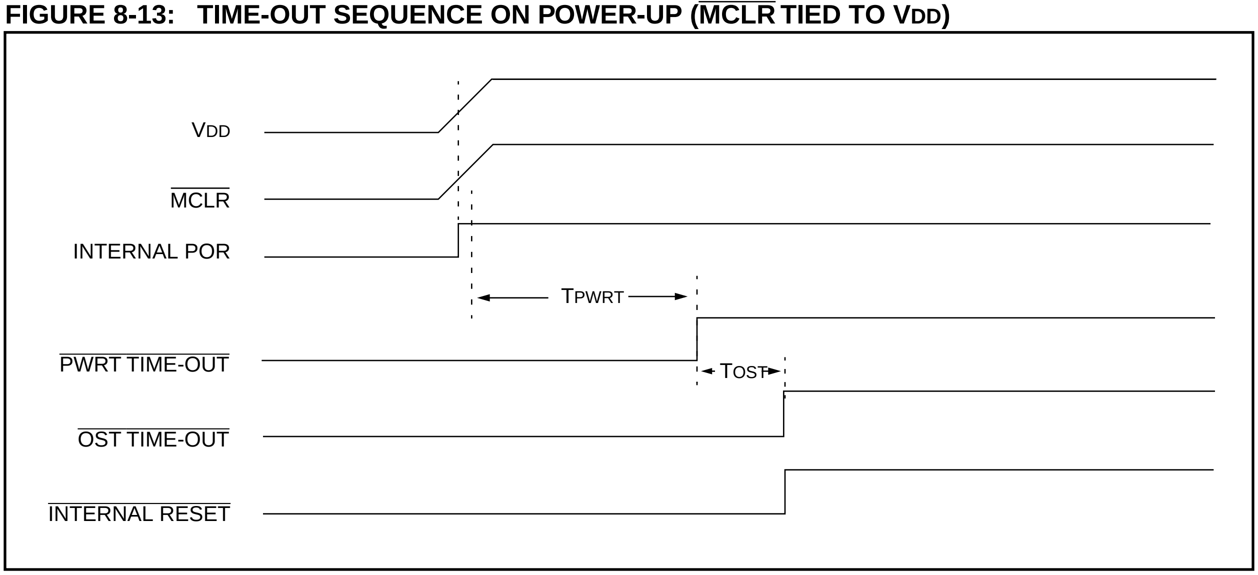


**FIGURE 8-17: INTERRUPT LOGIC, PIC16C710, 71, 711**

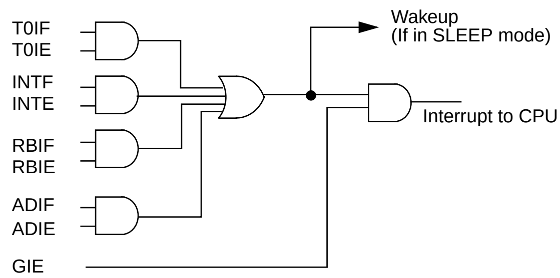
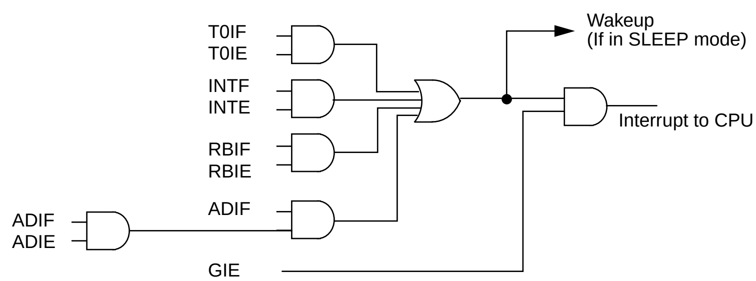



**FIGURE 8-18: INTERRUPT LOGIC, PIC16C715**



## 8.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either $V_{DD}$, or $V_{SS}$, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at $V_{DD}$ or $V_{SS}$ for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level ($V_{IHMC}$).

### 8.8.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External $\overline{MCLR}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. A/D conversion (when A/D clock source is RC).

Other peripherals cannot generate interrupts since during SLEEP, no on-chip Q clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

### 8.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep . The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

### CLRF — Clear f

| | |
|---|---|
| Syntax: | [*label*] CLRF f |
| Operands: | 0 ≤ f ≤ 127 |
| Operation: | 00h → (f)<br>1 → Z |
| Status Affected: | Z |
| Encoding: | `00` `0001` `1fff` `ffff` |
| Description: | The contents of register 'f' are cleared and the Z bit is set. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write register 'f' |

Example `CLRF FLAG_REG`

Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

### CLRW — Clear W

| | |
|---|---|
| Syntax: | [ *label* ] CLRW |
| Operands: | None |
| Operation: | 00h → (W)<br>1 → Z |
| Status Affected: | Z |
| Encoding: | `00` `0001` `0xxx` `xxxx` |
| Description: | W register is cleared. Zero bit (Z) is set. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | Process data | Write to W |

Example `CLRW`

Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

### CLRWDT — Clear Watchdog Timer

| | |
|---|---|
| Syntax: | [ *label* ] CLRWDT |
| Operands: | None |
| Operation: | 00h → WDT<br>0 → WDT prescaler,<br>1 → $\overline{TO}$<br>1 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Encoding: | `00` `0000` `0110` `0100` |
| Description: | `CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | Process data | Clear WDT Counter |

Example `CLRWDT`

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

### SLEEP

| | |
|---|---|
| Syntax: | [ *label* ] SLEEP |
| Operands: | None |
| Operation: | 00h → WDT,<br>0 → WDT prescaler,<br>1 → $\overline{TO}$,<br>0 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Encoding: | `00` `0000` `0110` `0011` |
| Description: | The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.<br>The processor is put into SLEEP mode with the oscillator stopped. See Section 8.8 for more details. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | NOP | Go to Sleep |

Example: SLEEP

### SUBLW — Subtract W from Literal

| | |
|---|---|
| Syntax: | [ *label* ] SUBLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | k - (W) → (W) |
| Status Affected: | C, DC, Z |
| Encoding: | `11` `110x` `kkkk` `kkkk` |
| Description: | The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register. |
| Words: | 1 |
| Cycles: | 1 |

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Process data | Write to W |

Example 1: `SUBLW 0x02`

Before Instruction

W = 1
C = ?
Z = ?

After Instruction

W = 1
C = 1; result is positive
Z = 0

Example 2: Before Instruction

W = 2
C = ?
Z = ?

After Instruction

W = 0
C = 1; result is zero
Z = 1

Example 3: Before Instruction

W = 3
C = ?
Z = ?

After Instruction

W = 0xFF
C = 0; result is negative
Z = 0

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

## 11.0 ELECTRICAL CHARACTERISTICS FOR PIC16C710 AND PIC16C711

**Absolute Maximum Ratings †**

Ambient temperature under bias........ -55 to +125˚C
Storage temperature........ -65˚C to +150˚C
Voltage on any pin with respect to VSS (except VDD, $\overline{\text{MCLR}}$, and RA4)........ -0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS........ -0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS........ 0 to +14V
Voltage on RA4 with respect to Vss........ 0 to +14V
Total power dissipation (Note 1)........ 1.0W
Maximum current out of VSS pin........ 300 mA
Maximum current into VDD pin........ 250 mA
Input clamp current, IIK (VI < 0 or VI > VDD)........ ± 20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)........ ± 20 mA
Maximum output current sunk by any I/O pin........ 25 mA
Maximum output current sourced by any I/O pin........ 25 mA
Maximum current sunk by PORTA........ 200 mA
Maximum current sourced by PORTA........ 200 mA
Maximum current sunk by PORTB........ 200 mA
Maximum current sourced by PORTB........ 200 mA

**Note 1:** Power dissipation is calculated as follows: Pdis = $V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC16C710-04<br>PIC16C711-04 | PIC16C710-10<br>PIC16C711-10 | PIC16C710-20<br>PIC16C711-20 | PIC16LC710-04<br>PIC16LC711-04 | PIC16C710/JW<br>PIC16C711/JW |
|---|---|---|---|---|---|
| RC | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq:4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 3.8 mA typ. at 3.0V<br>IPD: 5.0 µA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq:4 MHz max. |
| XT | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 6.0V<br>IDD: 3.8 mA typ. at 3.0V<br>IPD: 5.0 µA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 6.0V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V<br>IDD: 13.5 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq:20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. |
| LP | VDD: 4.0V to 6.0V<br>IDD: 52.5 µA typ. at 32 kHz, 4.0V<br>IPD: 0.9 µA typ. at 4.0V<br>Freq: 200 kHz max. | Not recommended for use in LP mode | Not recommended for use in LP mode | VDD: 2.5V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. | VDD: 2.5V to 6.0V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. |

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 12-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)**

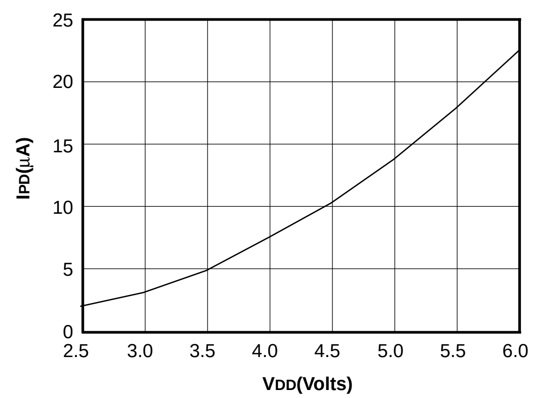



**FIGURE 12-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)**

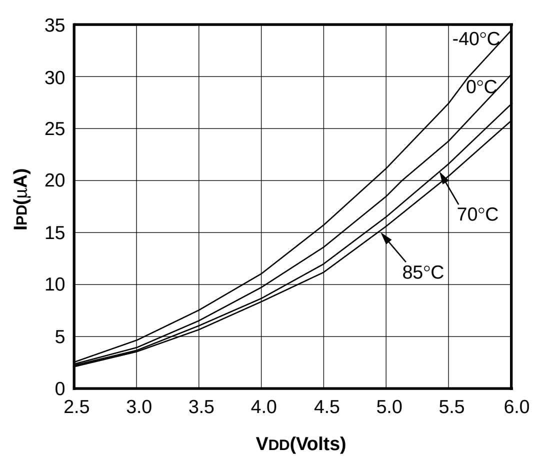
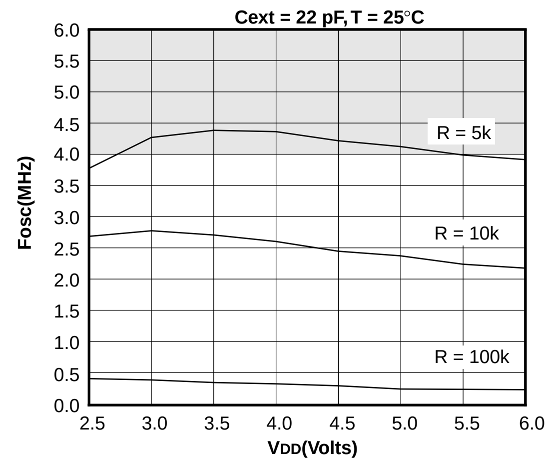



**FIGURE 12-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**




Shaded area is beyond recommended range.

**FIGURE 12-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**

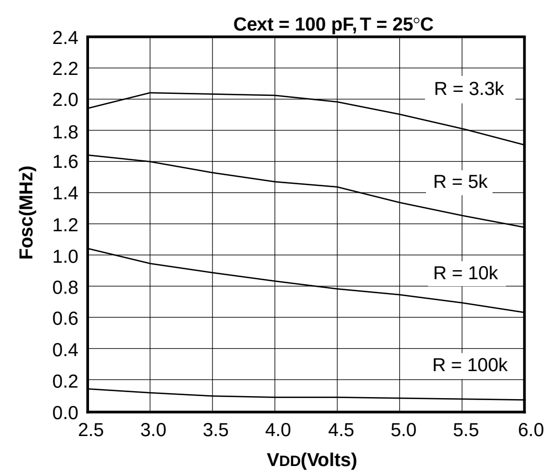
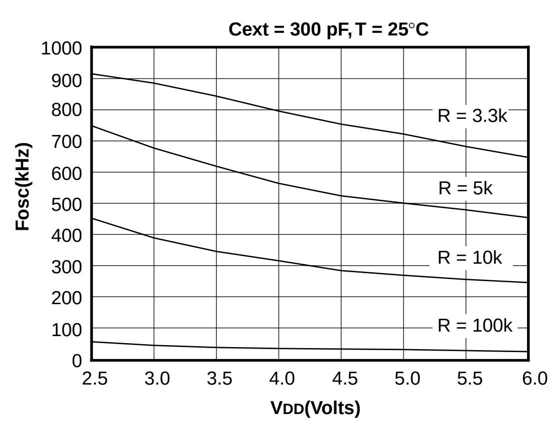
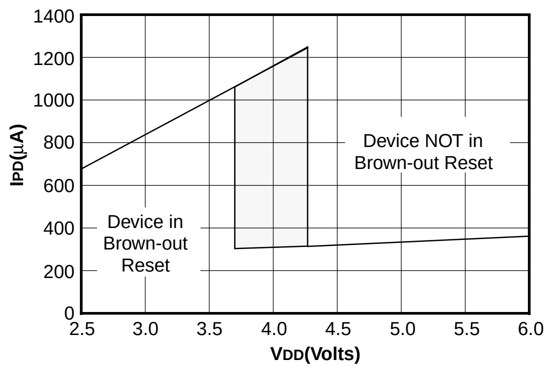



**FIGURE 12-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



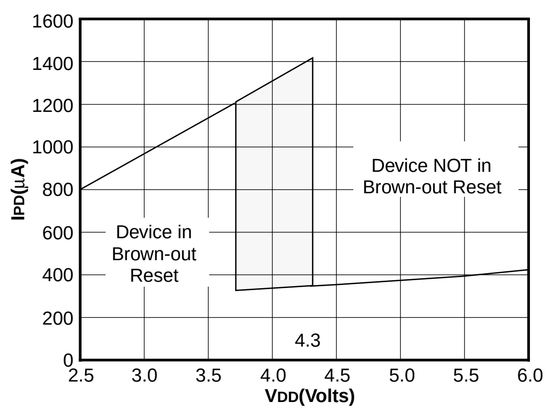
| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 12-8: TYPICAL $I_{PD}$ vs. $V_{DD}$ BROWN-OUT DETECT ENABLED (RC MODE)**




The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

**FIGURE 12-9: MAXIMUM $I_{PD}$ vs. $V_{DD}$ BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)**




The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

**FIGURE 12-10: TYPICAL $I_{PD}$ vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)**

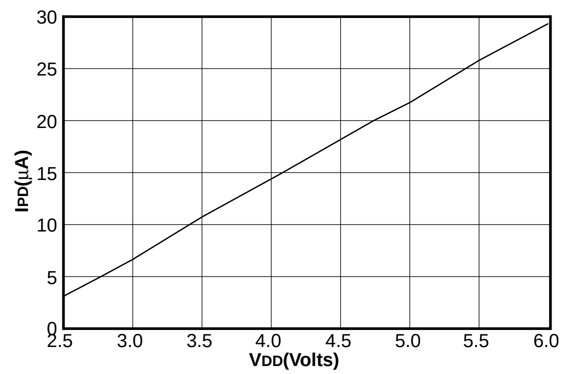
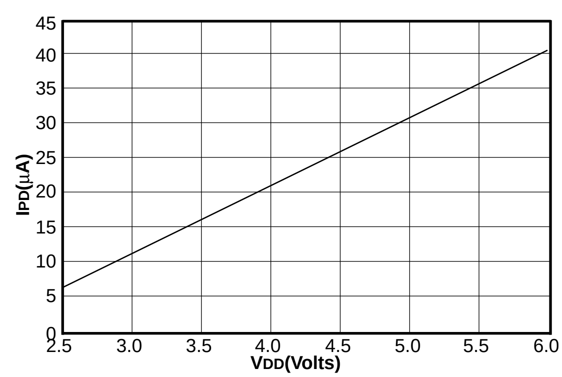



**FIGURE 12-11: MAXIMUM $I_{PD}$ vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)**



Applicable Devices 710 71 711 715

**TABLE 13-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)**

| OSC | PIC16C715-04 | PIC16C715-10 | PIC16C715-20 | PIC16LC715-04 | PIC16C715/JW |
|---|---|---|---|---|---|
| RC | VDD: 4.0V to 5.5V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 5.5V<br>IDD: 2.0 mA typ. at 3.0V<br>IPD: 0.9 µA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 5.5V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. |
| XT | VDD: 4.0V to 5.5V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 2.7 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4V<br>Freq: 4 MHz max. | VDD: 2.5V to 5.5V<br>IDD: 2.0 mA typ. at 3.0V<br>IPD: 0.9 µA typ. at 3V<br>Freq: 4 MHz max. | VDD: 4.0V to 5.5V<br>IDD: 5 mA max. at 5.5V<br>IPD: 21 µA max. at 4V<br>Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V<br>IDD: 13.5 mA typ. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 4 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 20 MHz max. | Do not use in HS mode | VDD: 4.5V to 5.5V<br>IDD: 30 mA max. at 5.5V<br>IPD: 1.5 µA typ. at 4.5V<br>Freq: 10 MHz max. |
| LP | VDD: 4.0V to 5.5V<br>IDD: 52.5 µA typ. at 32 kHz, 4.0V<br>IPD: 0.9 µA typ. at 4.0V<br>Freq: 200 kHz max. | Do not use in LP mode | Do not use in LP mode | VDD: 2.5V to 5.5V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. | VDD: 2.5V to 5.5V<br>IDD: 48 µA max. at 32 kHz, 3.0V<br>IPD: 5.0 µA max. at 3.0V<br>Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

## 13.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

| **T** | | | |
|---|---|---|---|
| F | Frequency | T | Time |

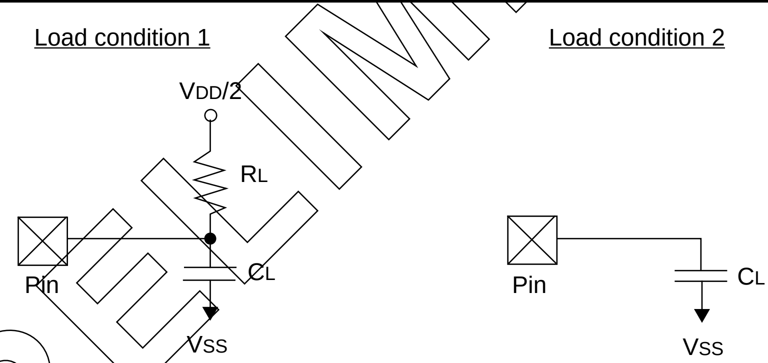
Lowercase letters (pp) and their meanings:

| **pp** | | | |
|---|---|---|---|
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{\text{RD}}$ |
| cs | $\overline{\text{CS}}$ | rw | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{\text{SS}}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | $\overline{\text{MCLR}}$ | wr | $\overline{\text{WR}}$ |

Uppercase letters and their meanings:

| **S** | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (Hi-impedance) | V | Valid |
| L | Low | Z | Hi-impedance |

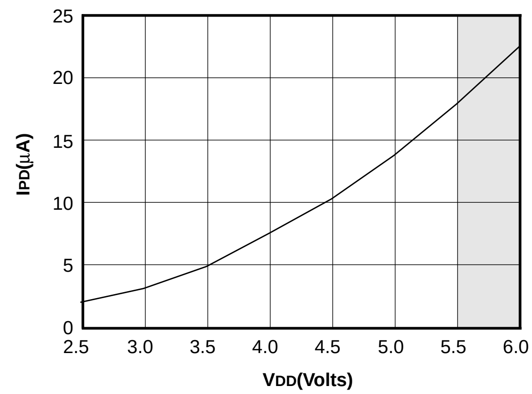
**FIGURE 13-1: LOAD CONDITIONS**




$R_L$ = 464Ω
$C_L$ = 50 pF for all pins except OSC2
15 pF for OSC2 output

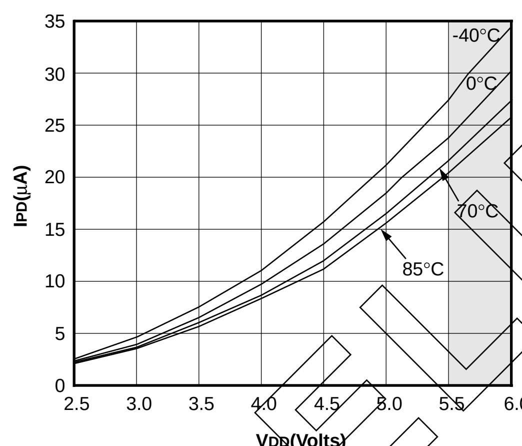
| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)**



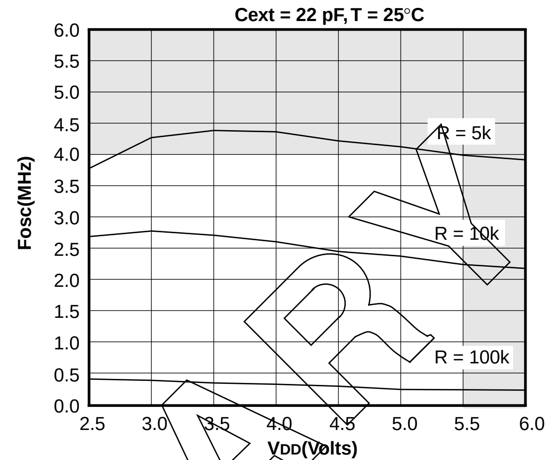

Shaded area is beyond recommended range.

**FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)**



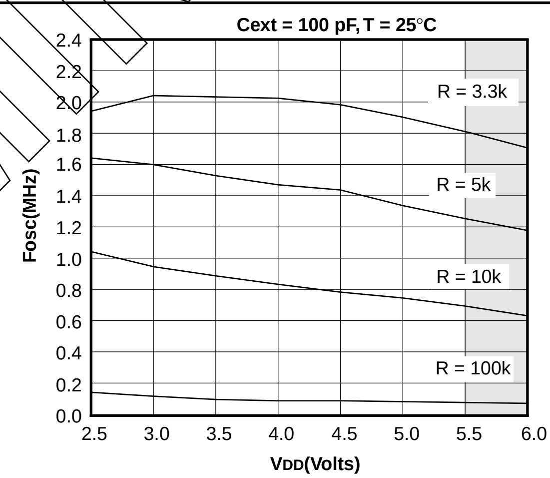

Shaded area is beyond recommended range.

**FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**



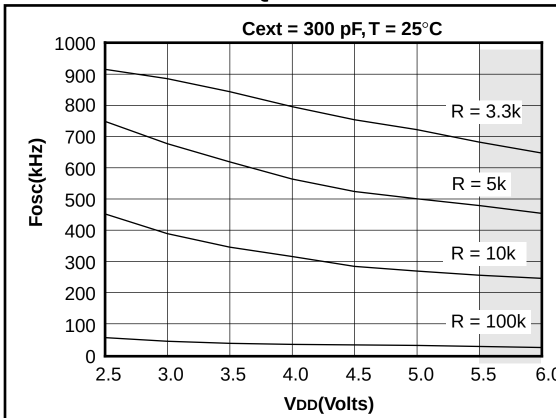

Shaded area is beyond recommended range.

**FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**




Shaded area is beyond recommended range.

**FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD**




Shaded area is beyond recommended range.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 14-12: TYPICAL IDD vs. FREQUENCY (RC MODE @ 22 pF, 25°C)**

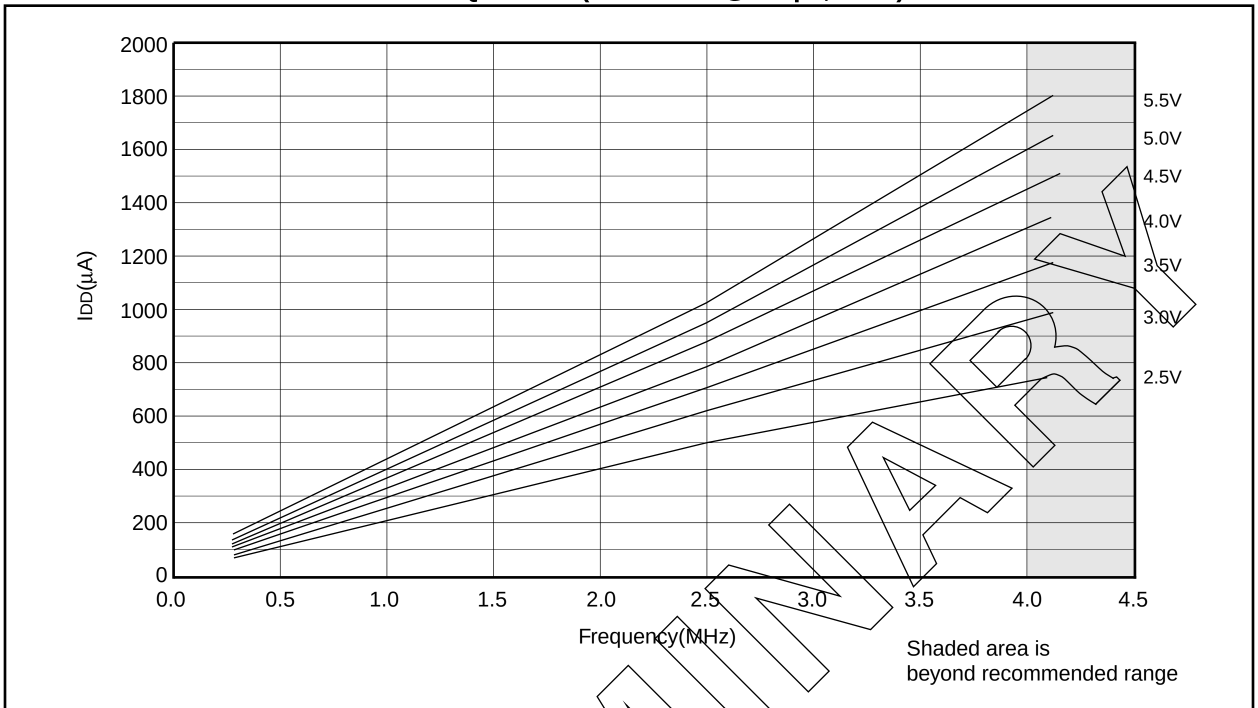
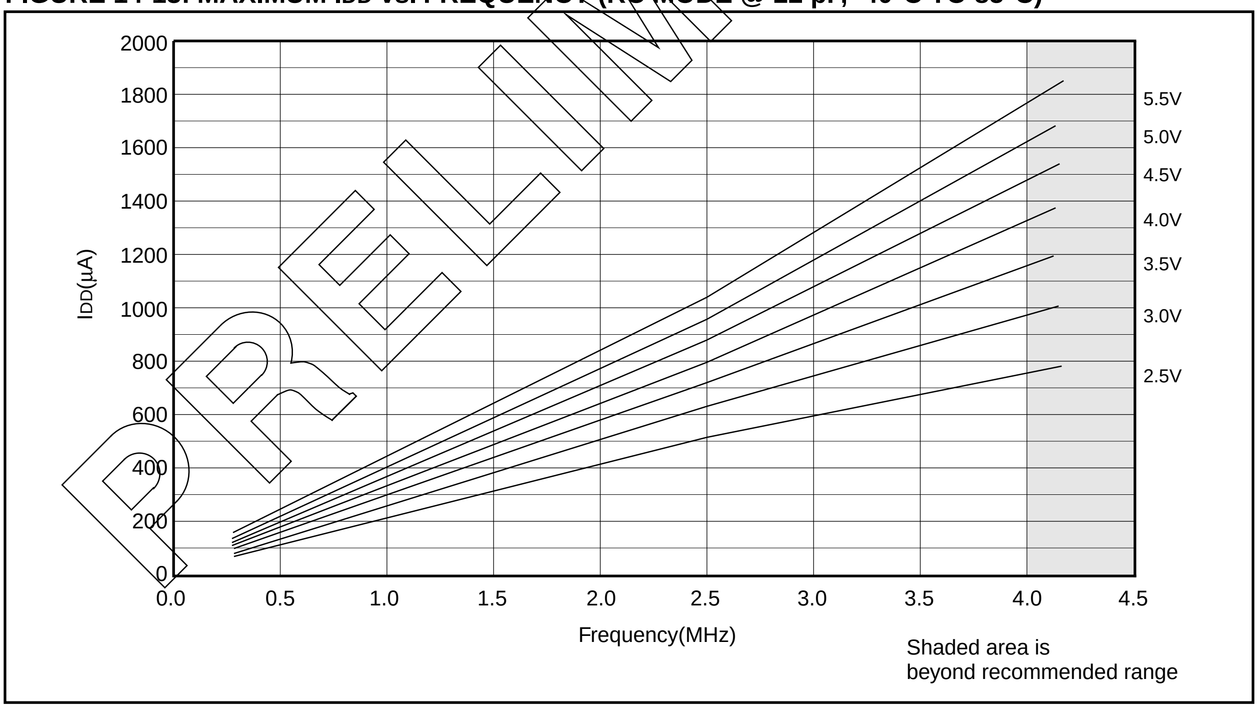



**FIGURE 14-13: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)**



| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 16-21: IOL VS. VOL, VDD = 3V**

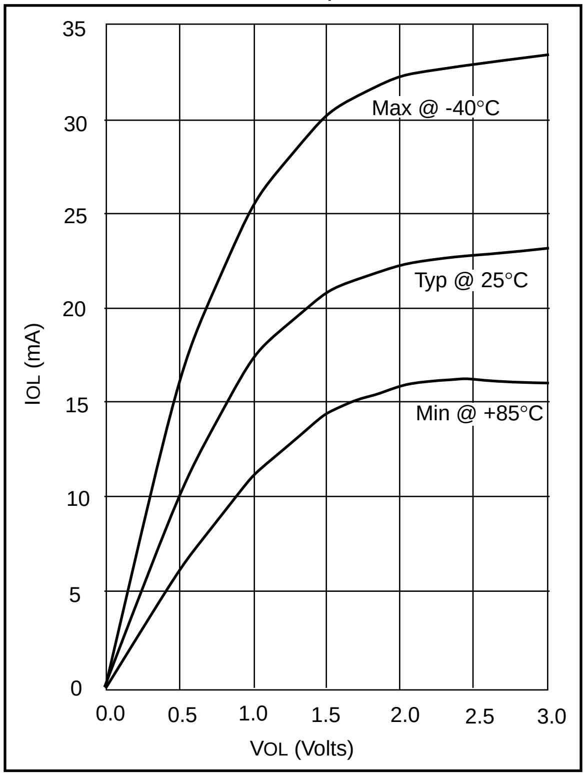
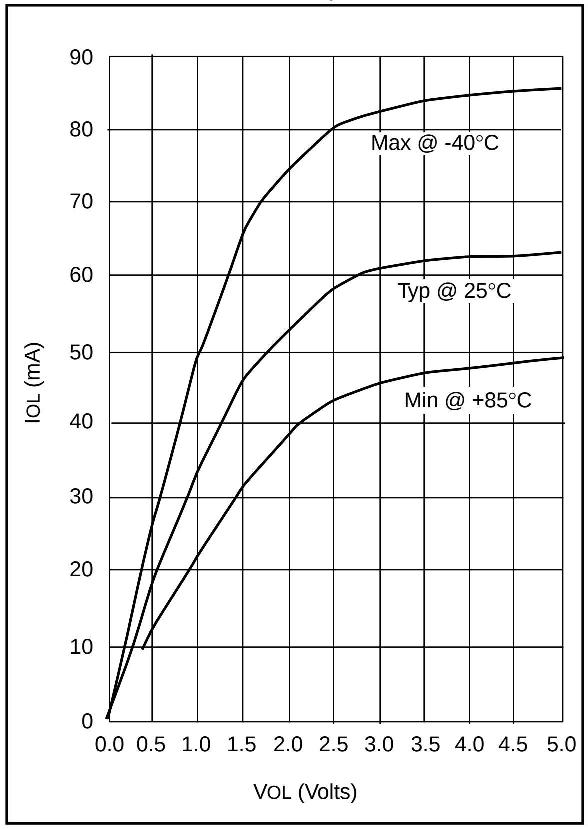


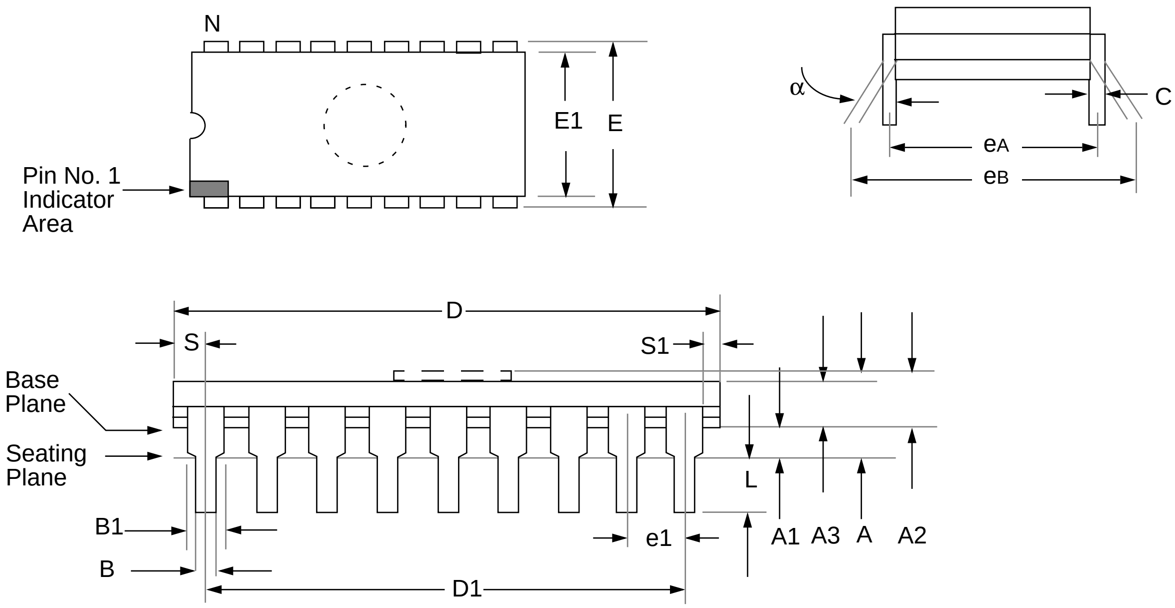

**FIGURE 16-22: IOL VS. VOL, VDD = 5V**




Data based on matrix samples. See first page of this section for details.

# 17.0 PACKAGING INFORMATION

## 17.1 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)




| Package Group: Ceramic CERDIP Dual In-Line (CDP) | | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| Symbol | Min | Max | Notes | Min | Max | Notes |
| α | 0° | 10° | | 0° | 10° | |
| A | — | 5.080 | | — | 0.200 | |
| A1 | 0.381 | 1.7780 | | 0.015 | 0.070 | |
| A2 | 3.810 | 4.699 | | 0.150 | 0.185 | |
| A3 | 3.810 | 4.445 | | 0.150 | 0.175 | |
| B | 0.355 | 0.585 | | 0.014 | 0.023 | |
| B1 | 1.270 | 1.651 | **Typical** | 0.050 | 0.065 | **Typical** |
| C | 0.203 | 0.381 | **Typical** | 0.008 | 0.015 | **Typical** |
| D | 22.352 | 23.622 | | 0.880 | 0.930 | |
| D1 | 20.320 | 20.320 | **Reference** | 0.800 | 0.800 | **Reference** |
| E | 7.620 | 8.382 | | 0.300 | 0.330 | |
| E1 | 5.588 | 7.874 | | 0.220 | 0.310 | |
| e1 | 2.540 | 2.540 | **Reference** | 0.100 | 0.100 | **Reference** |
| eA | 7.366 | 8.128 | **Typical** | 0.290 | 0.320 | **Typical** |
| eB | 7.620 | 10.160 | | 0.300 | 0.400 | |
| L | 3.175 | 3.810 | | 0.125 | 0.150 | |
| N | 18 | 18 | | 18 | 18 | |
| S | 0.508 | 1.397 | | 0.020 | 0.055 | |
| S1 | 0.381 | 1.270 | | 0.015 | 0.050 | |

## INDEX