# Microchip Technology - PIC16C710-20I/SS Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 13 |
| Program Memory Size | 896B (512 x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 36 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 6V |
| Data Converters | A/D 4x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c710-20i-ss |

**TABLE 3-1: PIC16C710/71/711/715 PINOUT DESCRIPTION**

| Pin Name | DIP Pin# | SSOP Pin#(4) | SOIC Pin# | I/O/P Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| OSC1/CLKIN | 16 | 18 | 16 | I | ST/CMOS(3) | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 15 | 17 | 15 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| $\overline{MCLR}$/VPP | 4 | 4 | 4 | I/P | ST | Master clear (reset) input or programming voltage input. This pin is an active low reset to the device. |
| | | | | | | PORTA is a bi-directional I/O port. |
| RA0/AN0 | 17 | 19 | 17 | I/O | TTL | RA0 can also be analog input0 |
| RA1/AN1 | 18 | 20 | 18 | I/O | TTL | RA1 can also be analog input1 |
| RA2/AN2 | 1 | 1 | 1 | I/O | TTL | RA2 can also be analog input2 |
| RA3/AN3/VREF | 2 | 2 | 2 | I/O | TTL | RA3 can also be analog input3 or analog reference voltage |
| RA4/T0CKI | 3 | 3 | 3 | I/O | ST | RA4 can also be the clock input to the Timer0 module. Output is open drain type. |
| | | | | | | PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. |
| RB0/INT | 6 | 7 | 6 | I/O | TTL/ST(1) | RB0 can also be the external interrupt pin. |
| RB1 | 7 | 8 | 7 | I/O | TTL | |
| RB2 | 8 | 9 | 8 | I/O | TTL | |
| RB3 | 9 | 10 | 9 | I/O | TTL | |
| RB4 | 10 | 11 | 10 | I/O | TTL | Interrupt on change pin. |
| RB5 | 11 | 12 | 11 | I/O | TTL | Interrupt on change pin. |
| RB6 | 12 | 13 | 12 | I/O | TTL/ST(2) | Interrupt on change pin. Serial programming clock. |
| RB7 | 13 | 14 | 13 | I/O | TTL/ST(2) | Interrupt on change pin. Serial programming data. |
| VSS | 5 | 4, 6 | 5 | P | — | Ground reference for logic and I/O pins. |
| VDD | 14 | 15, 16 | 14 | P | — | Positive supply for logic and I/O pins. |

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
4: The PIC16C71 is not available in SSOP package.

## 4.0 MEMORY ORGANIZATION

### 4.1 Program Memory Organization

The PIC16C71X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

| Device | Program Memory | Address Range |
|---|---|---|
| PIC16C710 | 512 x 14 | 0000h-01FFh |
| PIC16C71 | 1K x 14 | 0000h-03FFh |
| PIC16C711 | 1K x 14 | 0000h-03FFh |
| PIC16C715 | 2K x 14 | 0000h-07FFh |

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

**FIGURE 4-1: PIC16C710 PROGRAM MEMORY MAP AND STACK**

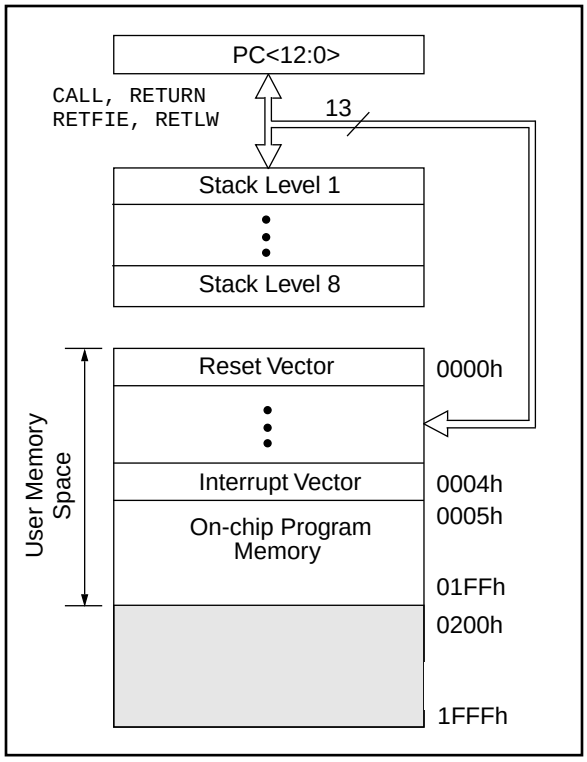



**FIGURE 4-2: PIC16C71/711 PROGRAM MEMORY MAP AND STACK**

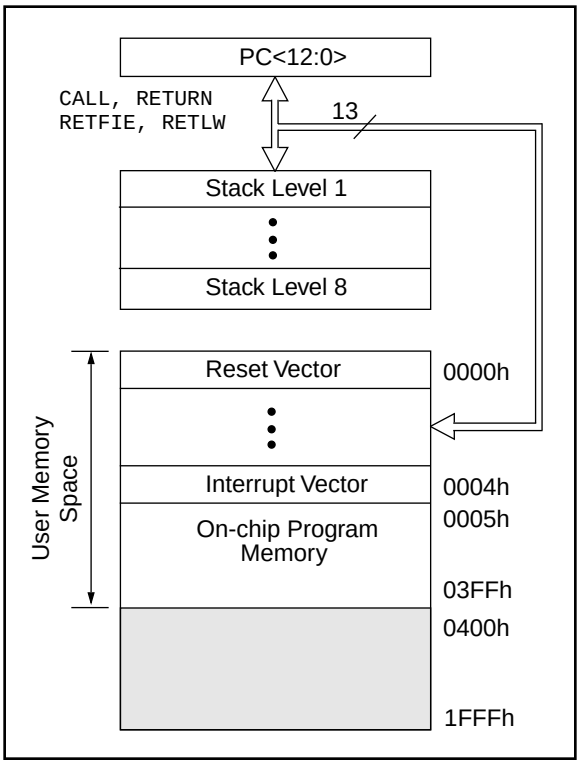
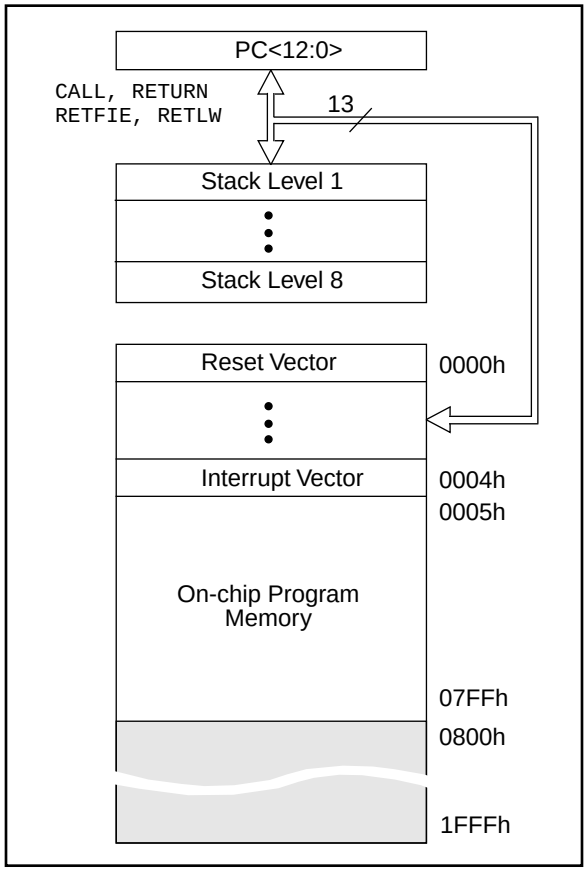



**FIGURE 4-3: PIC16C715 PROGRAM MEMORY MAP AND STACK**



### 6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

**Note:** To avoid an unintended device RESET, the following instruction sequence (shown in Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

**EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)**

```
BCF    STATUS, RP0  ;Bank 0
CLRF   TMR0         ;Clear TMR0 & Prescaler
BSF    STATUS, RP0  ;Bank 1
CLRWDT              ;Clears WDT
MOVLW  b'xxxx1xxx'  ;Selects new prescale value
MOVWF  OPTION_REG   ;and assigns the prescaler to the WDT
BCF    STATUS, RP0  ;Bank 0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 6-2.

**EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)**

```
CLRWDT               ;Clear WDT and prescaler
BSF      STATUS, RP0 ;Bank 1
MOVLW    b'xxxx0xxx' ;Select TMR0, new prescale value and
MOVWF    OPTION_REG  ;clock source
BCF      STATUS, RP0 ;Bank 0
```

**TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | TMR0 | Timer0 module’s register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Bh,8Bh, | INTCON | GIE | ADIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 81h | OPTION | $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 85h | TRISA | — | — | — | PORTA Data Direction Register | | | | | ---1 1111 | ---1 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

## 8.0 SPECIAL FEATURES OF THE CPU

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR) (PIC16C710/711/715)
  - Parity Error Reset (PER) (PIC16C715)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

### 8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

**FIGURE 8-1: CONFIGURATION WORD FOR PIC16C71**

| — | — | — | — | — | — | — | — | — | CP0 | PWRTE | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

bit13 bit0

Register: CONFIG
Address 2007h

bit 13-5: **Unimplemented:** Read as '1'

bit 4: **CP0:** Code protection bit
1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 3: **PWRTE:** Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

**TABLE 8-10: RESET CONDITION FOR SPECIAL REGISTERS, PIC16C710/71/711**

| Condition | Program Counter | STATUS Register | PCON Register PIC16C710/711 |
|---|---|---|---|
| Power-on Reset | 000h | 0001 1xxx | ---- --0x |
| $\overline{MCLR}$ Reset during normal operation | 000h | 000u uuuu | ---- --uu |
| $\overline{MCLR}$ Reset during SLEEP | 000h | 0001 0uuu | ---- --uu |
| WDT Reset | 000h | 0000 1uuu | ---- --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | ---- --uu |
| Brown-out Reset (PIC16C710/711) | 000h | 0001 1uuu | ---- --u0 |
| Interrupt wake-up from SLEEP | PC + 1(1) | uuu1 0uuu | ---- --uu |

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**TABLE 8-11: RESET CONDITION FOR SPECIAL REGISTERS, PIC16C715**

| Condition | Program Counter | STATUS Register | PCON Register |
|---|---|---|---|
| Power-on Reset | 000h | 0001 1xxx | u--- -10x |
| $\overline{MCLR}$ Reset during normal operation | 000h | 000u uuuu | u--- -uuu |
| $\overline{MCLR}$ Reset during SLEEP | 000h | 0001 0uuu | u--- -uuu |
| WDT Reset | 000h | 0000 1uuu | u--- -uuu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | u--- -uuu |
| Brown-out Reset | 000h | 0001 1uuu | u--- -uu0 |
| Parity Error Reset | 000h | uuu1 0uuu | u--- -0uu |
| Interrupt wake-up from SLEEP | PC + 1(1) | uuu1 0uuu | u--- -uuu |

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO $V_{DD}$): CASE 1**

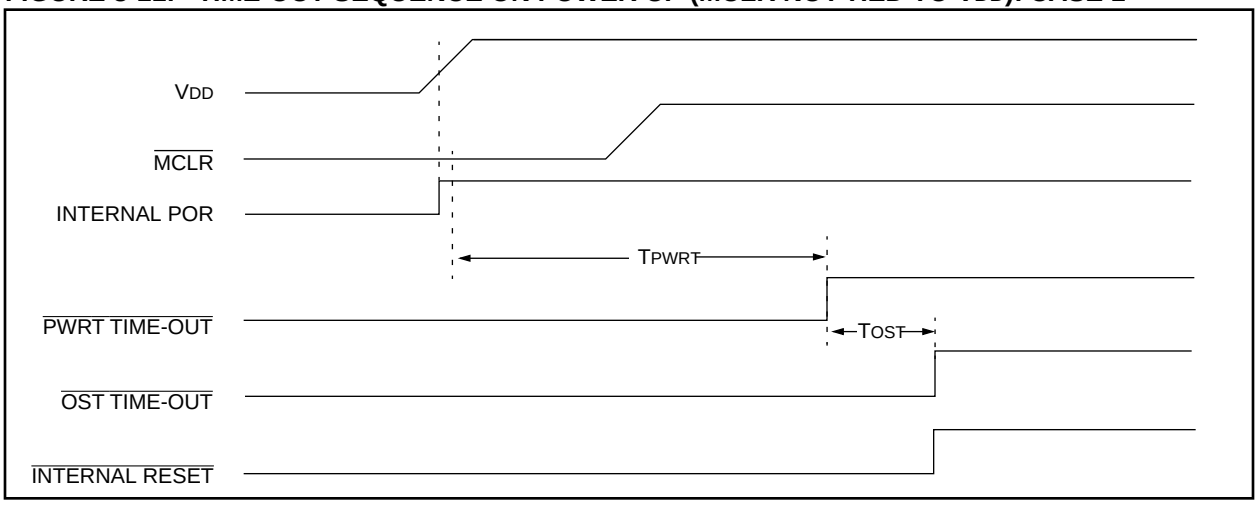



**FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO $V_{DD}$): CASE 2**

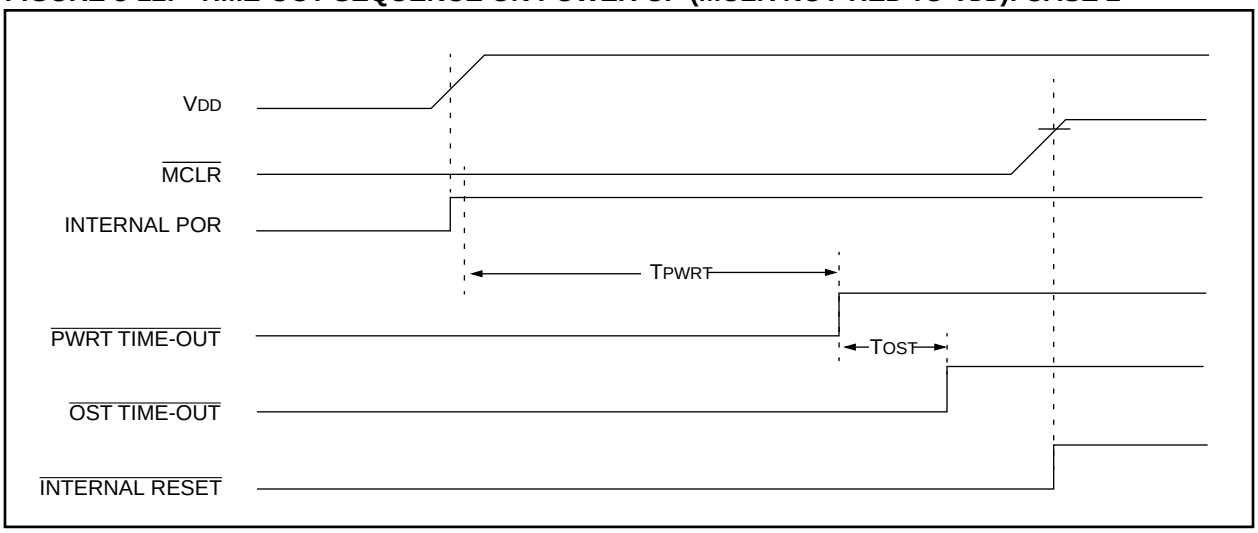



**FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO $V_{DD}$)**

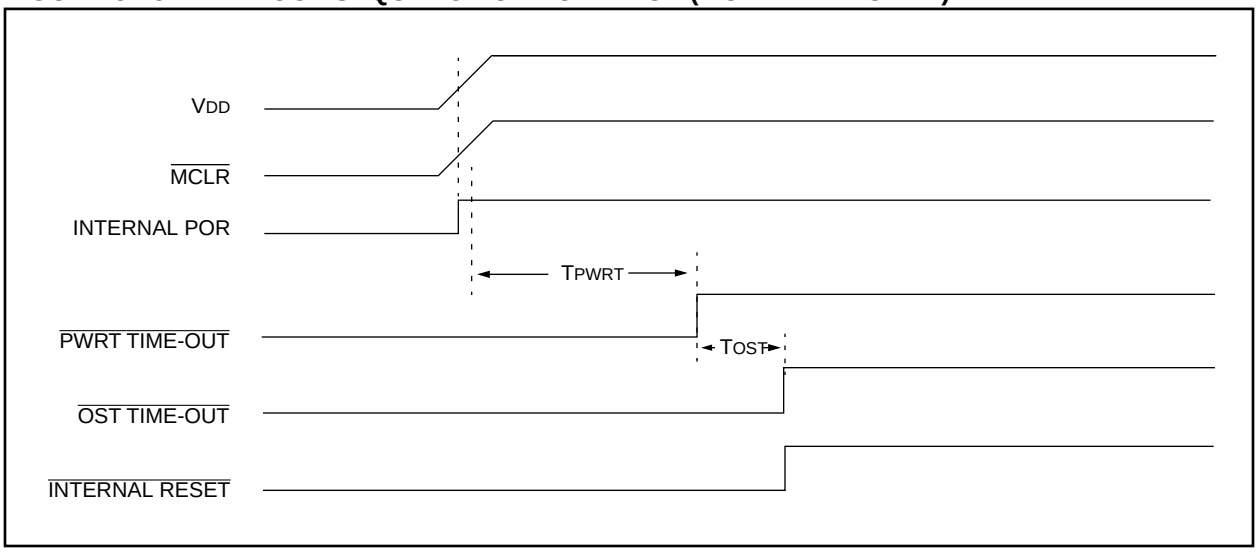


**FIGURE 8-17: INTERRUPT LOGIC, PIC16C710, 71, 711**

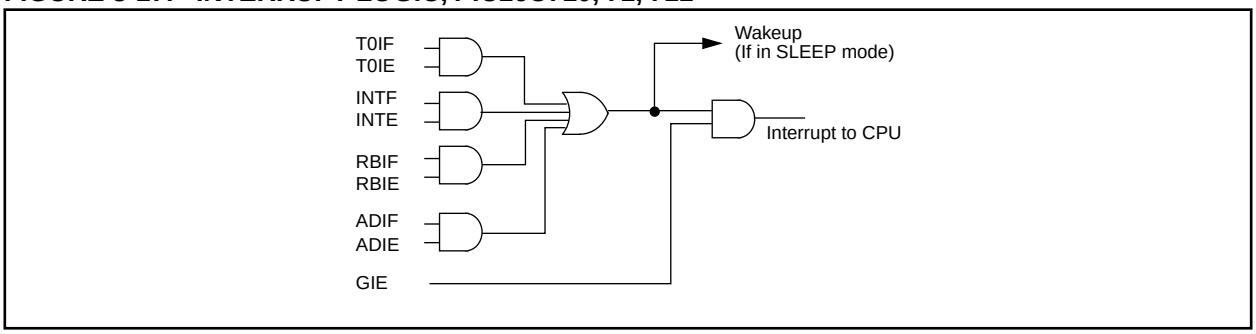
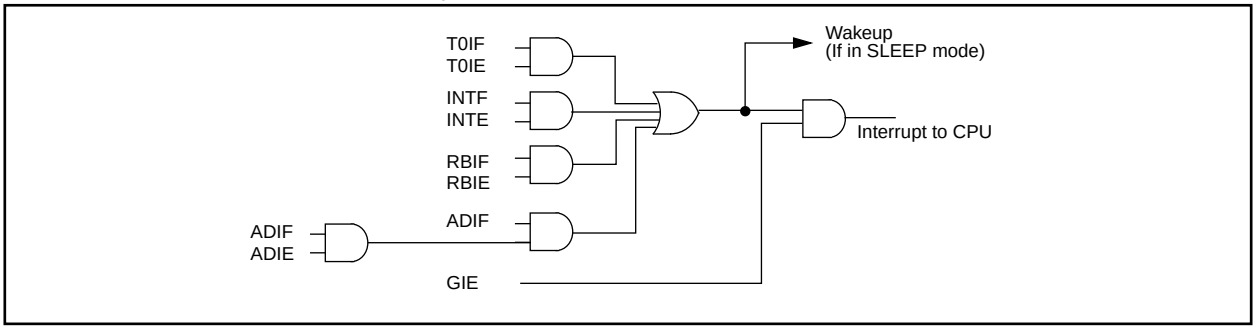



**FIGURE 8-18: INTERRUPT LOGIC, PIC16C715**



**NOTES:**

**GOTO** **Unconditional Branch**

Syntax: [ *label* ] GOTO k

Operands: $0 \le k \le 2047$

Operation: $k \rightarrow PC<10:0>$
$PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 10 | 1kkk | kkkk | kkkk |

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

| | Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|---|
| 1st Cycle | Decode | Read literal 'k' | Process data | Write to PC |
| 2nd Cycle | NOP | NOP | NOP | NOP |

Example

```
GOTO THERE
```

After Instruction
PC = Address THERE

**INCF** **Increment f**

Syntax: [ *label* ] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 1010 | dfff | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to dest |

Example

```
INCF    CNT, 1
```

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

**SLEEP**

Syntax: [ *label* ] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| | | | |
|---|---|---|---|
| 00 | 0000 | 0110 | 0011 |

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Section 8.8 for more details.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | NOP | Go to Sleep |

Example: SLEEP

**SUBLW Subtract W from Literal**

Syntax: [ *label* ] SUBLW k

Operands: 0 ≤ k ≤ 255

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Encoding:

| | | | |
|---|---|---|---|
| 11 | 110x | kkkk | kkkk |

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Process data | Write to W |

Example 1: SUBLW 0x02

Before Instruction
W = 1
C = ?
Z = ?

After Instruction
W = 1
C = 1; result is positive
Z = 0

Example 2: Before Instruction
W = 2
C = ?
Z = ?

After Instruction
W = 0
C = 1; result is zero
Z = 1

Example 3: Before Instruction
W = 3
C = ?
Z = ?

After Instruction
W = 0xFF
C = 0; result is negative
Z = 0

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

### 10.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

### 10.12 C Compiler (MPLAB-C)

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

### 10.13 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

### 10.14 MP-DriveWay™ – Application Code Generator

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

### 10.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

### 10.16 KEELOQ® Evaluation and Programming Tools

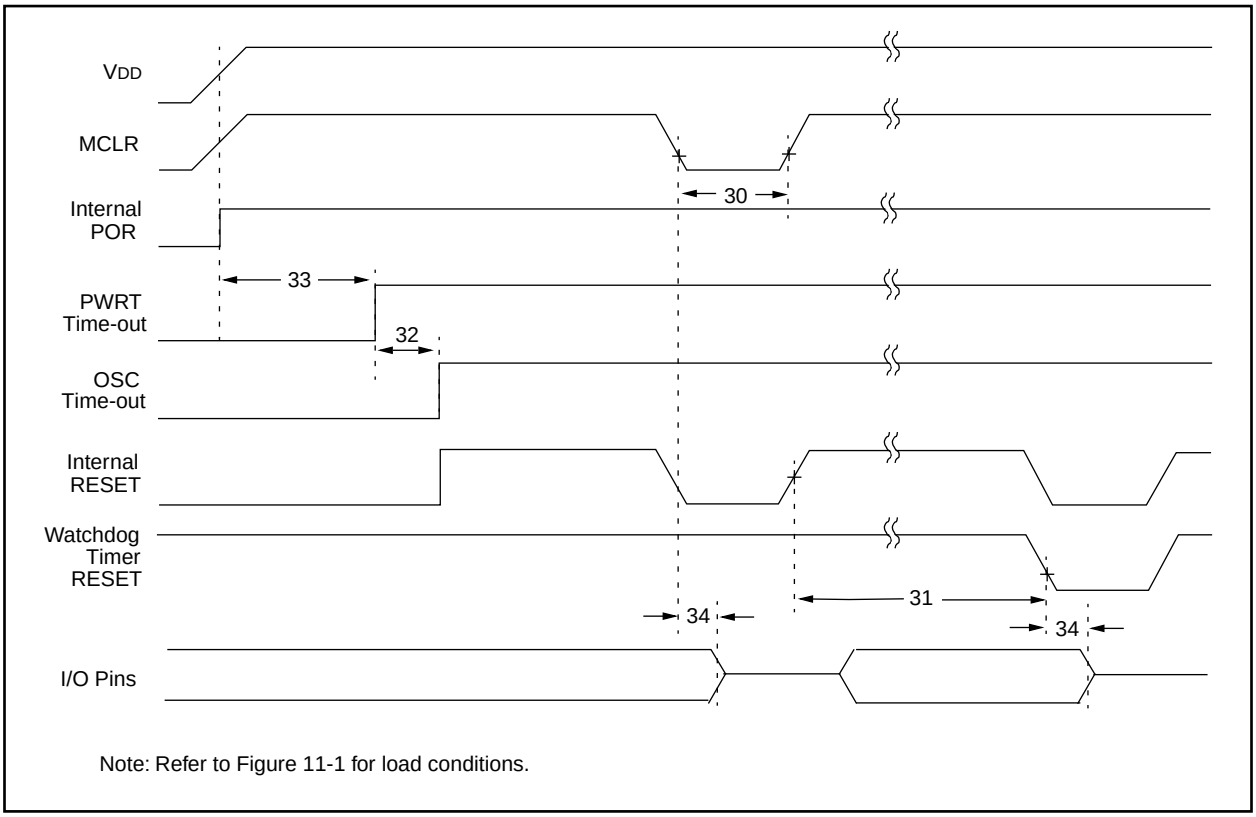
KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

**TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP**

| | | PIC12C5XX | PIC14000 | PIC16C5X | PIC16CXXX | PIC16C6X | PIC16C7XX | PIC16C8X | PIC16C9XX | PIC17C4X | PIC17C75X | 24CXX 25CXX 93CXX | HCS200 HCS300 HCS301 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Emulator Products | PICMASTER®/ PICMASTER-CE In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | Available 3Q97 | | |
| | ICEPIC Low-Cost In-Circuit Emulator | ✓ | | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | |
| Software Tools | MPLAB™ Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | MPLAB™ C Compiler | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | *fuzzy*TECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | MP-DriveWay™ Applications Code Generator | | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | | |
| | Total Endurance™ Software Model | | | | | | | | | | | ✓ | |
| Programmers | PICSTART® Lite Ultra Low-Cost Dev. Kit | | | ✓ | | ✓ | ✓ | ✓ | | | | | |
| | PICSTART® Plus Low-Cost Universal Dev. Kit | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| | PRO MATE® II Universal Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | KEELOQ® Programmer | | | | | | | | | | | | ✓ |
| Demo Boards | SEEVAL® Designers Kit | | | | | | | | | | | ✓ | |
| | PICDEM-1 | | | ✓ | ✓ | | | ✓ | | ✓ | | | |
| | PICDEM-2 | | | | | ✓ | ✓ | | | | | | |
| | PICDEM-3 | | | | | | | | ✓ | | | | |
| | KEELOQ® Evaluation Kit | | | | | | | | | | | | ✓ |

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 11-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




Note: Refer to Figure 11-1 for load conditions.

**FIGURE 11-5: BROWN-OUT RESET TIMING**

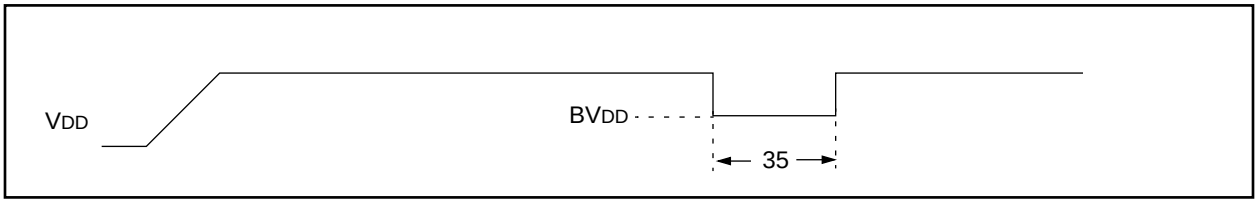



**TABLE 11-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30 | TmcL | $\overline{MCLR}$ Pulse Width (low) | 1 | — | — | µs | VDD = 5V, -40˚C to +125˚C |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7* | 18 | 33* | ms | VDD = 5V, -40˚C to +125˚C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024TOSC | — | — | TOSC = OSC1 period |
| 33 | Tpwrt | Power up Timer Period | 28* | 72 | 132* | ms | VDD = 5V, -40˚C to +125˚C |
| 34 | TIOZ | I/O Hi-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset | — | — | 1.1 | µs | |
| 35 | TBOR | Brown-out Reset pulse width | 100 | — | — | µs | 3.8V ≤ VDD ≤ 4.2V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

## 13.1 DC Characteristics: PIC16C715-04 (Commercial, Industrial, Extended) PIC16C715-10 (Commercial, Industrial, Extended) PIC16C715-20 (Commercial, Industrial, Extended))

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>-40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | Supply Voltage | VDD | 4.0 | - | 5.5 | V | XT, RC and LP osc configuration |
| D001A | | | 4.5 | - | 5.5 | V | HS osc configuration |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | V | Device in SLEEP mode |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D005 | Brown-out Reset Voltage | BVDD | 3.7 | 4.0 | 4.3 | V | BODEN configuration bit is enabled |
| D010 | Supply Current (Note 2) | IDD | - | 2.7 | 5 | mA | XT, RC osc configuration (PIC16C715-04)<br>FOSC = 4 MHz, VDD = 5.5V (Note 4) |
| D013 | | | - | 13.5 | 30 | mA | HS osc configuration (PIC16C715-20)<br>FOSC = 20 MHz, VDD = 5.5V |
| D015 | Brown-out Reset Current (Note 5) | ΔIBOR | - | 300* | 500 | µA | BOR enabled VDD = 5.0V |
| D020 | Power-down Current (Note 3) | IPD | - | 10.5 | 42 | µA | VDD = 4.0V, WDT enabled, -40°C to +85°C |
| D021 | | | - | 1.5 | 21 | µA | VDD = 4.0V, WDT disabled, -0°C to +70°C |
| D021A | | | - | 1.5 | 24 | µA | VDD = 4.0V, WDT disabled, -40°C to +85°C |
| D021B | | | - | 1.5 | 30 | µA | VDD = 4.0V, WDT disabled, -40°C to +125°C |
| D023 | Brown-out Reset Current (Note 5) | ΔIBOR | - | 300* | 500 | µA | BOR enabled VDD = 5.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

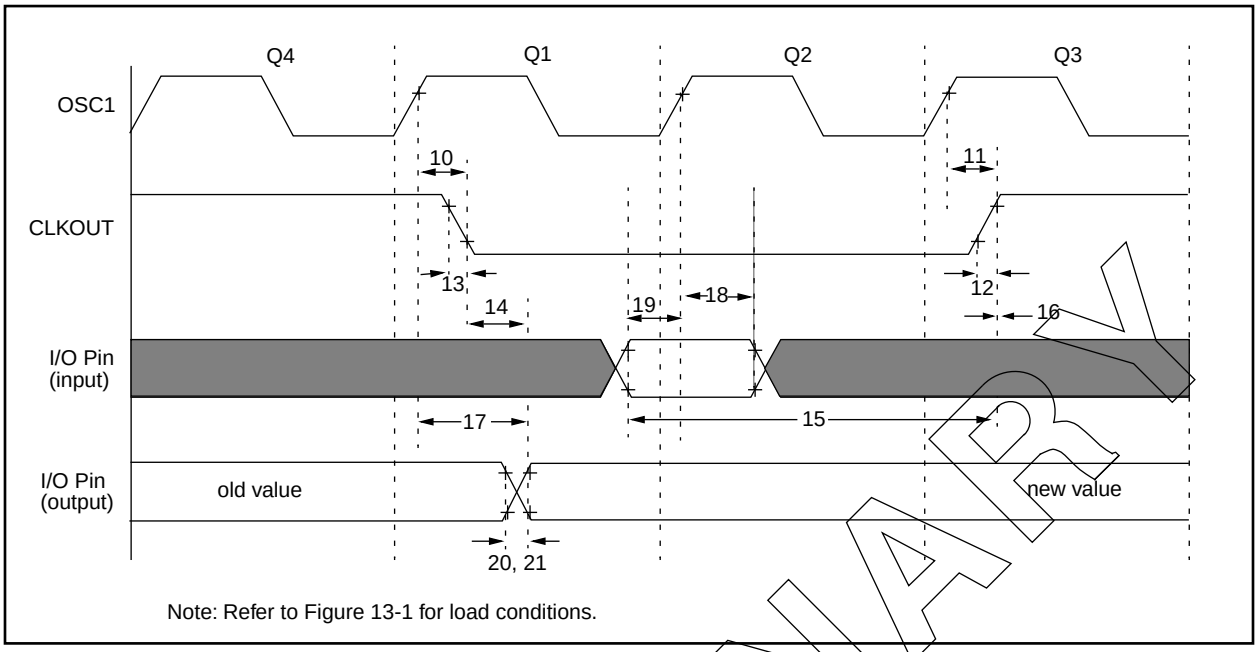
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 13-3: CLKOUT AND I/O TIMING**




Note: Refer to Figure 13-1 for load conditions.

**TABLE 13-3: CLKOUT AND I/O TIMING REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | | — | 15 | 30 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | | — | 15 | 30 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | | — | 5 | 15 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | | — | 5 | 15 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | | 0.25TCY + 25 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | | — | — | 80 - 100 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | | TBD | — | — | ns | |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | | TBD | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16C715 | — | 10 | 25 | ns | |
| | | | PIC16LC715 | — | — | 60 | ns | |
| 21* | TioF | Port output fall time | PIC16C715 | — | 10 | 25 | ns | |
| | | | PIC16LC715 | — | — | 60 | ns | |
| 22††* | Tinp | INT pin high or low time | | 20 | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change INT high or low time | | 20 | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 14-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)**

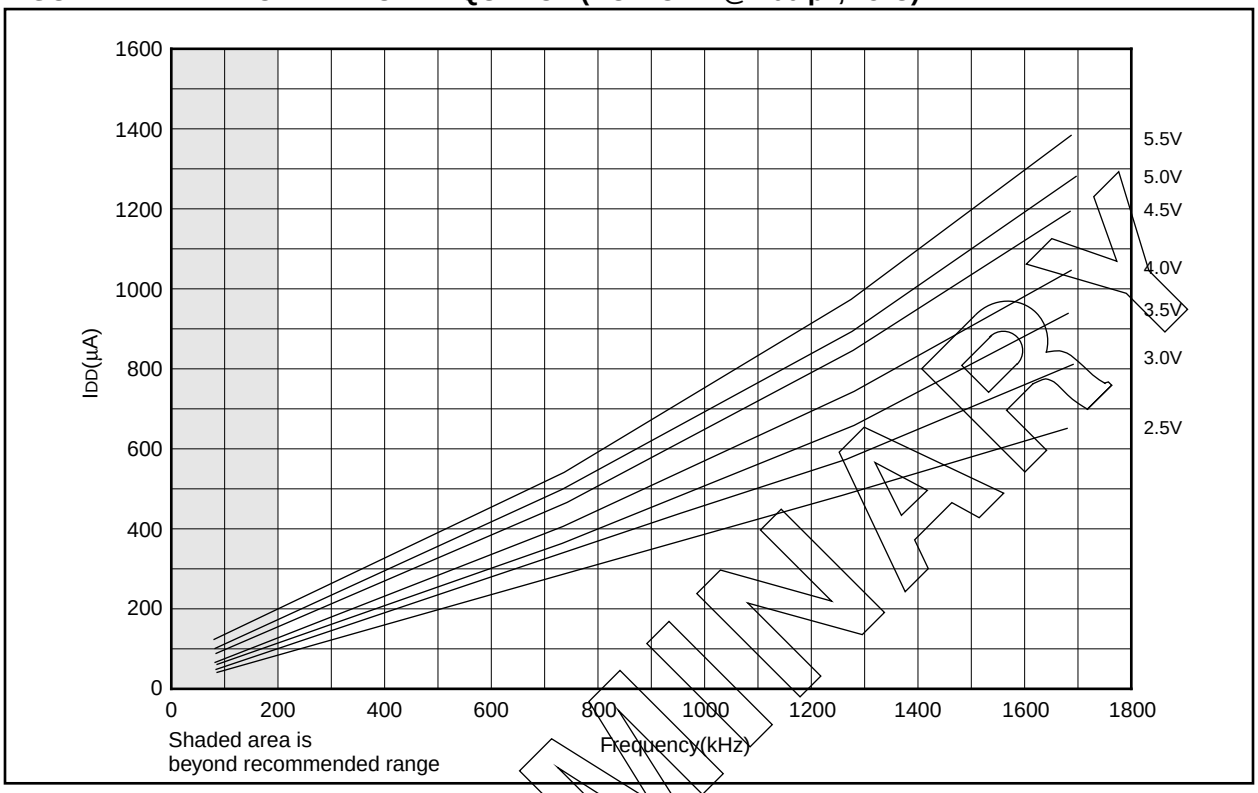
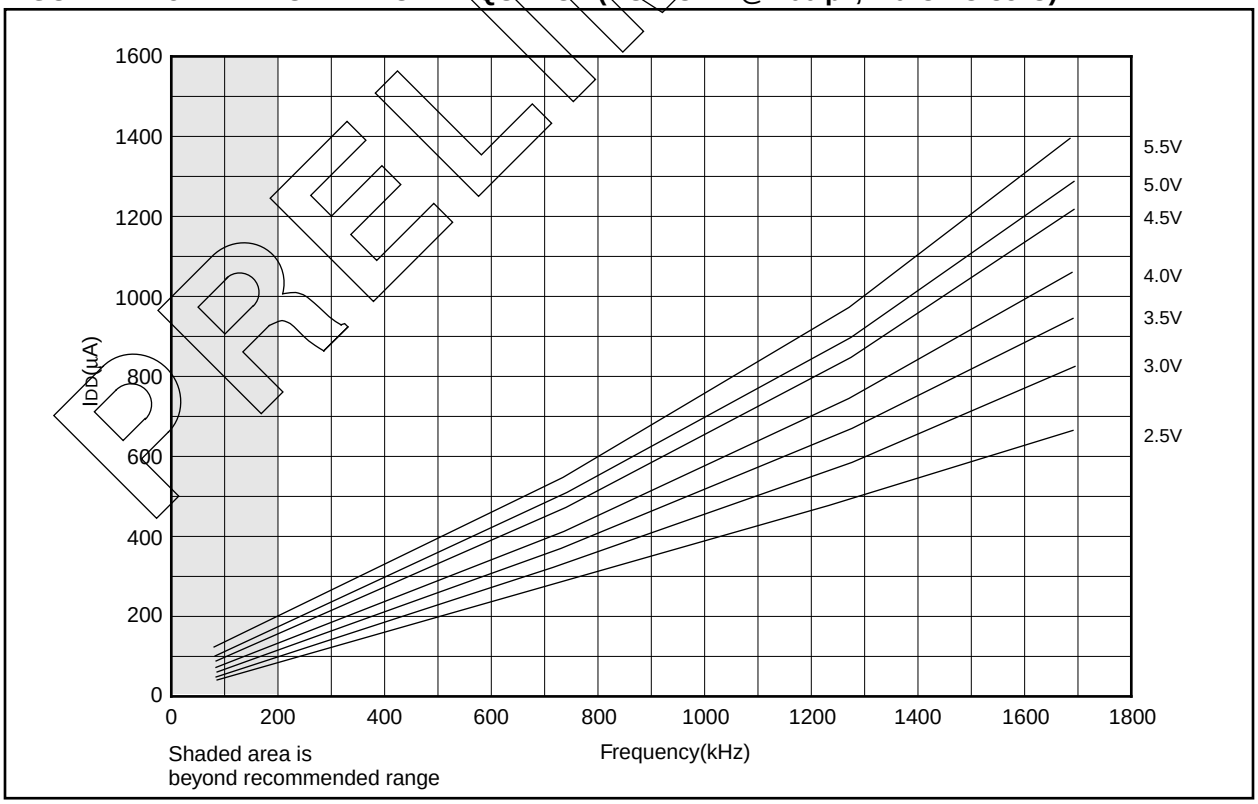



**FIGURE 14-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)**



| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**TABLE 15-6: A/D CONVERTER CHARACTERISTICS**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | | — | — | 8 bits | bits | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| A02 | EABS | Absolute error | PIC16**C**71 | — | — | < ±1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| | | | PIC16**LC**71 | — | — | < ±2 | LSb | VREF = VDD = 3.0V (Note 3) |
| A03 | EIL | Integral linearity error | PIC16**C**71 | — | — | < ±1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| | | | PIC16**LC**71 | — | — | < ±2 | LSb | VREF = VDD = 3.0V (Note 3) |
| A04 | EDL | Differential linearity error | PIC16**C**71 | — | — | < ±1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| | | | PIC16**LC**71 | — | — | < ±2 | LSb | VREF = VDD = 3.0V (Note 3) |
| A05 | EFS | Full scale error | PIC16**C**71 | — | — | < ±1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| | | | PIC16**LC**71 | — | — | < ±2 | LSb | VREF = VDD = 3.0V (Note 3) |
| A06 | EOFF | Offset error | PIC16**C**71 | — | — | < ±1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF |
| | | | PIC16**LC**71 | — | — | < ±2 | LSb | VREF = VDD = 3.0V (Note 3) |
| A10 | — | Monotonicity | | — | guaranteed | — | — | VSS ≤ VAIN ≤ VREF |
| A20 | VREF | Reference voltage | | 3.0V | — | VDD + 0.3 | V | |
| A25 | VAIN | Analog input voltage | | VSS - 0.3 | — | VREF | V | |
| A30 | ZAIN | Recommended impedance of analog voltage source | | — | — | 10.0 | kΩ | |
| A40 | IAD | A/D conversion current (VDD) | | — | 180 | — | μA | Average current consumption when A/D is on. (Note 1) |
| A50 | IREF | VREF input current (Note 2) | PIC16**C**71 | 10 | — | 1000 | μA | During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1. |
| | | | | — | — | 40 | μA | During A/D Conversion cycle |
| | | | PIC16**LC**71 | — | — | 1 | mA | During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1. |
| | | | | — | — | 10 | μA | During A/D Conversion cycle |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

3: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V. VAIN must be between VSS and VREF.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 16-14: MAXIMUM IDD VS. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)**

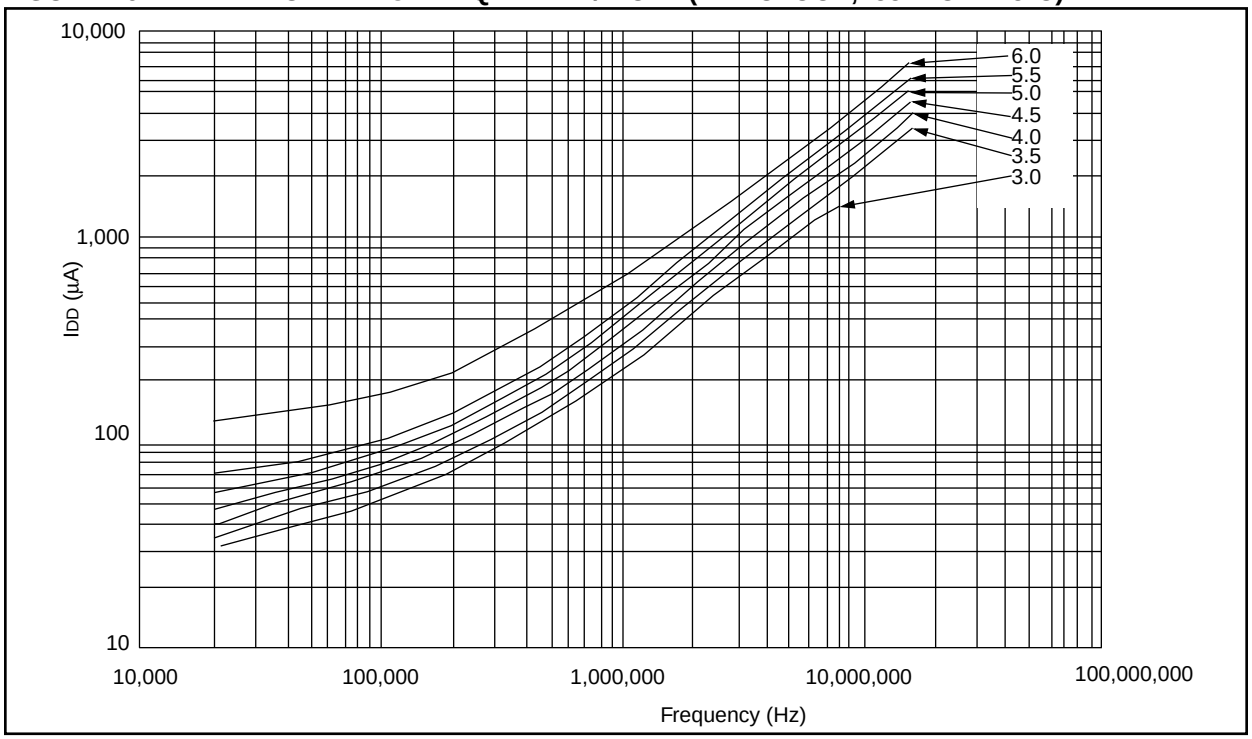



**FIGURE 16-15: WDT TIMER TIME-OUT PERIOD VS. VDD**

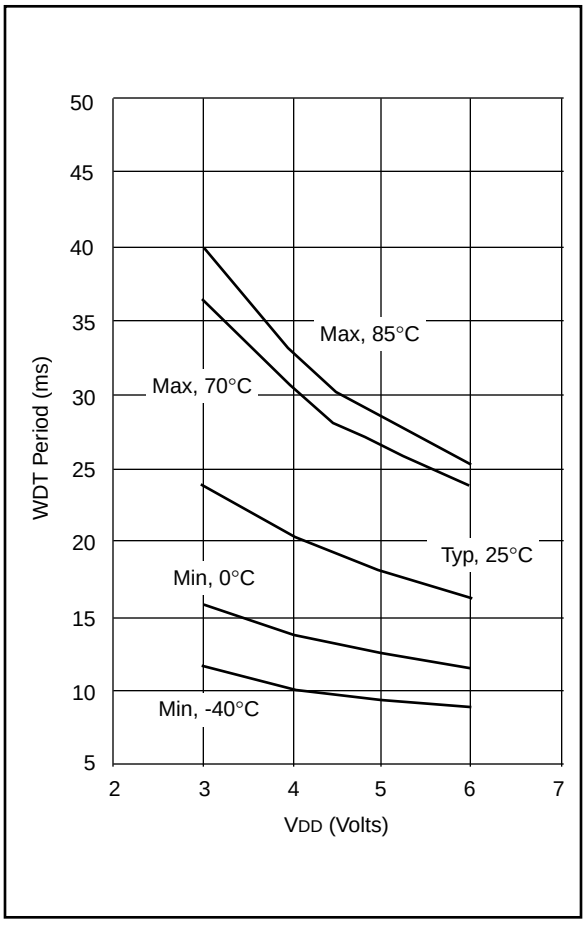
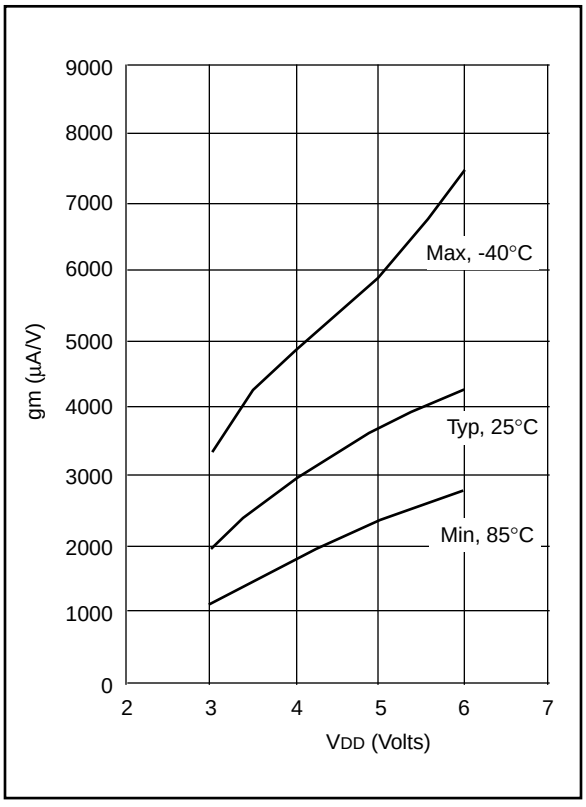



**FIGURE 16-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR VS. VDD**




Data based on matrix samples. See first page of this section for details.

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