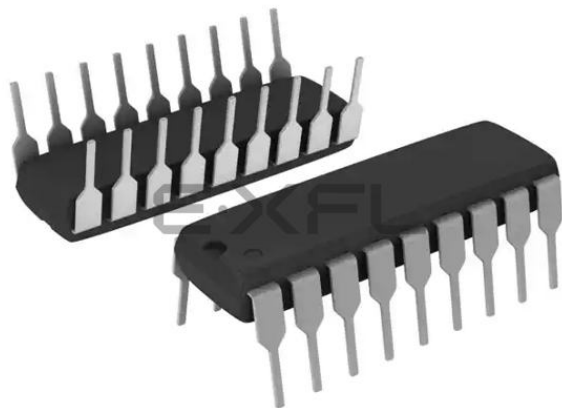




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c711-04-p

PIC16C71X

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input/VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111
9Fh	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

[illegible][illegible]

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

PIC16C71X

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

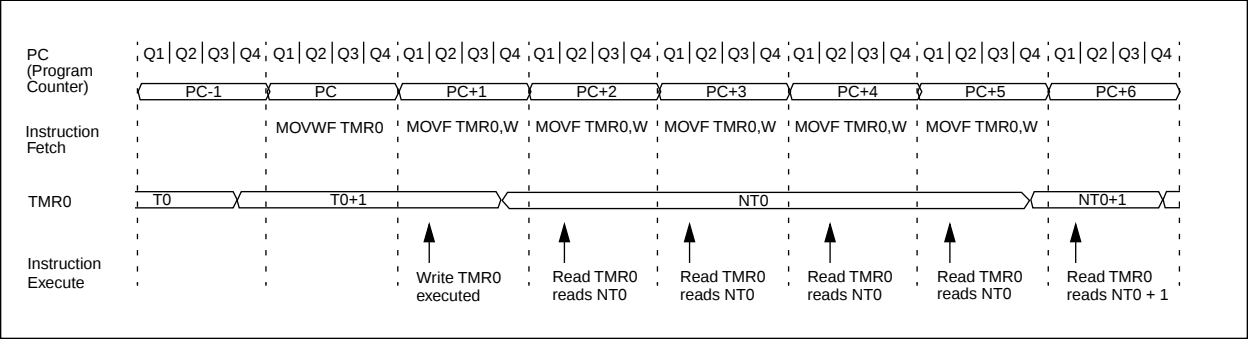
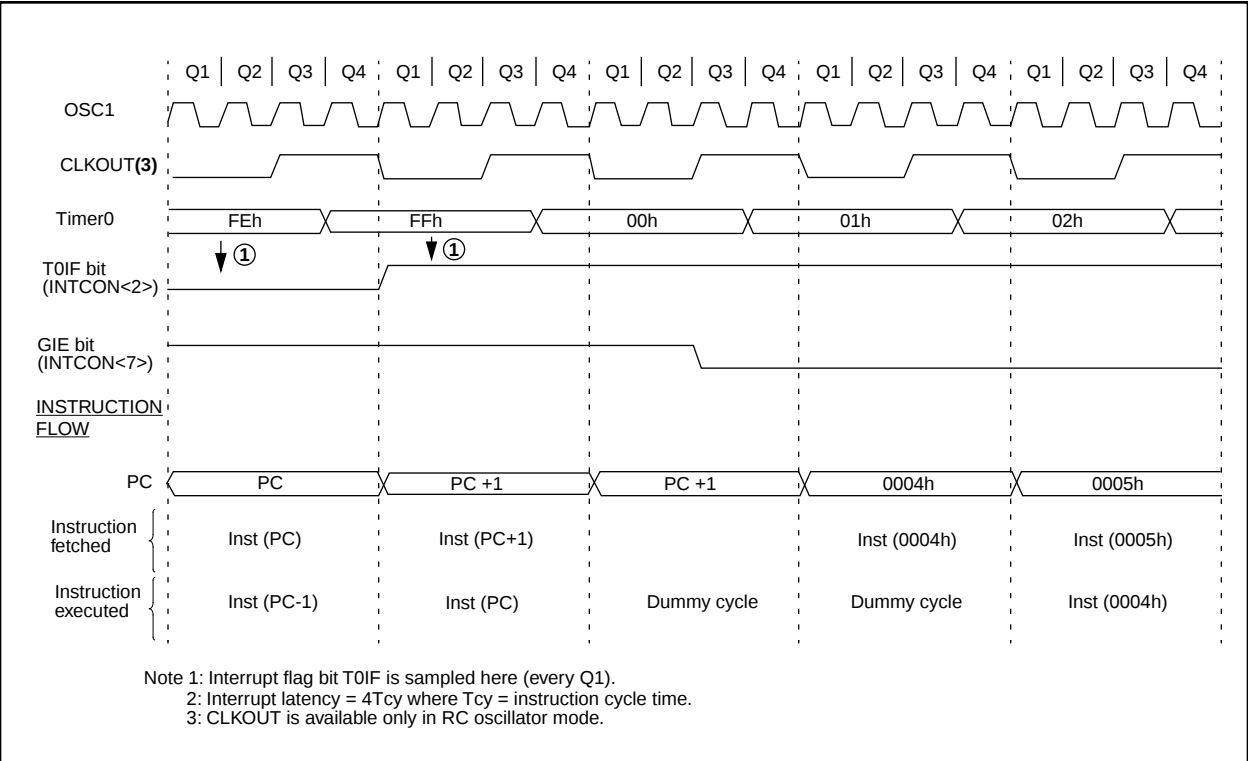


FIGURE 6-4: TIMER0 INTERRUPT TIMING



PIC16C71X

NOTES:

PIC16C71X

7.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-5. The source impedance (R_s) and the internal sampling switch (R_{ss}) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (R_{ss}) impedance varies over the device voltage (V_{DD}), Figure 7-5. The source impedance affects the offset voltage at the analog input (due to pin leakage current).

The maximum recommended impedance for analog sources is 10 k Ω . After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation calculates the acquisition time to within 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

EQUATION 7-1: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \cdot (1 - e^{(-T_{CAP}/CHOLD(RIC + R_{SS} + R_s)))}$$

Given: $V_{HOLD} = (V_{REF}/512)$, for 1/2 LSb resolution

The above equation reduces to:

$$T_{CAP} = -(51.2 \text{ pF})(1 \text{ k}\Omega + R_{SS} + R_s) \ln(1/511)$$

Example 7-1 shows the calculation of the minimum required acquisition time T_{ACQ} . This calculation is based on the following system assumptions.

CHOLD = 51.2 pF

$R_s = 10 \text{ k}\Omega$

1/2 LSb error

$V_{DD} = 5V \rightarrow R_{ss} = 7 \text{ k}\Omega$

Temp (application system max.) = 50°C

$V_{HOLD} = 0$ @ $t = 0$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0 T_{AD} delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 7-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$T_{ACQ} = \text{Amplifier Settling Time} +$

Holding Capacitor Charging Time +

Temperature Coefficient

$$T_{ACQ} = 5 \mu s + T_{CAP} + [(Temp - 25^\circ C)(0.05 \mu s/^\circ C)]$$

$$T_{CAP} = -CHOLD (RIC + R_{SS} + R_s) \ln(1/511)$$

$$-51.2 \text{ pF} (1 \text{ k}\Omega + 7 \text{ k}\Omega + 10 \text{ k}\Omega) \ln(0.0020)$$

$$-51.2 \text{ pF} (18 \text{ k}\Omega) \ln(0.0020)$$

$$-0.921 \mu s (-6.2364)$$

$$5.747 \mu s$$

$$T_{ACQ} = 5 \mu s + 5.747 \mu s + [(50^\circ C - 25^\circ C)(0.05 \mu s/^\circ C)]$$

$$10.747 \mu s + 1.25 \mu s$$

$$11.997 \mu s$$

FIGURE 7-5: ANALOG INPUT MODEL

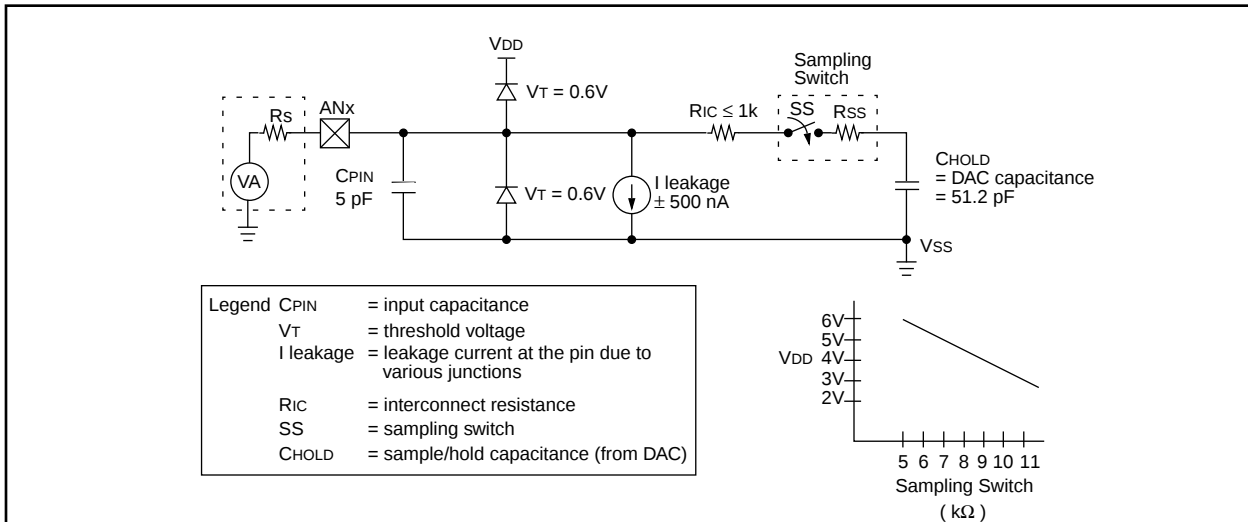


TABLE 8-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C710/71/711

Register	Power-on Reset, Brown-out Reset ⁽⁵⁾	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000h	0000h	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	---x 0000	---u 0000	---u uuuu
PORTB	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
ADRES	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	00-0 0000	00-0 0000	uu-u uuuu
OPTION	1111 1111	1111 1111	uuuu uuuu
TRISA	---1 1111	---1 1111	---u uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PCON ⁽⁴⁾	---- --0u	---- --uu	---- --uu
ADCON1	---- --00	---- --00	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-10 for reset value for specific condition.

4: The PCON register is not implemented on the PIC16C71.

5: Brown-out reset is not implemented on the PIC16C71.

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

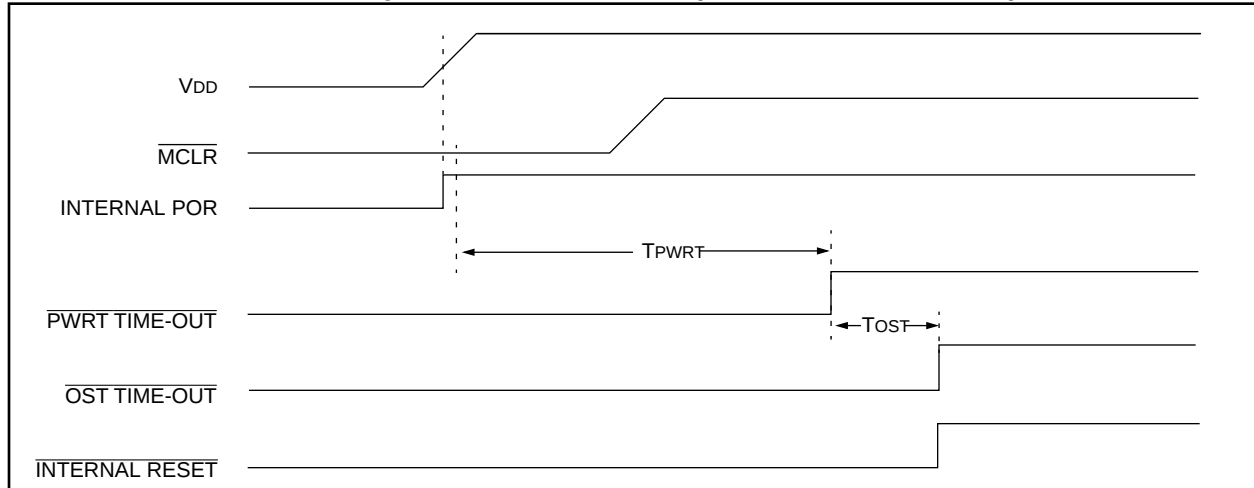


FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

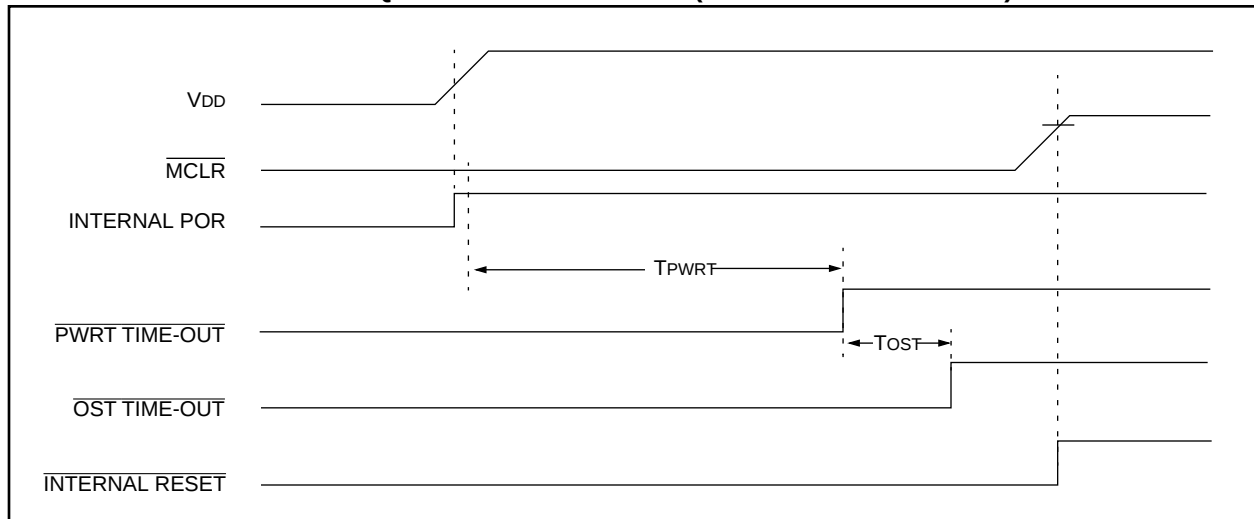
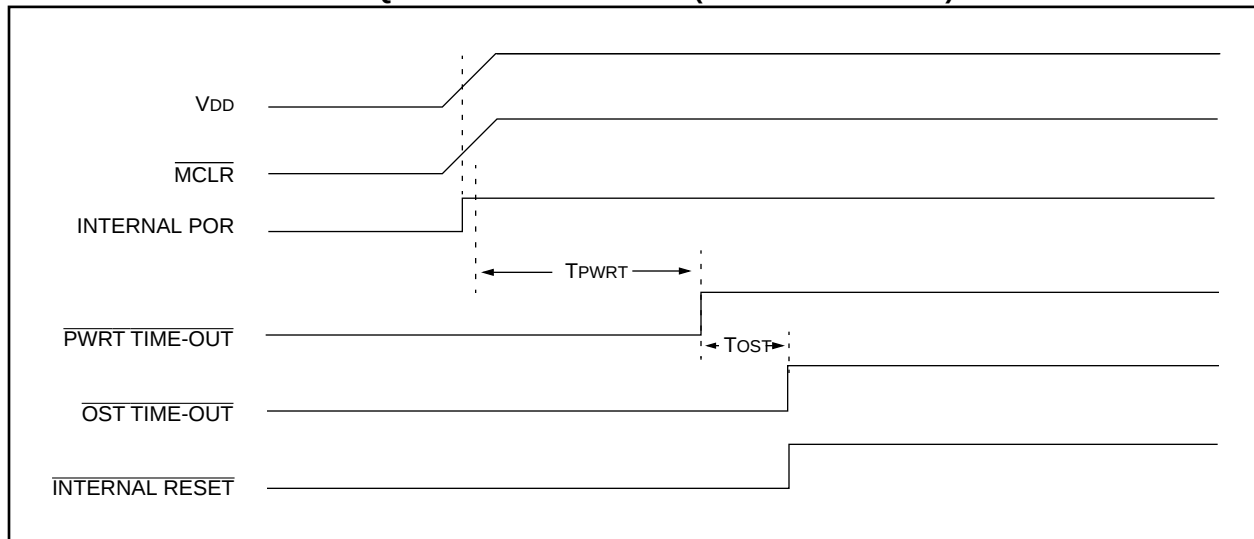


FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})



PIC16C71X

NOTES:

PIC16C71X

IORWF Inclusive OR W with f

Syntax:	[<i>label</i>] IORWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .OR. (f) $\rightarrow$ (dest)			
Status Affected:	$\bar{Z}$			
Encoding:	00	0100	dfff	ffff
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to dest

Example IORWF RESULT, 0

Before Instruction

RESULT = 0x13
W = 0x91

After Instruction

RESULT = 0x13
W = 0x93
Z = 1

MOVF Move f

Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) $\rightarrow$ (dest)			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write to dest

Example MOVF FSR, 0

After Instruction

W = value in FSR register
Z = 1

MOVLW Move Literal to W

Syntax:	[<i>label</i>] MOVLW k			
Operands:	$0 \leq k \leq 255$			
Operation:	$k \rightarrow (W)$			
Status Affected:	None			
Encoding:	11	00xx	kkkk	kkkk
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process data	Write to W

Example

MOVLW 0x5A

After Instruction

W = 0x5A

MOVWF Move W to f

Syntax:	[<i>label</i>] MOVWF f			
Operands:	$0 \leq f \leq 127$			
Operation:	(W) $\rightarrow$ (f)			
Status Affected:	None			
Encoding:	00	0000	1fff	ffff
Description:	Move data from W register to register 'f'.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write register 'f'

Example

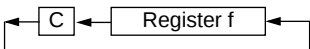
MOVWF OPTION_REG

Before Instruction

OPTION = 0xFF
W = 0x4F

After Instruction

OPTION = 0x4F
W = 0x4F

RLF		Rotate Left f through Carry							
Syntax:	[<i>label</i>] RLF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	See description below								
Status Affected:	C								
Encoding:	<table><tr><td>00</td><td>1101</td><td>dfff</td><td>ffff</td></tr></table>					00	1101	dfff	ffff
00	1101	dfff	ffff						
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'. 								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write to dest					

Example

RLF REG1, 0

Before Instruction

REG1 = 1110 0110

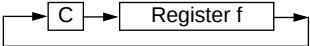
C = 0

After Instruction

REG1 = 1110 0110

W = 1100 1100

C = 1

RRF		Rotate Right f through Carry							
Syntax:	[<i>label</i>] RRF f,d								
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]								
Operation:	See description below								
Status Affected:	C								
Encoding:	<table><tr><td>00</td><td>1100</td><td>dfff</td><td>ffff</td></tr></table>					00	1100	dfff	ffff
00	1100	dfff	ffff						
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. 								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write to dest					

Example

RRF REG1, 0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 0111 0011

C = 0

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Applicable Devices	710	71	711	715
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11.4 Timing Parameter Symbolology

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 11-1: LOAD CONDITIONS

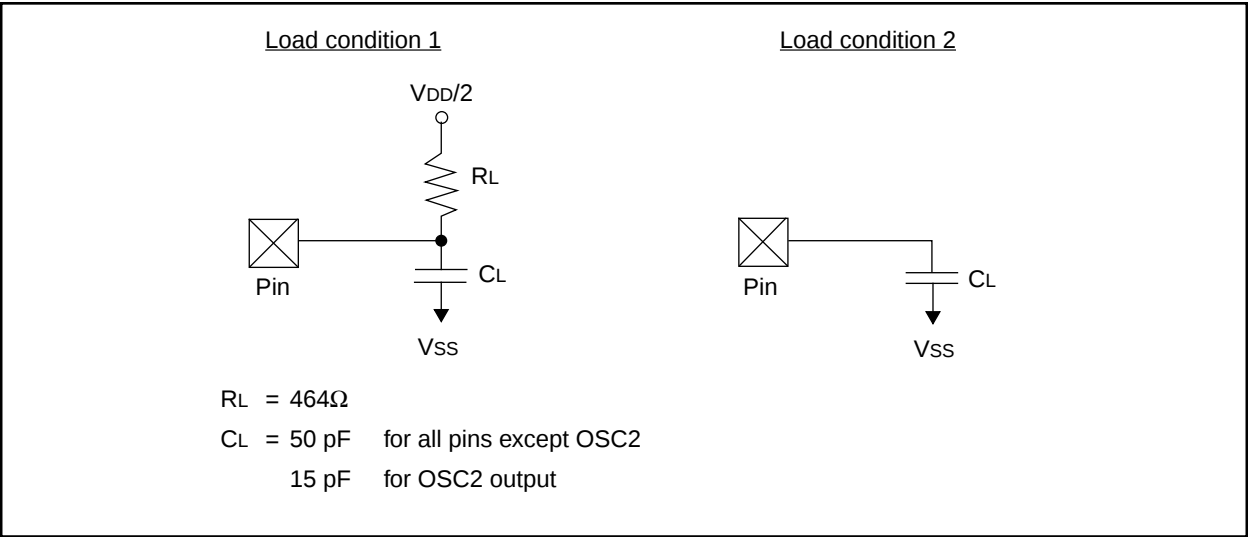


TABLE 11-6: A/D CONVERTER CHARACTERISTICS:
PIC16C710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C710/711-10 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C710/711-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16LC710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	8-bits	bit	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A02	EABS	Absolute error	—	—	$< \pm 1$	LSb	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A03	EIL	Integral linearity error	—	—	$< \pm 1$	LSb	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A04	EDL	Differential linearity error	—	—	$< \pm 1$	LSb	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A05	EFS	Full scale error	—	—	$< \pm 1$	LSb	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A06	EOFF	Offset error	—	—	$< \pm 1$	LSb	$V_{REF} = V_{DD}$, $V_{SS} \leq AIN \leq V_{REF}$
A10	—	Monotonicity	—	guaranteed	—	—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	VREF	Reference voltage	2.5V	—	$V_{DD} + 0.3$	V	
A25	VAIN	Analog input voltage	$V_{SS} - 0.3$	—	$V_{REF} + 0.3$	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	k Ω	
A40	IAD	A/D conversion current (V_{DD})	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	—	1000	μA	During VAIN acquisition. Based on differential of V_{HOLD} to V_{AIN} . To charge $CHOLD$ see Section 7.1. During A/D Conversion cycle
			—	—	10	μA	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current.

The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

FIGURE 13-6: TIMER0 CLOCK TIMINGS

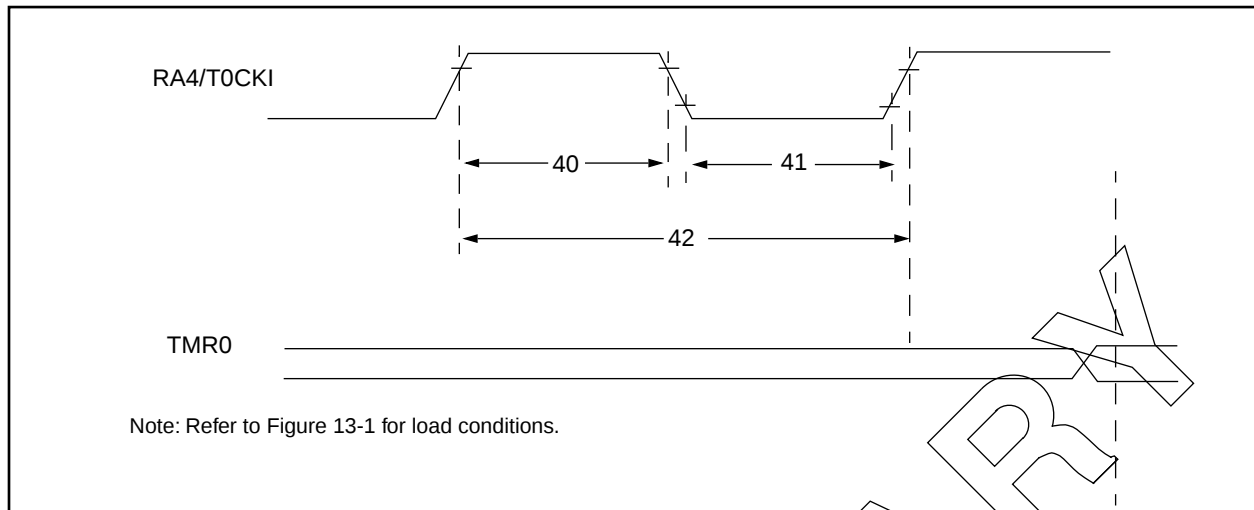


TABLE 13-5: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	ns	
			With Prescaler	10^*	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	ns	
			With Prescaler	10^*	—	ns	
42	Tt0P	T0CKI Period	Greater of: $20\mu s$ or $\frac{T_{CY} + 40^*}{N}$		—	ns	N = prescale value (1, 2, 4,..., 256)
48	Tcke2tmr1	Delay from external clock edge to timer increment	$2T_{osc}$	—	$7T_{osc}$	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-18: TYPICAL I_{DD} vs. CAPACITANCE @ 500 kHz (RC MODE)

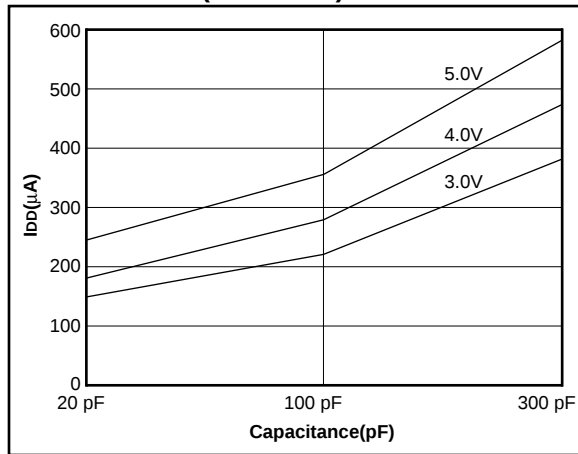


TABLE 14-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average	
		Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5V$.

FIGURE 14-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. V_{DD}

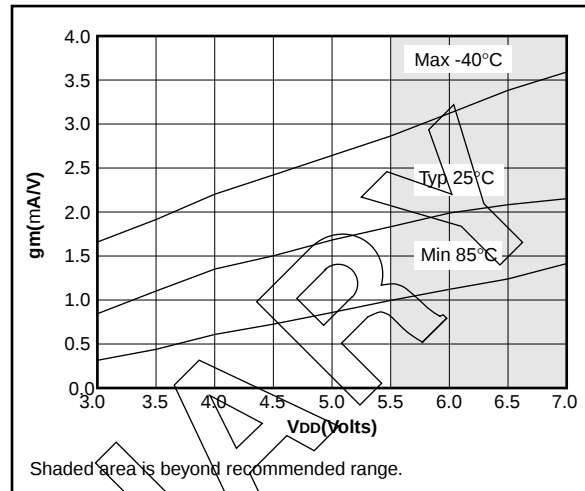


FIGURE 14-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. V_{DD}

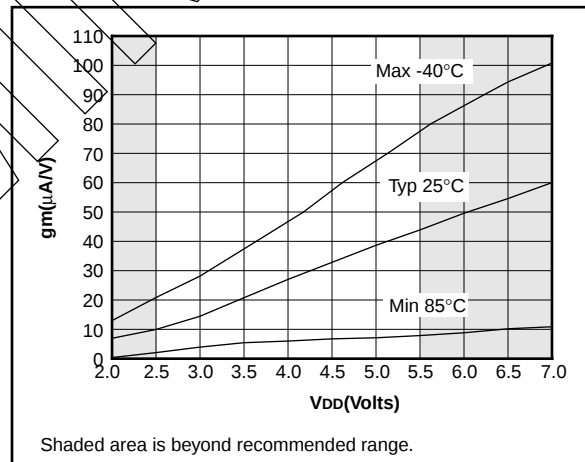
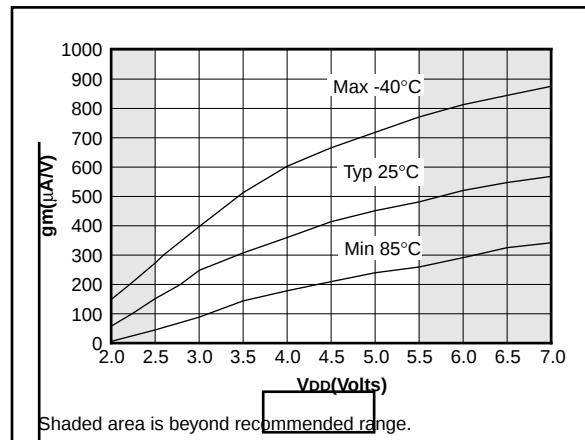


FIGURE 14-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. V_{DD}



15.2 DC Characteristics: PIC16LC71-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0	-	6.0	V	XT, RC, and LP osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.4	2.5	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A				15	32	μA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3)	IPD	-	5	20	μA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021				0.6	9	μA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A				0.6	12	μA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

PIC16C71X

Applicable Devices 710 71 711 715

15.3 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial) PIC16LC71-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030 D031 D032 D033	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$, OSC1 (in RC mode) OSC1 (in XT, HS and LP)	V_{IL}	V_{SS}	-	0.15V 0.8V 0.2V _{DD} 0.3V _{DD}	V	For entire V_{DD} range $4.5 \leq V_{DD} \leq 5.5\text{V}$ Note1
D040 D040A D041 D042 D042A D043	Input High Voltage I/O ports (Note 4) with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$, RB0/INT OSC1 (XT, HS and LP) OSC1 (in RC mode)	V_{IH}	2.0 0.25V _{DD} + 0.8V 0.85V _{DD} 0.85V _{DD} 0.7V _{DD} 0.9V _{DD}	- - - - - -	V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V	$4.5 \leq V_{DD} \leq 5.5\text{V}$ For entire V_{DD} range For entire V_{DD} range Note1
D070	PORTB weak pull-up current	IPURB	50	250	†400	μA	$V_{DD} = 5\text{V}$, $V_{PIN} = V_{SS}$
D060 D061 D063	Input Leakage Current (Notes 2, 3) I/O ports $\overline{\text{MCLR}}$, RA4/T0CKI OSC1	I_{IL}	- - -	- - -	±1 ±5 ±5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080 D083	Output Low Voltage I/O ports OSC2/CLKOUT (RC osc config)	V_{OL}	- -	- -	0.6 0.6	V	$I_{OL} = 8.5\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $I_{OL} = 1.6\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D090 D092	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (RC osc config)	V_{OH}	$V_{DD} - 0.7$ $V_{DD} - 0.7$	- -	- -	V	$I_{OH} = -3.0\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $I_{OH} = -1.3\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D130*	Open-Drain High Voltage	V_{OD}	-	-	14	V	RA4 pin

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.
- 2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 15-5: TIMER0 EXTERNAL CLOCK TIMINGS

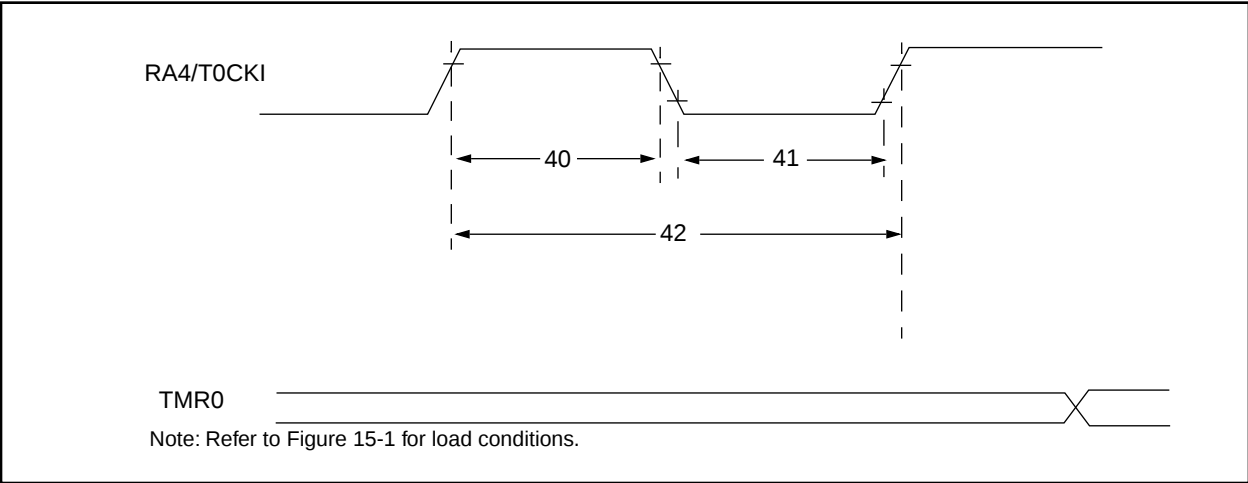


TABLE 15-5: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	Must also meet parameter 42
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period	No Prescaler	$T_{CY} + 40$	—	—	ns	N = prescale value (2, 4,..., 256)
			With Prescaler	Greater of: $20 \text{ ns or } \frac{T_{CY} + 40}{N}$				

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C71X

$\overline{TO}$ bit	17
TOSE bit	18
TRISA Register	14, 16, 25
TRISB Register	14, 16, 27
Two's Complement	7

U

Upward Compatibility	3
UV Erasable Devices	5

W

W Register	
ALU	7
Wake-up from SLEEP	66
Watchdog Timer (WDT)	47, 52, 56, 65
WDT	56
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WDT Period	65
WDTE bit	47, 48

Z

Z bit	17
Zero bit	7

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PIC16C71X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX		Examples
					Pattern:	QTP, SQTP, Code or Special Requirements
					Package:	JW = Windowed Cerdip SO = SOIC SP = Skinny plastic dip P = PDIP SS = SSOP
					Temperature Range:	- = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C
					Frequency Range:	04 = 200 kHz (PIC16C7X-04) 04 = 4 MHz 10 = 10 MHz 20 = 20 MHz
					Device	PIC16C7X :V _{DD} range 4.0V to 6.0V PIC16C7XT :V _{DD} range 4.0V to 6.0V (Tape/Reel) PIC16LC7X :V _{DD} range 2.5V to 6.0V PIC16LC7XT :V _{DD} range 2.5V to 6.0V (Tape/Reel)

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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