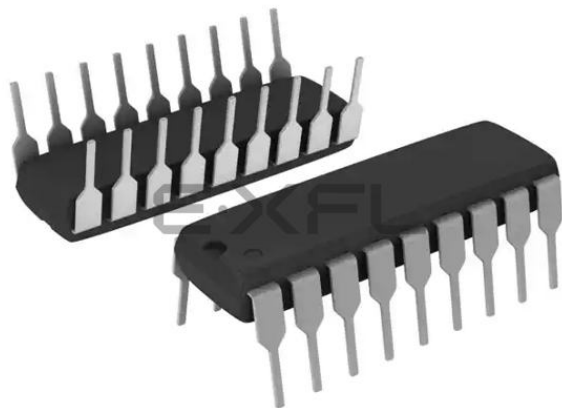




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c711-20-p

PIC16C71X

FIGURE 3-1: PIC16C71X BLOCK DIAGRAM

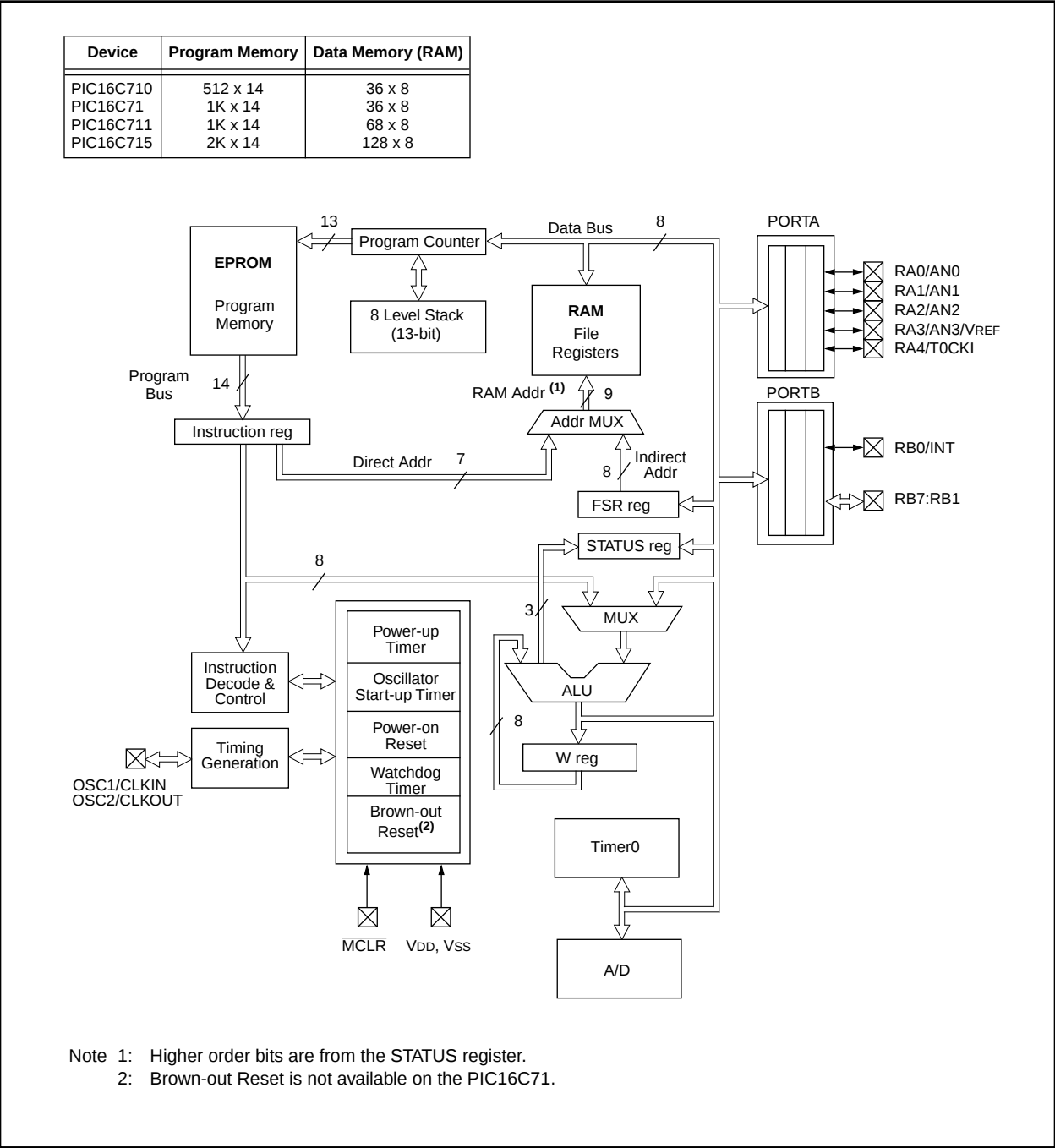


TABLE 3-1: PIC16C710/71/711/715 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SSOP Pin# ⁽⁴⁾	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	16	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	4	4	4	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
RA0/AN0	17	19	17	I/O	TTL	PORTA is a bi-directional I/O port. RA0 can also be analog input0 RA1 can also be analog input1 RA2 can also be analog input2 RA3 can also be analog input3 or analog reference voltage RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA1/AN1	18	20	18	I/O	TTL	
RA2/AN2	1	1	1	I/O	TTL	
RA3/AN3/VREF	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	
RB0/INT	6	7	6	I/O	TTL/ST ⁽¹⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0 can also be the external interrupt pin. Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.
RB1	7	8	7	I/O	TTL	
RB2	8	9	8	I/O	TTL	
RB3	9	10	9	I/O	TTL	
RB4	10	11	10	I/O	TTL	
RB5	11	12	11	I/O	TTL	
RB6	12	13	12	I/O	TTL/ST ⁽²⁾	
RB7	13	14	13	I/O	TTL/ST ⁽²⁾	
VSS	5	4, 6	5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 Note 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 Note 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
 Note 4: The PIC16C71 is not available in SSOP package.

PIC16C71X

FIGURE 4-5: PIC16C711 REGISTER FILE MAP

File Address			File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h		PCON	87h
08h	ADCON0	ADCON1	88h
09h	ADRES	ADRES	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	General Purpose Register	General Purpose Register	8Ch
		Mapped in Bank 0 ⁽²⁾	
4Fh			CFh
50h			D0h
7Fh			FFh

Bank 0 Bank 1

 Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.
 Note 2: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

FIGURE 4-6: PIC16C715 REGISTER FILE MAP

File Address			File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh	ADRES		9Eh
1Fh	ADCON0	ADCON1	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
7Fh	Bank 0	Bank 1	FFh

 Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

PIC16C71X

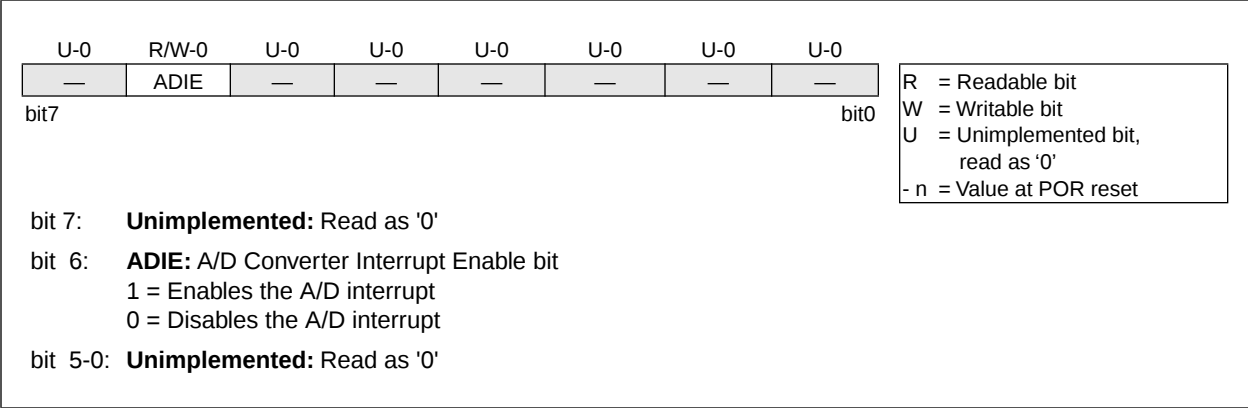
4.2.2.4 PIE1 REGISTER

Applicable Devices	710	71	711	715
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Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

This register contains the individual enable bits for the Peripheral interrupts.

FIGURE 4-10: PIE1 REGISTER (ADDRESS 8Ch)



PIC16C71X

FIGURE 7-2: ADCON0 REGISTER (ADDRESS 1Fh), PIC16C715

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	—	CHS1	CHS0	GO/DONE	—	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
 00 = Fosc/2
 01 = Fosc/8
 10 = Fosc/32
 11 = FRC (clock derived from an RC oscillation)

bit 5: **Unused**

bit 6-3: **CHS1:CHS0:** Analog Channel Select bits
 000 = channel 0, (RA0/AN0)
 001 = channel 1, (RA1/AN1)
 010 = channel 2, (RA2/AN2)
 011 = channel 3, (RA3/AN3)
 100 = channel 0, (RA0/AN0)
 101 = channel 1, (RA1/AN1)
 110 = channel 2, (RA2/AN2)
 111 = channel 3, (RA3/AN3)

bit 2: **GO/DONE:** A/D Conversion Status bit
 If ADON = 1
 1 = A/D conversion in progress (setting this bit starts the A/D conversion)
 0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented:** Read as '0'

bit 0: **ADON:** A/D On bit
 1 = A/D converter module is operating
 0 = A/D converter module is shutoff and consumes no operating current

FIGURE 7-3: ADCON1 REGISTER, PIC16C710/711 (ADDRESS 88h), PIC16C715 (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PCFG1	PCFG0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1-0: **PCFG1:PCFG0:** A/D Port Configuration Control bits

PCFG1:PCFG0	RA1 & RA0	RA2	RA3	VREF
00	A	A	A	VDD
01	A	A	VREF	RA3
10	A	D	D	VDD
11	D	D	D	VDD

A = Analog input
D = Digital I/O

PIC16C71X

7.4 A/D Conversions

Example 7-2 shows how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 pin (channel 0).

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

EXAMPLE 7-2: A/D CONVERSION

```
BSF    STATUS, RP0      ; Select Bank 1
CLRF   ADCON1           ; Configure A/D inputs
BCF    STATUS, RP0      ; Select Bank 0
MOVLW  0xC1             ; RC Clock, A/D is on, Channel 0 is selected
MOVWF  ADCON0           ;
BSF    INTCON, ADIE      ; Enable A/D Interrupt
BSF    INTCON, GIE       ; Enable all interrupts
;
; Ensure that the required sampling time for the selected input channel has elapsed.
; Then the conversion may be started.
;
BSF    ADCON0, GO        ; Start A/D Conversion
:      ; The ADIF bit will be set and the GO/DONE bit
:      ; is cleared upon completion of the A/D Conversion.
```

PIC16C71X

TABLE 7-3: REGISTERS/BITS ASSOCIATED WITH A/D, PIC16C710/71/711

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh	INTCON	GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
89h	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
08h	ADCON0	ADCS1	ADCS0	—	CHS1	CHS0	GO/DONE	ADIF	ADON	00-0 0000	00-0 0000
88h	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	PORTA Data Direction Register					---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

TABLE 7-4: REGISTERS/BITS ASSOCIATED WITH A/D, PIC16C715

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	ADIE	—	—	—	—	—	—	-0-- ----	-0-- ----
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	---- --00	---- --00
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

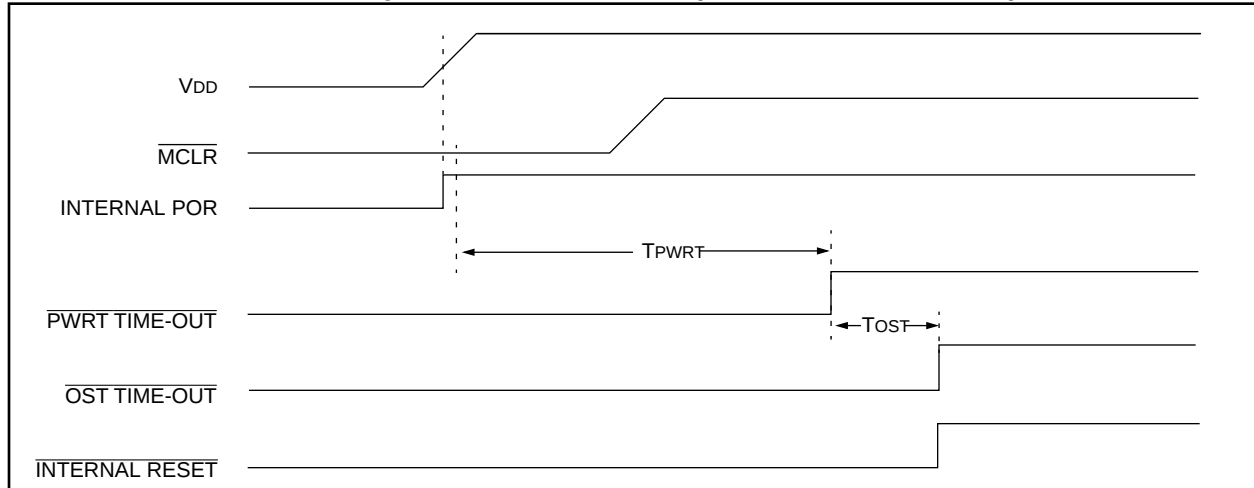


FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

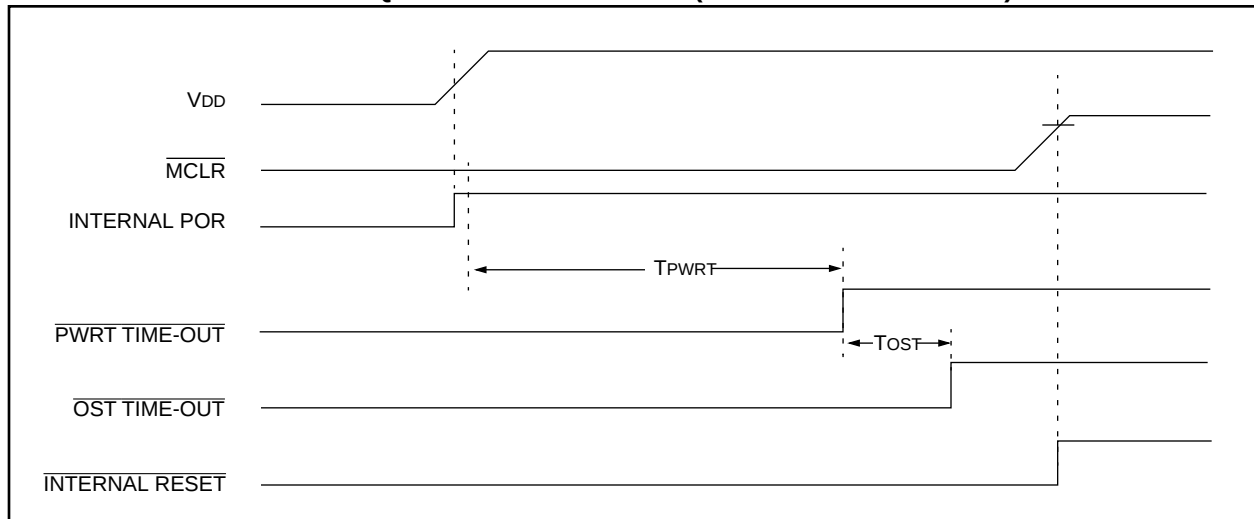
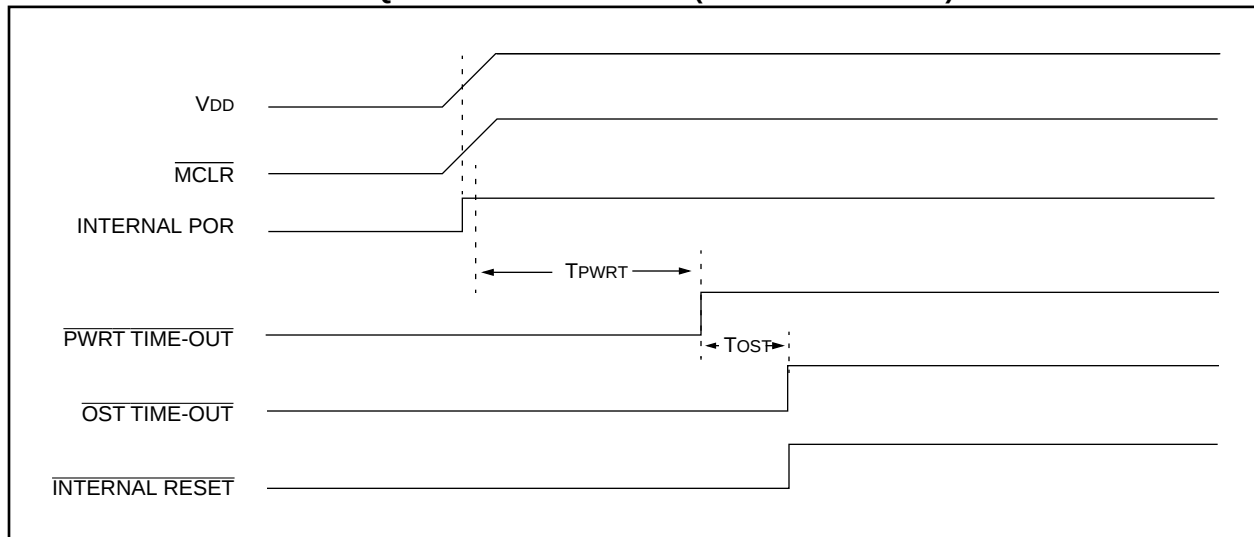


FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})



8.7 Watchdog Timer (WDT)

Applicable Devices	710	71	711	715
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The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 8.1).

8.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be

assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

8.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 8-20: WATCHDOG TIMER BLOCK DIAGRAM

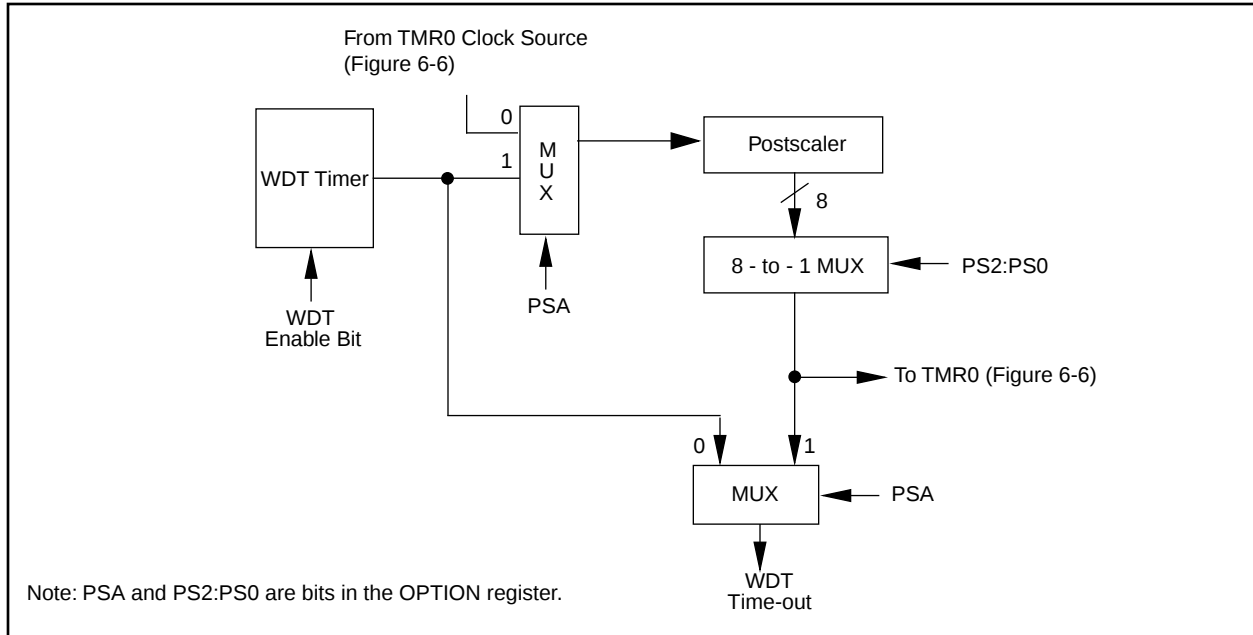


FIGURE 8-21: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h,181h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 8-1, Figure 8-2 and Figure 8-3 for operation of these bits.

Applicable Devices	710	71	711	715
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FIGURE 12-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

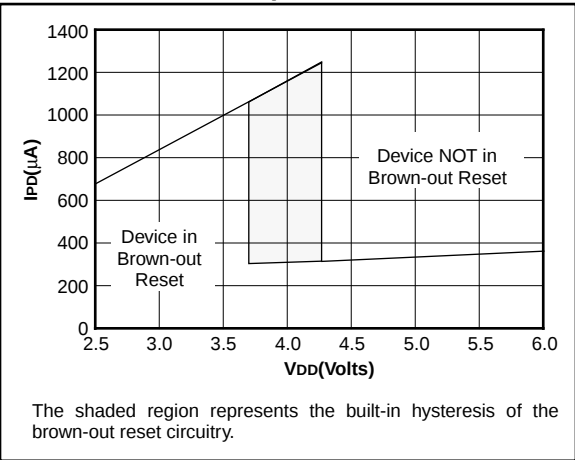


FIGURE 12-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

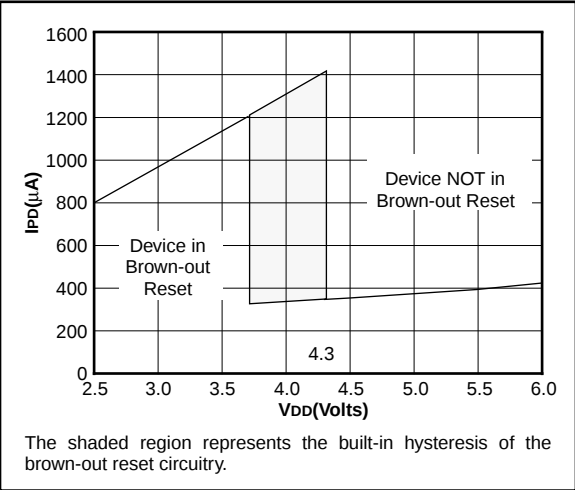


FIGURE 12-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

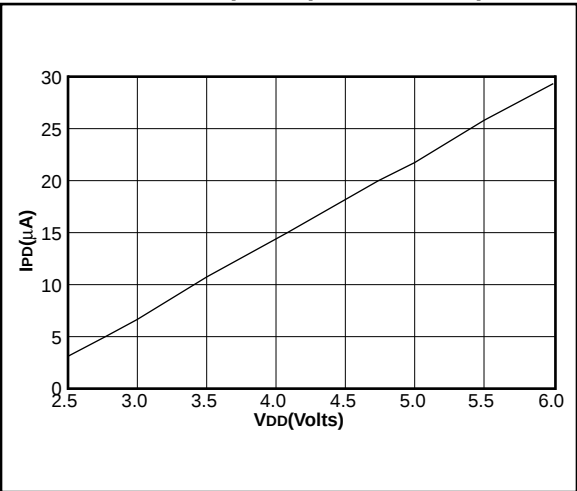
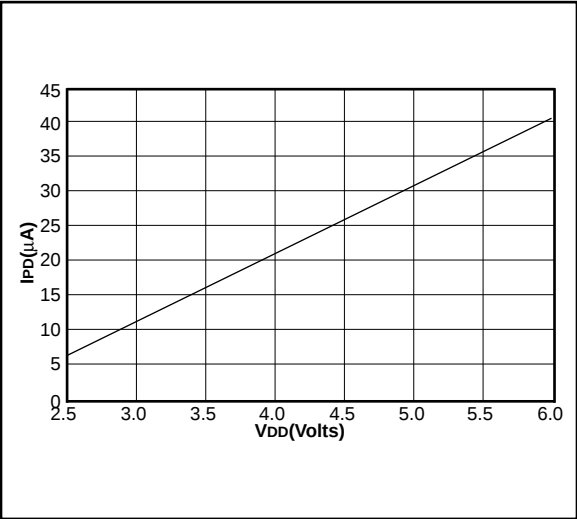


FIGURE 12-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 12-16: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

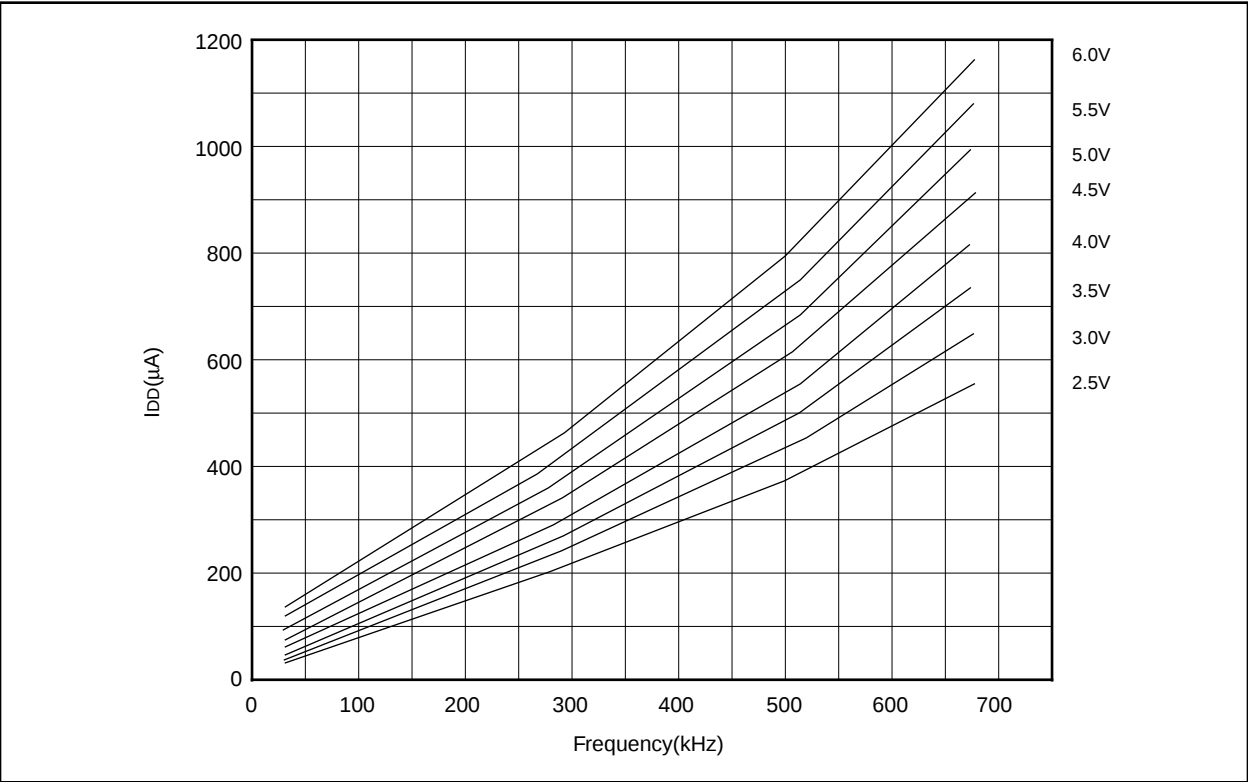
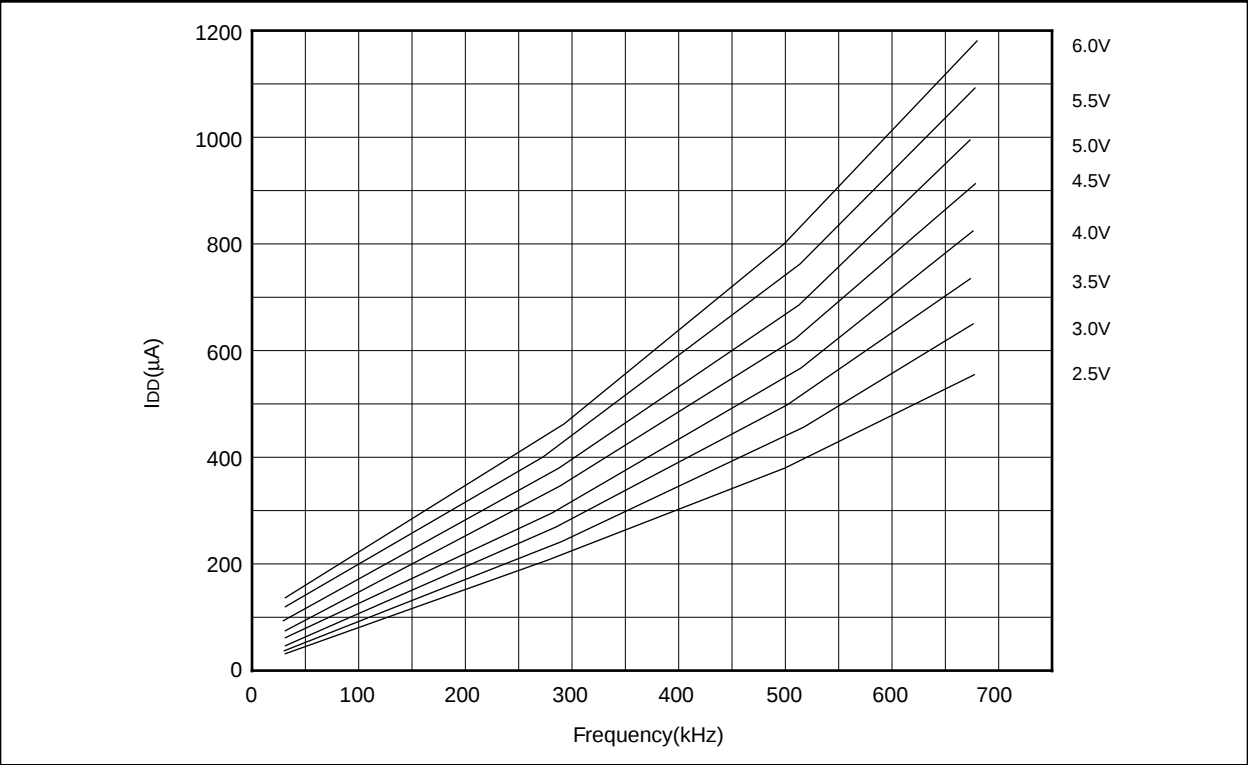


FIGURE 12-17: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 13-7: A/D CONVERSION TIMING

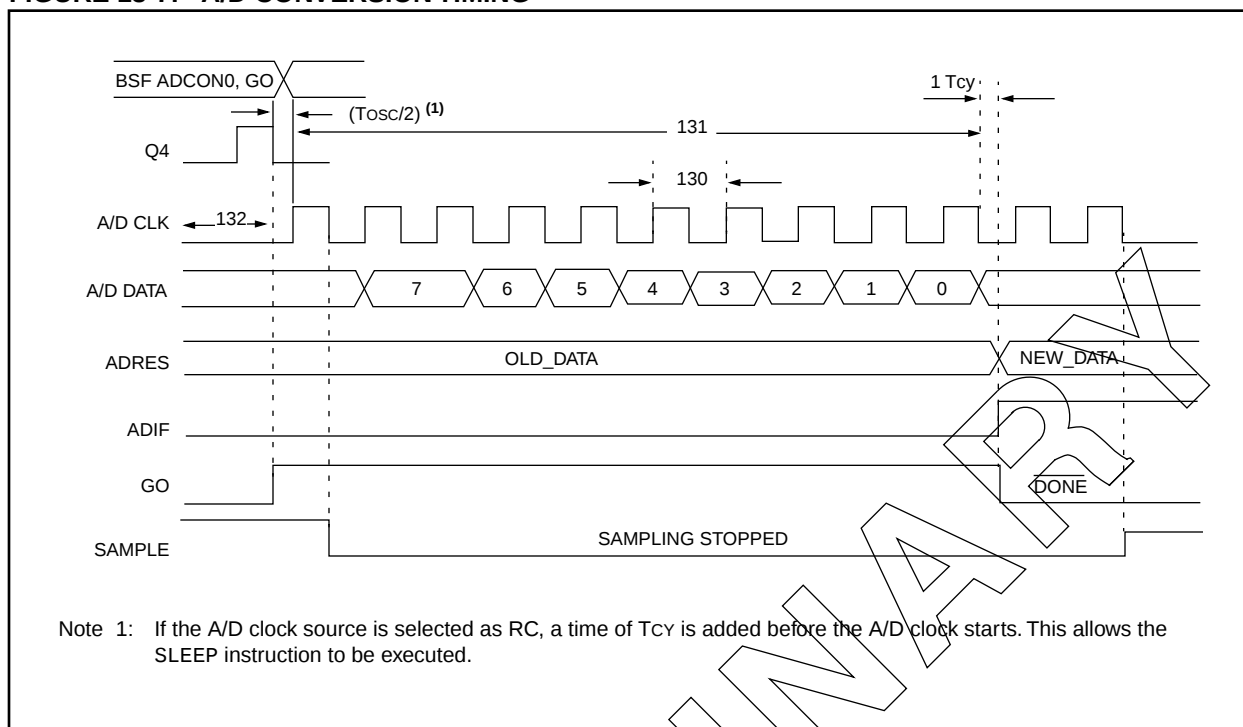


TABLE 13-8: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	1.6	—	—	μs	VREF ≥ 3.0V
130	TAD	A/D Internal RC Oscillator source	2.0	—	—	μs	VREF full range
			3.0	6.0	9.0	μs	ADCS1:ADCS0 = 11 (RC oscillator source)
			2.0	4.0	6.0	μs	PIC16LC715, VDD = 3.0V
							PIC16C715
131	Tcnv	Conversion time (not including S/H time). Note 1	—	9.5TAD	—	—	
132	TACQ	Acquisition time	Note 2	20	—	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{cy} cycle.

Applicable Devices	710	71	711	715
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14.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C715

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 14-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

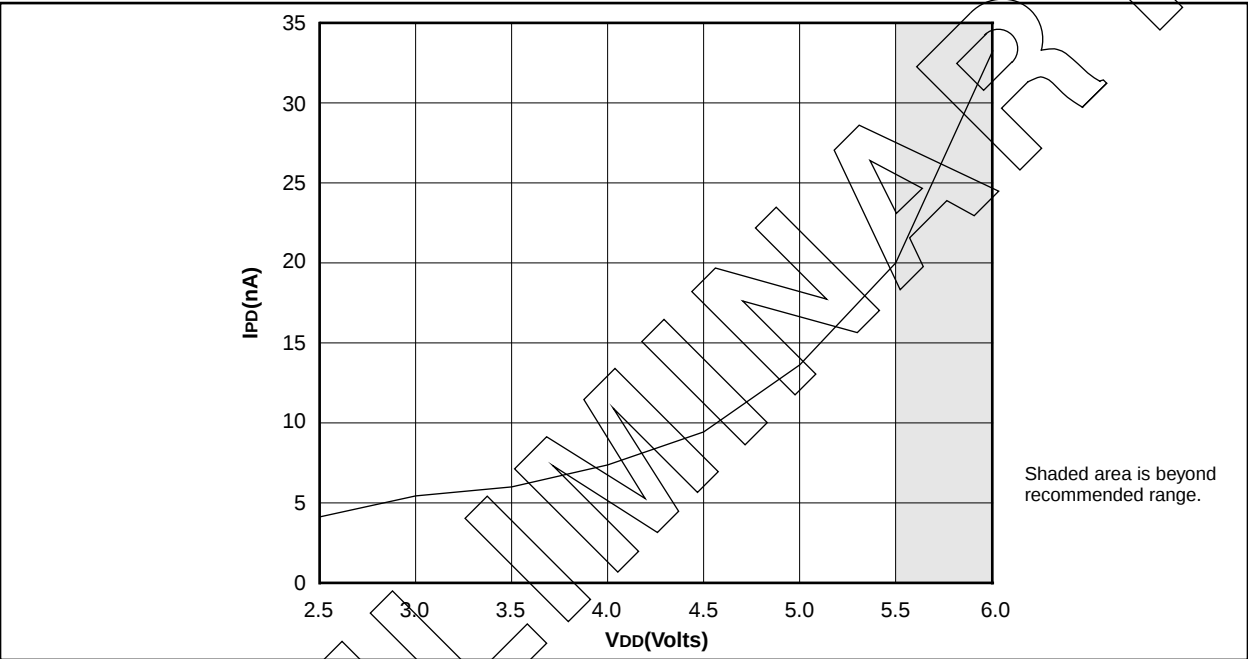


FIGURE 14-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)

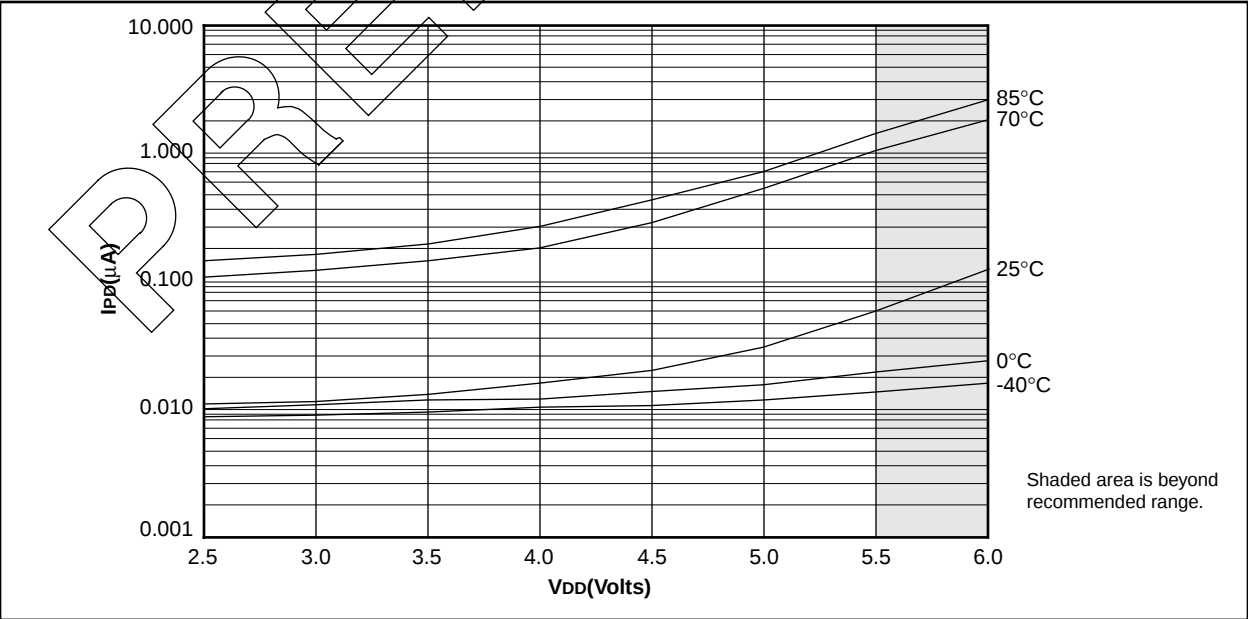


FIGURE 16-7: MAXIMUM IPD vs. VDD
WATCHDOG DISABLED

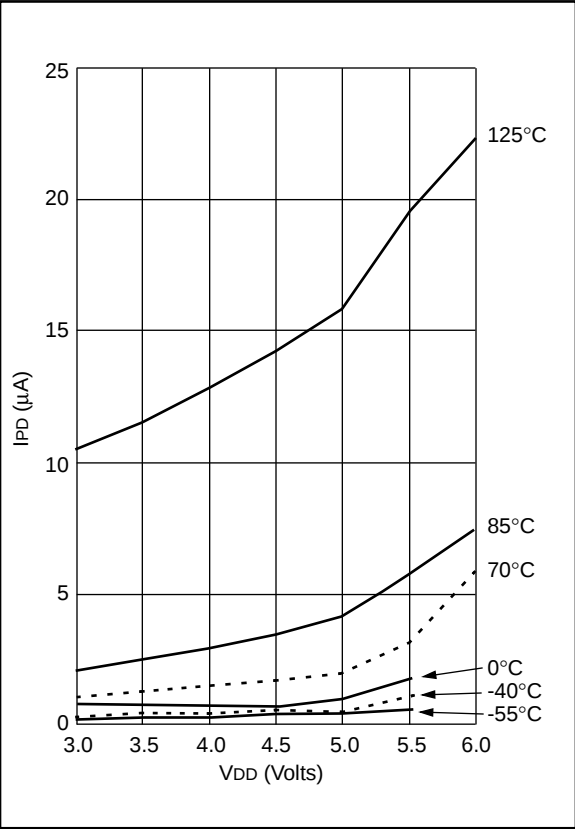


FIGURE 16-8: MAXIMUM IPD vs. VDD
WATCHDOG ENABLED

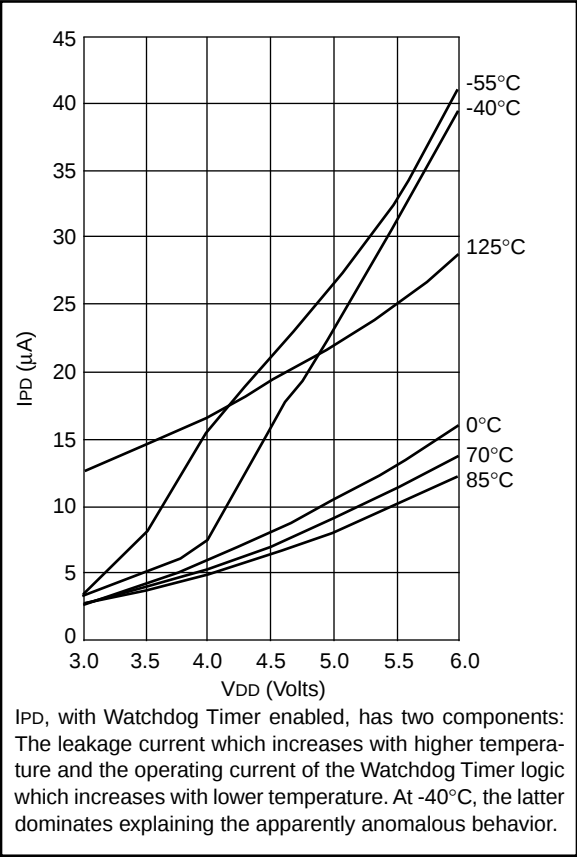
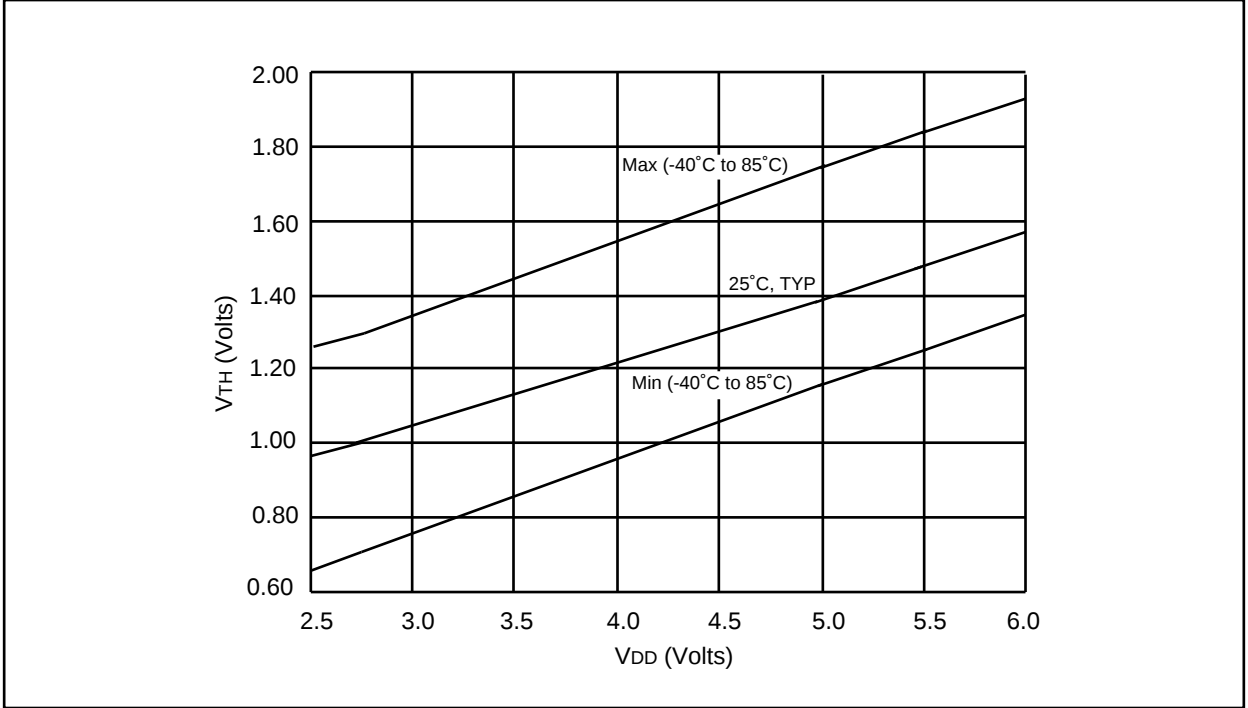


FIGURE 16-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD



Data based on matrix samples. See first page of this section for details.

PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 16-14: MAXIMUM I_{DD} vs. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)

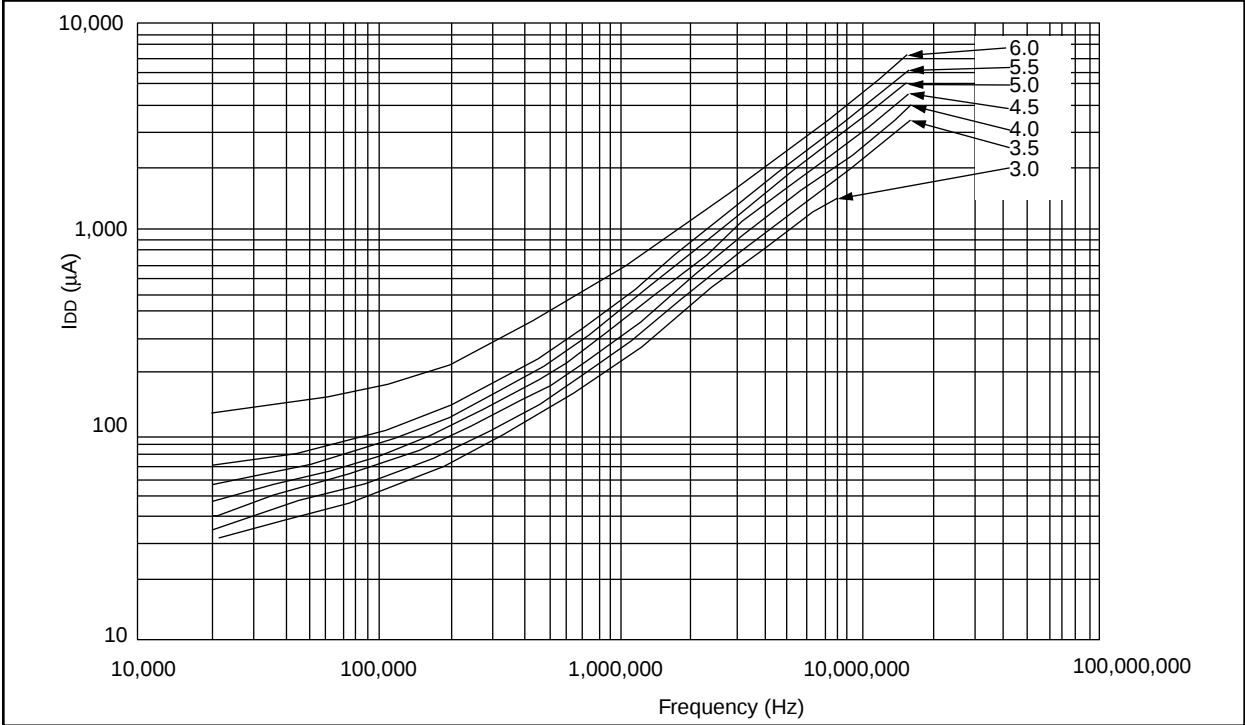


FIGURE 16-15: WDT TIMER TIME-OUT PERIOD vs. V_{DD}

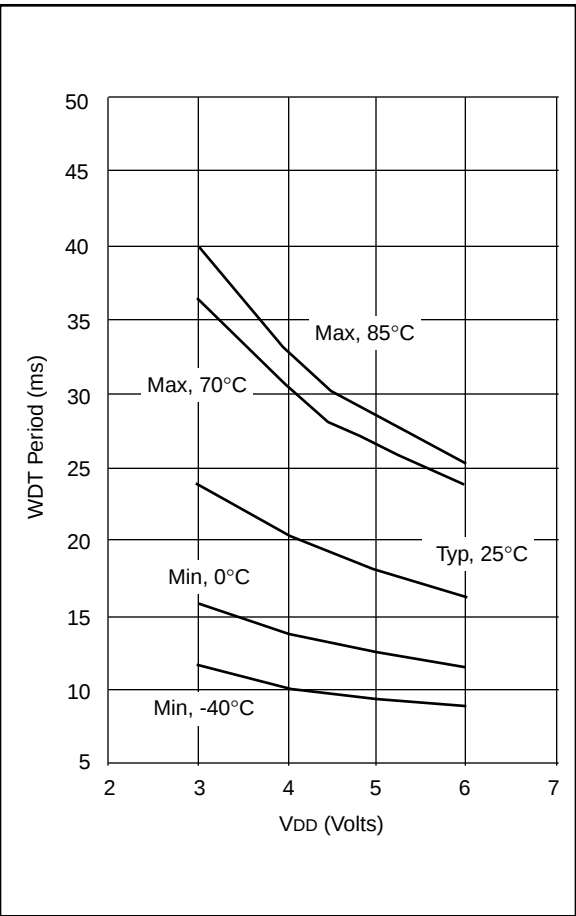
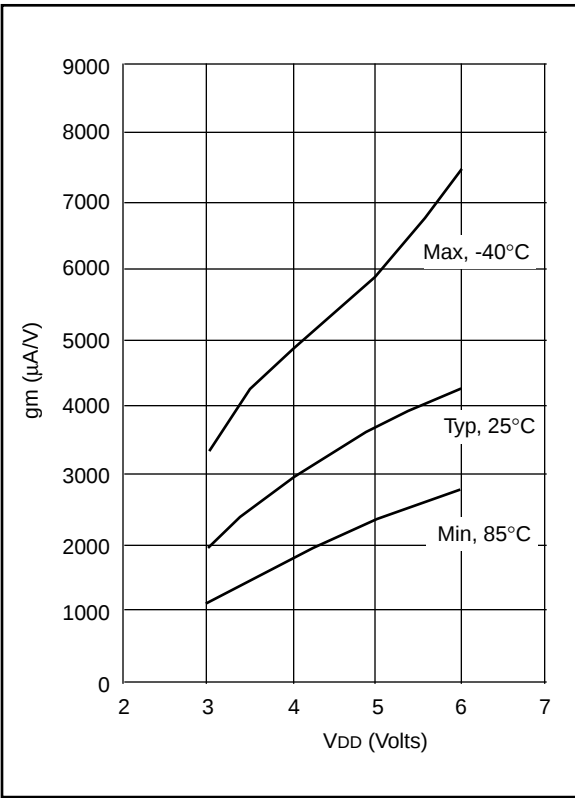


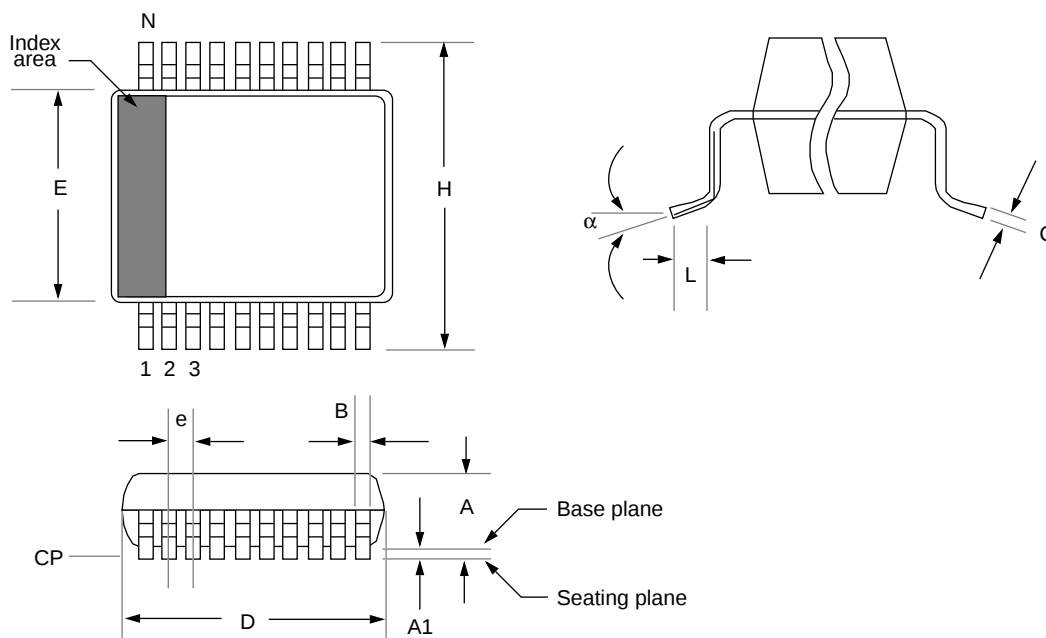
FIGURE 16-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. V_{DD}



Data based on matrix samples. See first page of this section for details.

PIC16C71X

17.4 20-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)



Package Group: Plastic SSOP						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	7.070	7.330		0.278	0.289	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	Reference	0.026	0.026	Reference
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	20	20		20	20	
CP	-	0.102		-	0.004	

Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.

3: This outline conforms to JEDEC MS-026.

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PIC16C71X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX		Examples
					Pattern:	QTP, SQTP, Code or Special Requirements
					Package:	JW = Windowed Cerdip SO = SOIC SP = Skinny plastic dip P = PDIP SS = SSOP
					Temperature Range:	- = 0°C to +70°C I = -40°C to +85°C E = -40°C to +125°C
					Frequency Range:	04 = 200 kHz (PIC16C7X-04) 04 = 4 MHz 10 = 10 MHz 20 = 20 MHz
					Device	PIC16C7X :V _{DD} range 4.0V to 6.0V PIC16C7XT :V _{DD} range 4.0V to 6.0V (Tape/Reel) PIC16LC7X :V _{DD} range 2.5V to 6.0V PIC16LC7XT :V _{DD} range 2.5V to 6.0V (Tape/Reel)

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

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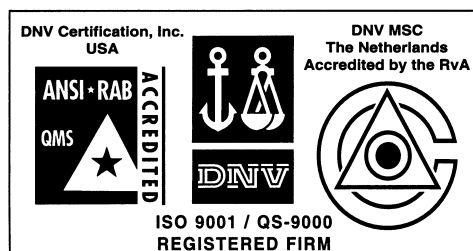
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