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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

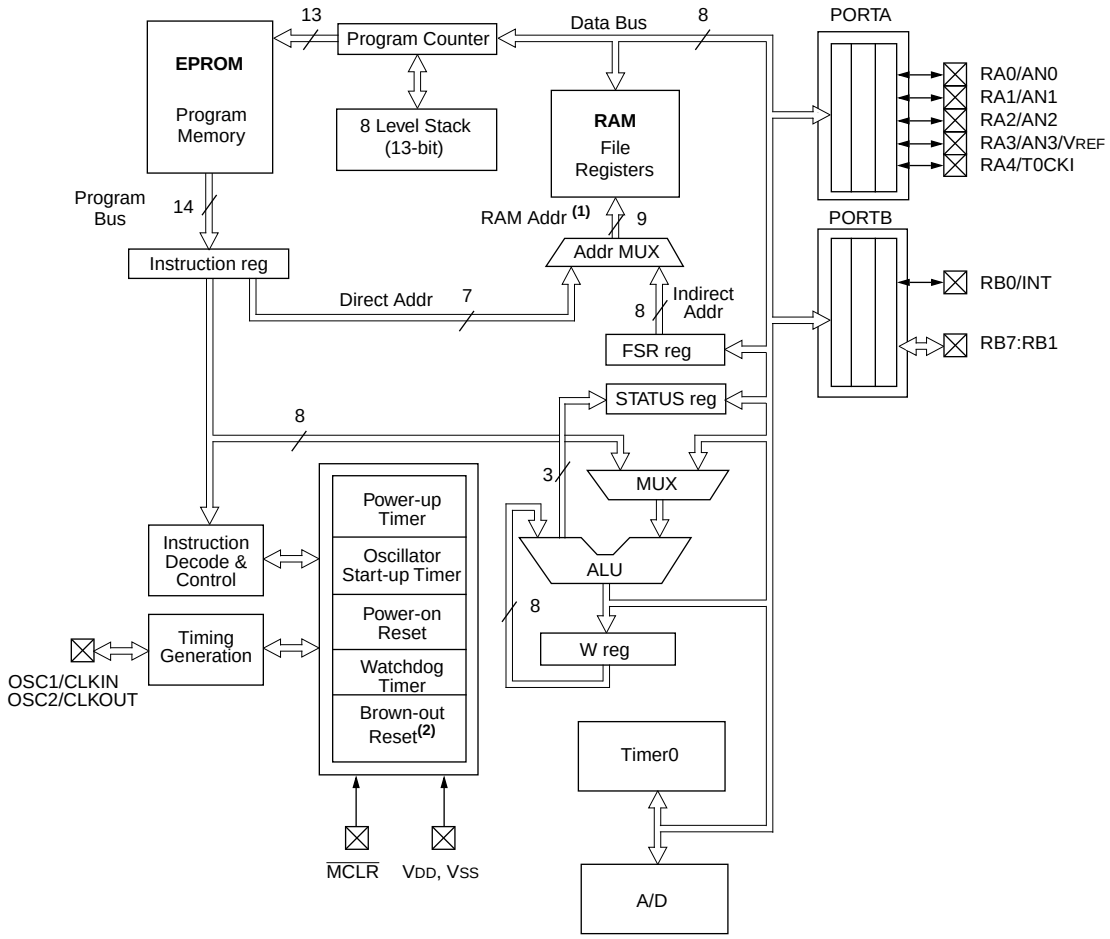
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c711-20-ss

NOTES:

FIGURE 3-1: PIC16C71X BLOCK DIAGRAM

Device	Program Memory	Data Memory (RAM)
PIC16C710	512 x 14	36 x 8
PIC16C71	1K x 14	36 x 8
PIC16C711	1K x 14	68 x 8
PIC16C715	2K x 14	128 x 8



Note 1: Higher order bits are from the STATUS register.
2: Brown-out Reset is not available on the PIC16C71.

NOTES:

8.0 SPECIAL FEATURES OF THE CPU

Applicable Devices	710	71	711	715

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR) (PIC16C710/711/715)
  - Parity Error Reset (PER) (PIC16C715)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 8-1: CONFIGURATION WORD FOR PIC16C71

—	—	—	—	—	—	—	—	—	CP0	PWRTE	WDTE	FOSC1	FOSC0

bit13 bit0

Register: CONFIG
Address 2007h

bit 13-5: **Unimplemented:** Read as '1'

bit 4: **CP0:** Code protection bit
1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 3: **PWRTE:** Power-up Timer Enable bit
1 = Power-up Timer enabled
0 = Power-up Timer disabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

8.4.5 TIME-OUT SEQUENCE

Applicable Devices	710	71	711	715

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 8-11, Figure 8-12, and Figure 8-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 8-12). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 8-10 and Table 8-11 show the reset conditions for some special function registers, while Table 8-12 and Table 8-13 show the reset conditions for all the registers.

8.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices	710	71	711	715

The Power Control/Status Register, PCON has up to two bits, depending upon the device.

Bit0 is Brown-out Reset Status bit, $\overline{BOR}$. Bit $\overline{BOR}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred. The $\overline{BOR}$ bit is a "Don't Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

For the PIC16C715, bit2 is $\overline{PER}$ (Parity Error Reset). It is cleared on a Parity Error Reset and must be set by user software. It will also be set on a Power-on Reset.

For the PIC16C715, bit7 is MPEEN (Memory Parity Error Enable). This bit reflects the status of the MPEEN bit in configuration word. It is unaffected by any reset of interrupt.

8.4.7 PARITY ERROR RESET (PER)

Applicable Devices	710	71	711	715

The PIC16C715 has on-chip parity bits that can be used to verify the contents of program memory. Parity bits may be useful in applications in order to increase overall reliability of a system.

There are two parity bits for each word of Program Memory. The parity bits are computed on alternating bits of the program word. One computation is performed using even parity, the other using odd parity. As a program executes, the parity is verified. The even parity bit is XOR'd with the even bits in the program memory word. The odd parity bit is negated and XOR'd with the odd bits in the program memory word. When an error is detected, a reset is generated and the $\overline{PER}$ flag bit 2 in the PCON register is cleared (logic '0'). This indication can allow software to act on a failure. However, there is no indication of the program memory location of the failure in Program Memory. This flag can only be set (logic '1') by software.

The parity array is user selectable during programming. Bit 7 of the configuration word located at address 2007h can be programmed (read as '0') to disable parity. If left unprogrammed (read as '1'), parity is enabled.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C71

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024 TOSC
RC	72 ms	—	—

TABLE 8-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C710/711/715

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	—	72 ms	—

TABLE 8-10: RESET CONDITION FOR SPECIAL REGISTERS, PIC16C710/71/711

Condition	Program Counter	STATUS Register	PCON Register PIC16C710/711
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset (PIC16C710/711)	000h	0001 1uuu	---- --u0
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 8-11: RESET CONDITION FOR SPECIAL REGISTERS, PIC16C715

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	u--- -10x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	u--- -uuu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	u--- -uuu
WDT Reset	000h	0000 1uuu	u--- -uuu
WDT Wake-up	PC + 1	uuu0 0uuu	u--- -uuu
Brown-out Reset	000h	0001 1uuu	u--- -uu0
Parity Error Reset	000h	uuu1 0uuu	u--- -0uu
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	u--- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2047$

Operation: $k \rightarrow PC<10:0>$
$PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	Process data	Write to PC
2nd Cycle	NOP	NOP	NOP	NOP

Example

```
GOTO THERE
```

After Instruction
PC = Address THERE

INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

00	1010	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

Example

```
INCF    CNT, 1
```

Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2TCY instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
NOP	NOP	NOP	NOP

Example

```
HERE     INCFSZ     CNT, 1
         GOTO       LOOP
CONTINUE •
         •
         •
```

Before Instruction
PC = address HERE
After Instruction
CNT = CNT + 1
if CNT= 0,
PC = address CONTINUE
if CNT≠ 0,
PC = address HERE +1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example

```
IORLW   0x35
```

Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 1

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

11	01xx	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	NOP	Write to W, Pop from the Stack
2nd Cycle	NOP	NOP	NOP	NOP

Example

```
CALL TABLE  ;W contains table
            ;offset value
•           ;W now has table value
•
•
TABLE ADDWF PC   ;W = offset
      RETLW k1   ;Begin table
      RETLW k2   ;
      •
      •
      •
      RETLW kn   ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	NOP	NOP	Pop from the Stack
2nd Cycle	NOP	NOP	NOP	NOP

Example

```
RETURN
```

After Interrupt
PC = TOS

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C75X	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products	PICMASTER®/ PICMASTER-CE In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	Available 3Q97		
	ICEPIC Low-Cost In-Circuit Emulator	✓		✓	✓	✓	✓	✓					
Software Tools	MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MPLAB™ C Compiler	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	*fuzzy*TECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	MP-DriveWay™ Applications Code Generator			✓	✓	✓	✓	✓		✓			
	Total Endurance™ Software Model											✓	
Programmers	PICSTART® Lite Ultra Low-Cost Dev. Kit			✓		✓	✓	✓					
	PICSTART® Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	KEELOQ® Programmer												✓
Demo Boards	SEEVAL® Designers Kit											✓	
	PICDEM-1			✓	✓			✓		✓			
	PICDEM-2					✓	✓						
	PICDEM-3								✓				
	KEELOQ® Evaluation Kit												✓

Applicable Devices	710	71	711	715

11.1 DC Characteristics: PIC16C710-04 (Commercial, Industrial, Extended) PIC16C711-04 (Commercial, Industrial, Extended) PIC16C710-10 (Commercial, Industrial, Extended) PIC16C711-10 (Commercial, Industrial, Extended) PIC16C710-20 (Commercial, Industrial, Extended) PIC16C711-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Param. No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	-	6.0	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
			3.7	4.0	4.4	V	Extended Range Only
D010	Supply Current (Note 2)	IDD	-	2.7	5	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3)	IPD	-	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	21	µA	VDD = 4.0V, WDT disabled, -0°C to +70°C
D021A			-	1.5	24	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	1.5	30	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	µA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

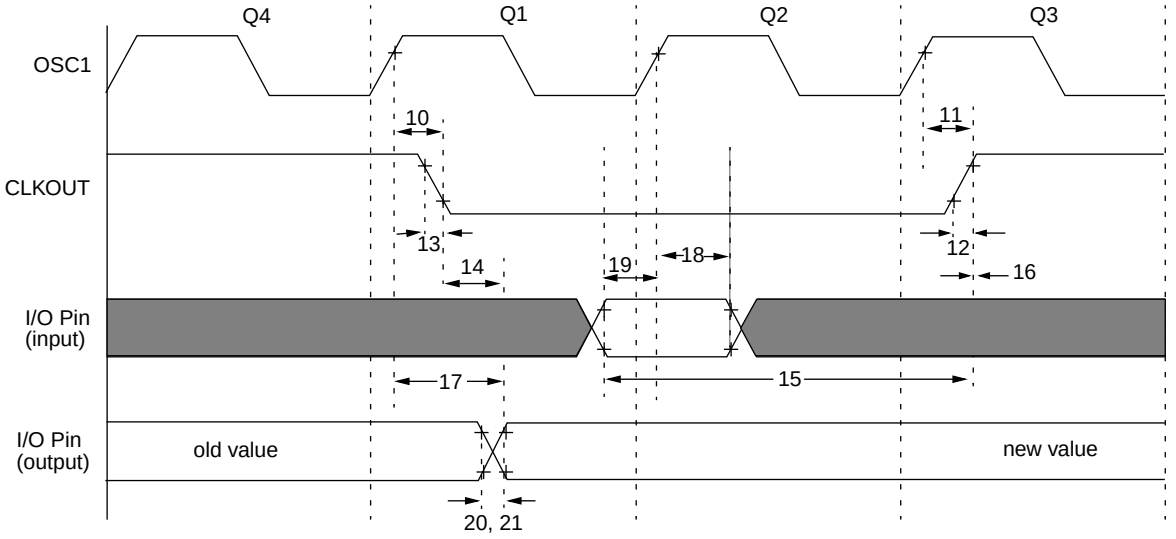
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

Applicable Devices	710	71	711	715

FIGURE 11-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 11-1 for load conditions.

TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	—	80 - 100	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16**C**710/711	—	10	25	ns	
			PIC16**LC**710/711	—	—	60	ns	
21*	TioF	Port output fall time	PIC16**C**710/711	—	10	25	ns	
			PIC16**LC**710/711	—	—	60	ns	
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		20	—	—	ns	

* These parameters are characterized but not tested.

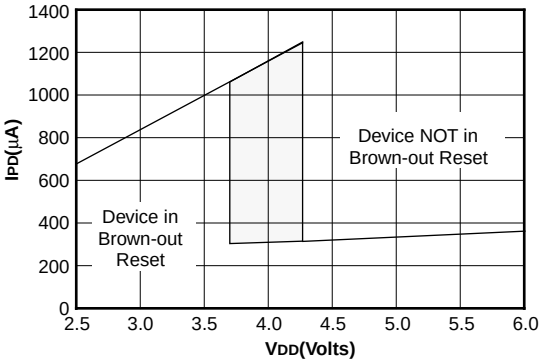
† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

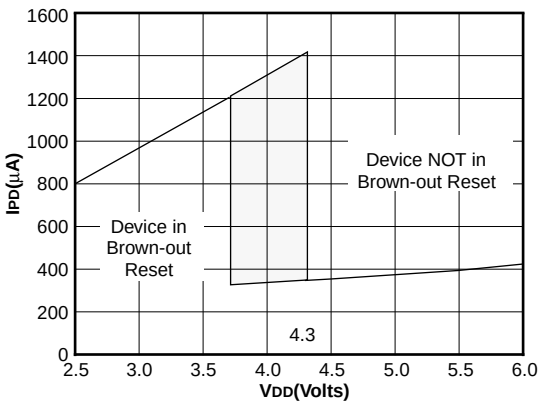
Applicable Devices	710	71	711	715

FIGURE 12-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 12-9: MAXIMUM IPD vs. VDD BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)



The shaded region represents the built-in hysteresis of the brown-out reset circuitry.

FIGURE 12-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

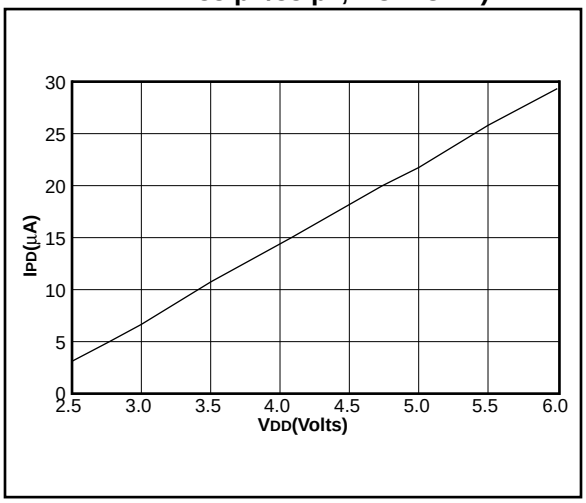
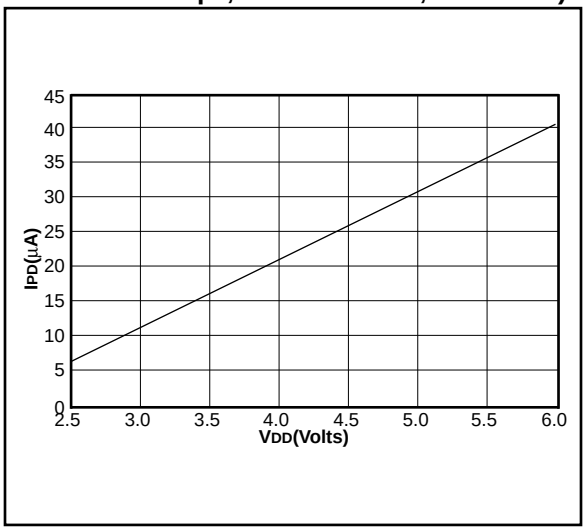


FIGURE 12-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



Applicable Devices	710	71	711	715

FIGURE 12-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

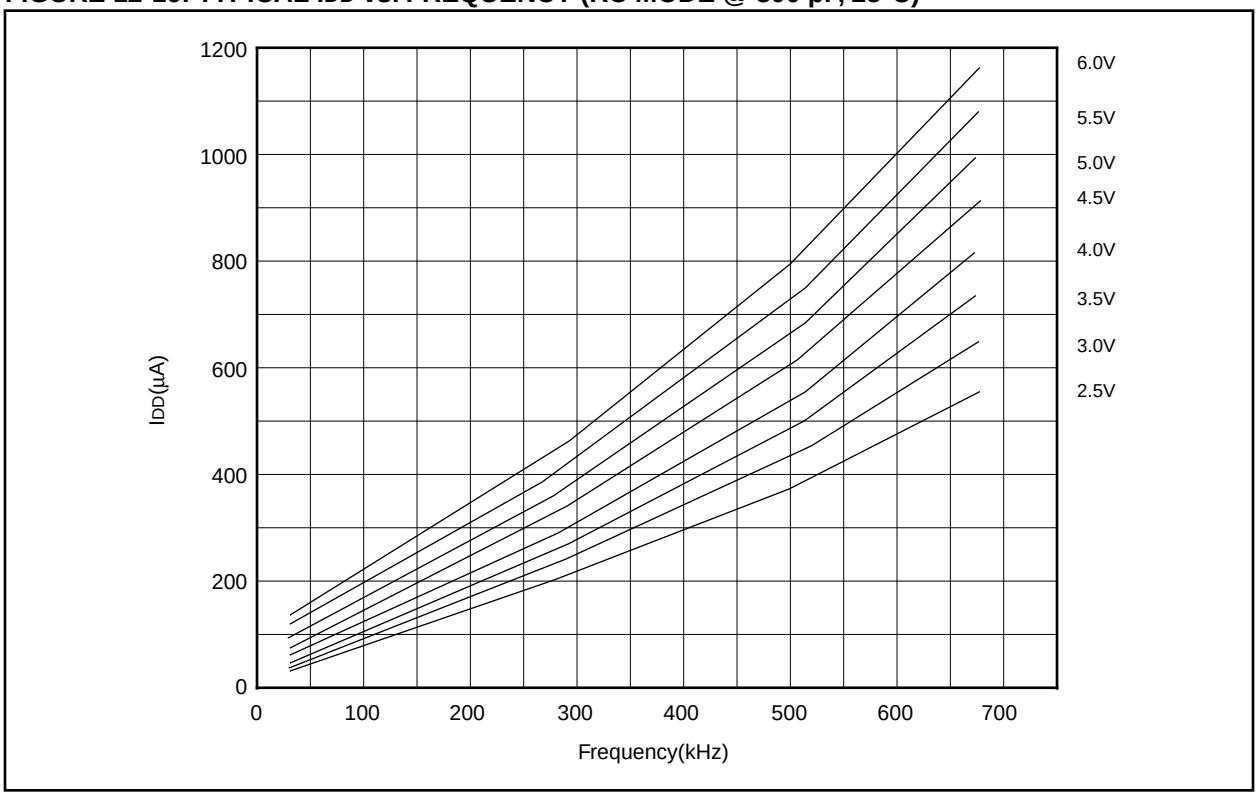
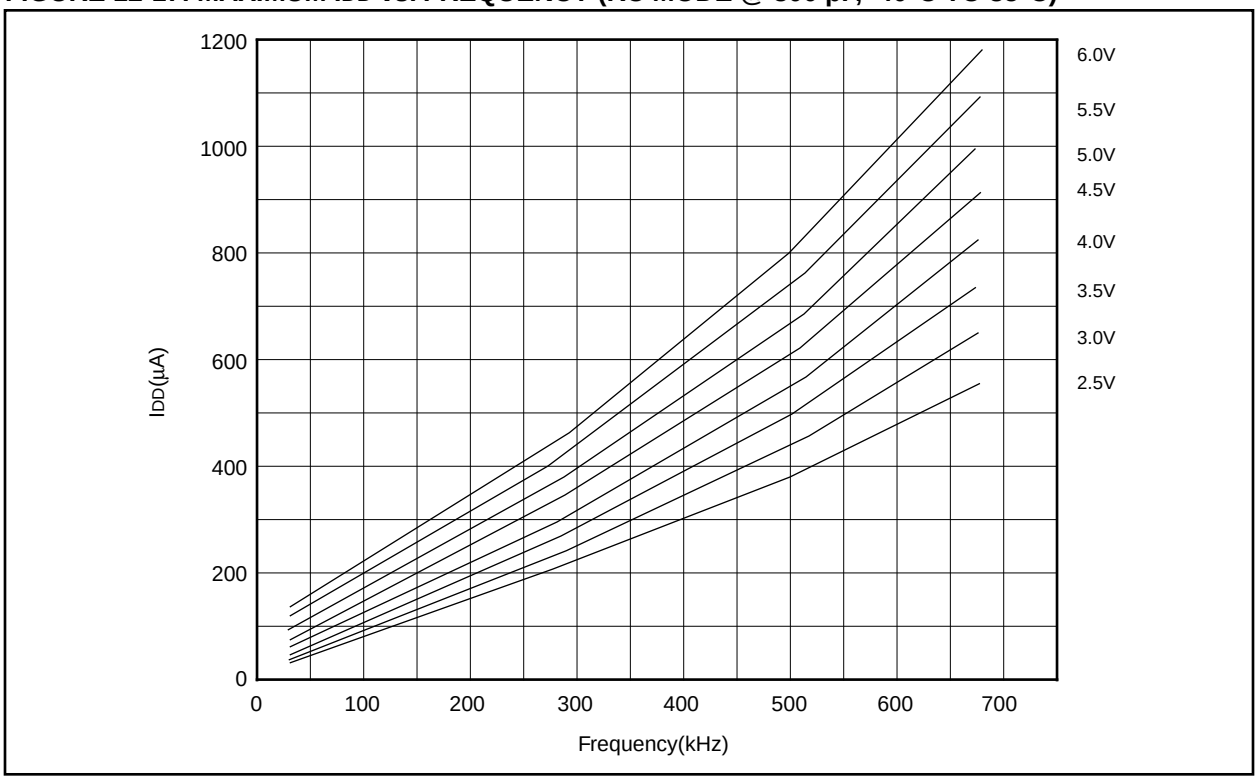


FIGURE 12-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Applicable Devices 710 71 711 715

TABLE 13-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C715-04	PIC16C715-10	PIC16C715-20	PIC16LC715-04	PIC16C715/JW
RC	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 5.5V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
XT	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 5.5V IDD: 2.0 mA typ. at 3.0V IPD: 0.9 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 20 MHz max.	Do not use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.
LP	VDD: 4.0V to 5.5V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 5.5V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 5.5V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

Applicable Devices	710	71	711	715

FIGURE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

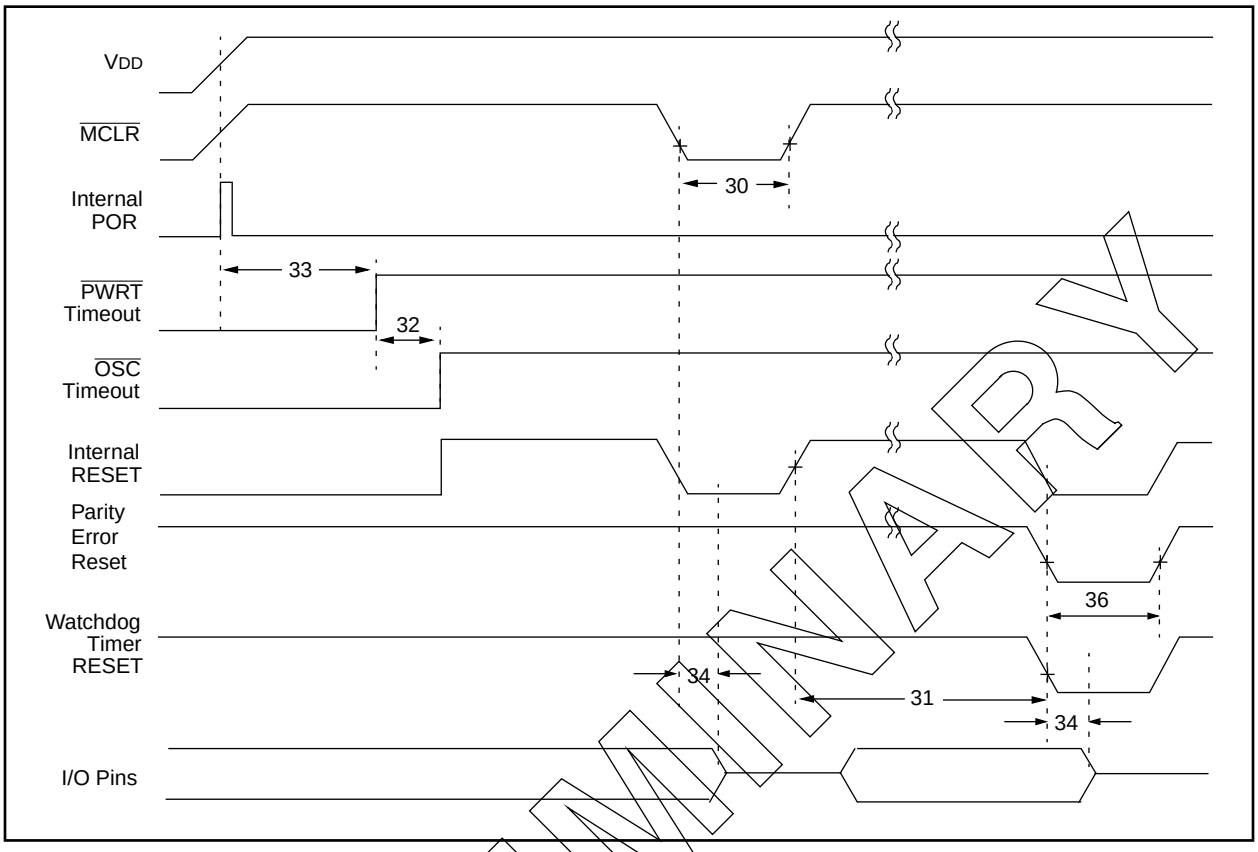


FIGURE 13-5: BROWN-OUT RESET TIMING

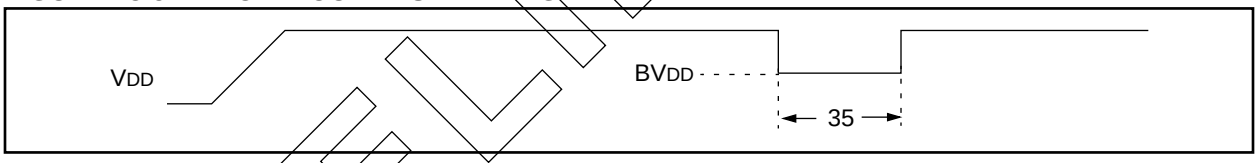


TABLE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—	—	µs	VDD = 5V, -40˚C to +125˚C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40˚C to +125˚C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40˚C to +125˚C
34	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ BVDD (D005)
36	TPER	Parity Error Reset	—	TBD	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Applicable Devices	710	71	711	715

FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

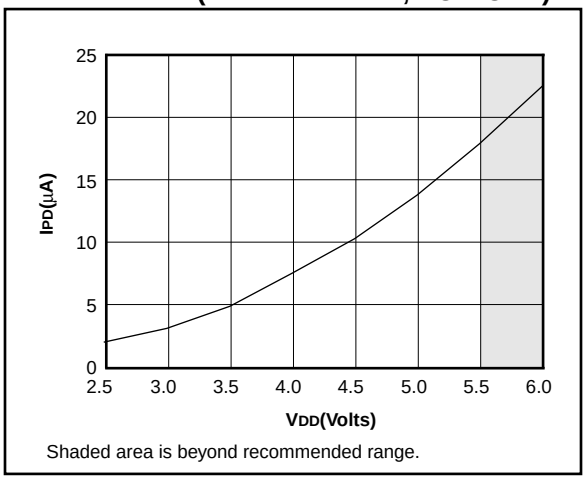


FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

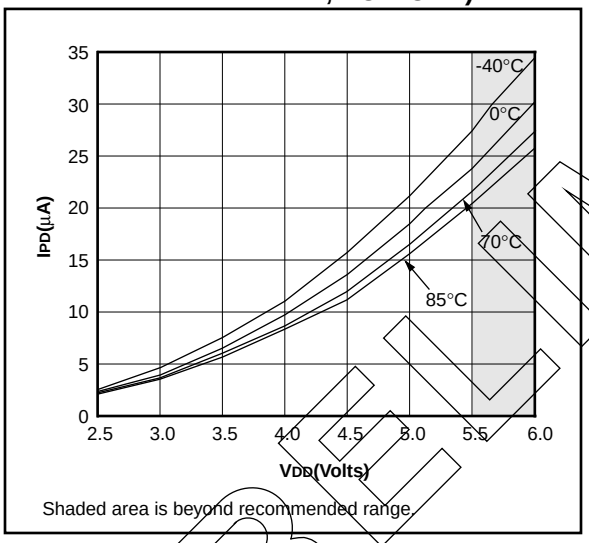


FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

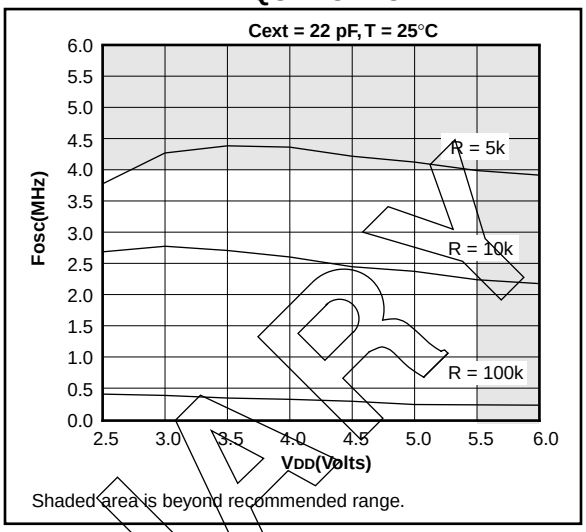


FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

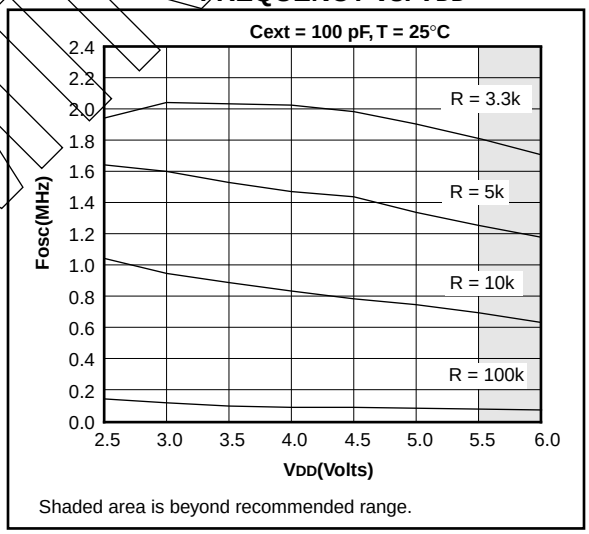
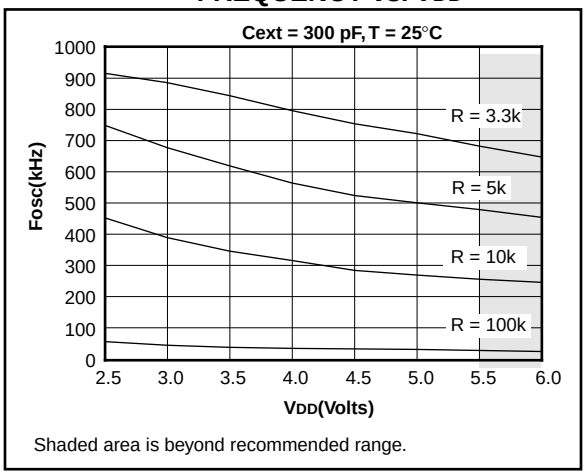


FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Applicable Devices	710	71	711	715

FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY VS. VDD

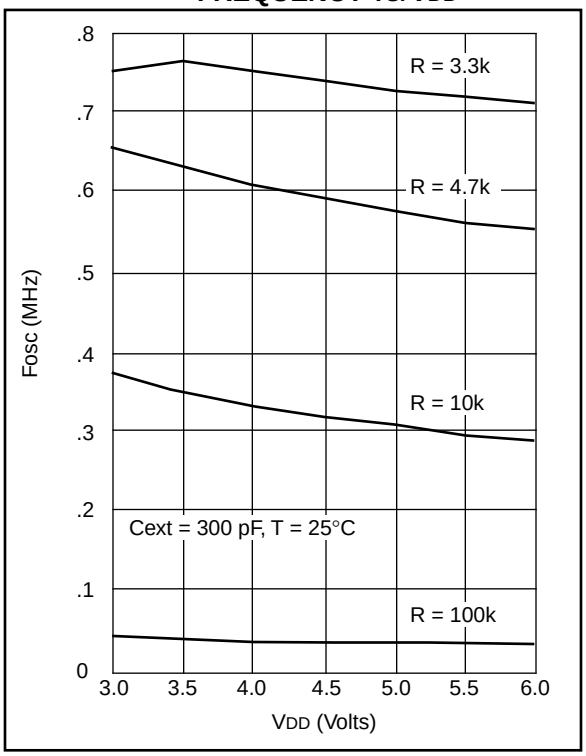


FIGURE 16-5: TYPICAL IPD VS. VDD WATCHDOG TIMER DISABLED 25°C

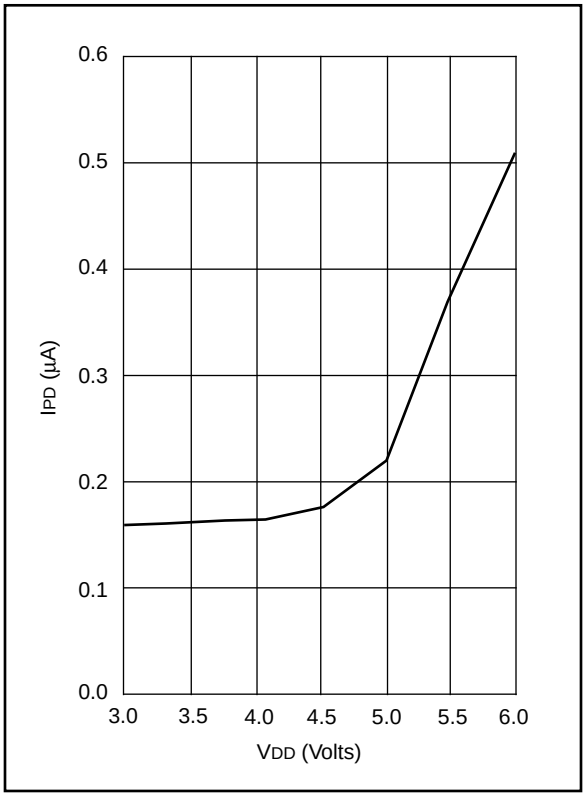
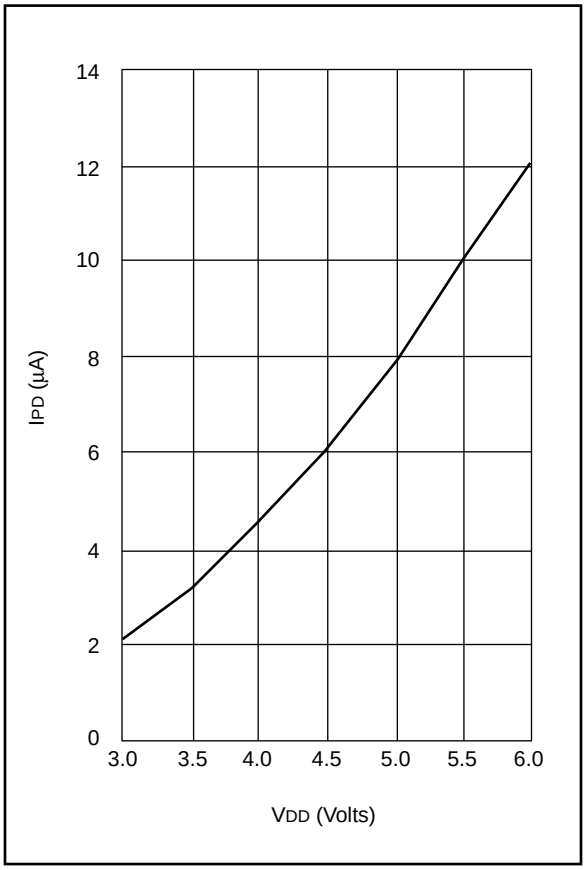


TABLE 16-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20 pF	4.7k	4.52 MHz	±17.35%
	10k	2.47 MHz	±10.10%
	100k	290.86 kHz	±11.90%
100 pF	3.3k	1.92 MHz	±9.43%
	4.7k	1.49 MHz	±9.83%
	10k	788.77 kHz	±10.92%
	100k	88.11 kHz	±16.03%
300 pF	3.3k	726.89 kHz	±10.97%
	4.7k	573.95 kHz	±10.14%
	10k	307.31 kHz	±10.43%
	100k	33.82 kHz	±11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.

FIGURE 16-6: TYPICAL IPD VS. VDD WATCHDOG TIMER ENABLED 25°C



Data based on matrix samples. See first page of this section for details.

Applicable Devices	710	71	711	715

FIGURE 16-21: IOL VS. VOL, VDD = 3V

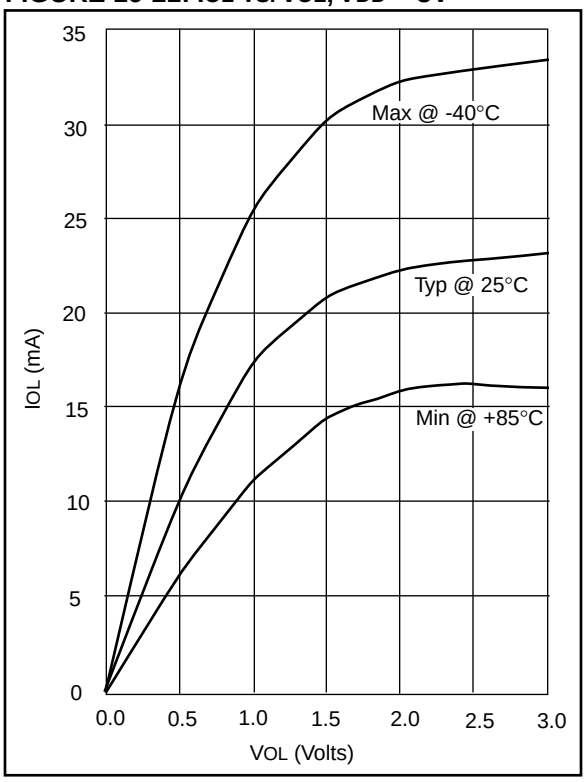
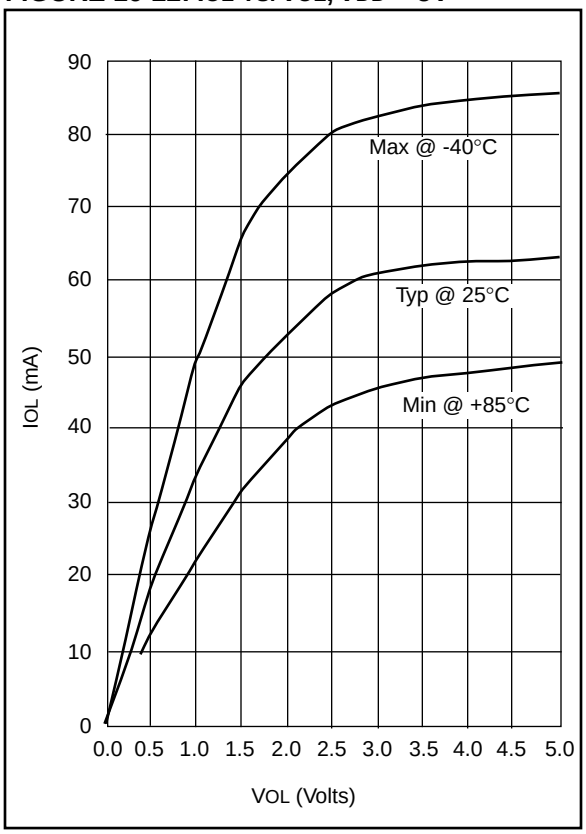


FIGURE 16-22: IOL VS. VOL, VDD = 5V



Data based on matrix samples. See first page of this section for details.

NOTES: