



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c711t-20i-so

PIC16C71X

FIGURE 3-1: PIC16C71X BLOCK DIAGRAM

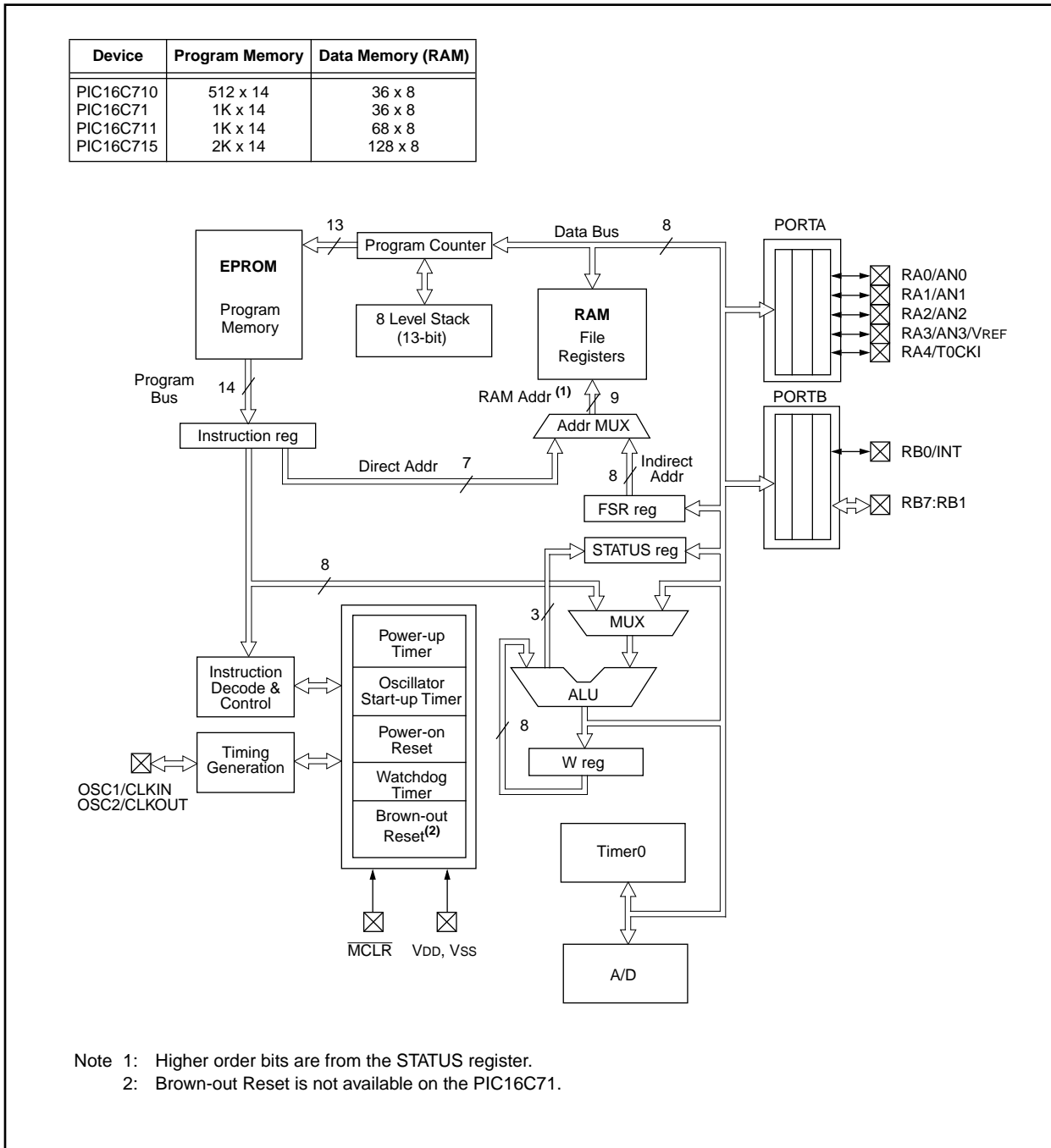


TABLE 4-2: PIC16C715 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR, PER	Value on all other resets (3)
Bank 0											
00h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	T \overline{O}	P \overline{D}	Z	DC	C	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					---x 0000	---u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh	—	Unimplemented								—	—
0Eh	—	Unimplemented								—	—
0Fh	—	Unimplemented								—	—
10h	—	Unimplemented								—	—
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C715, always maintain these bits clear.

PIC16C71X

4.2.2.2 OPTION REGISTER

Applicable Devices 710 71 711 715

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **RBP_U**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

PIC16C71X

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

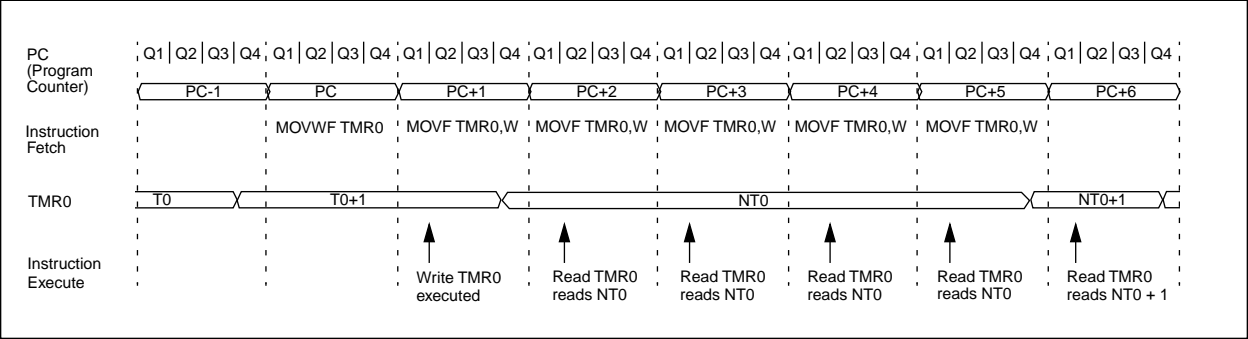
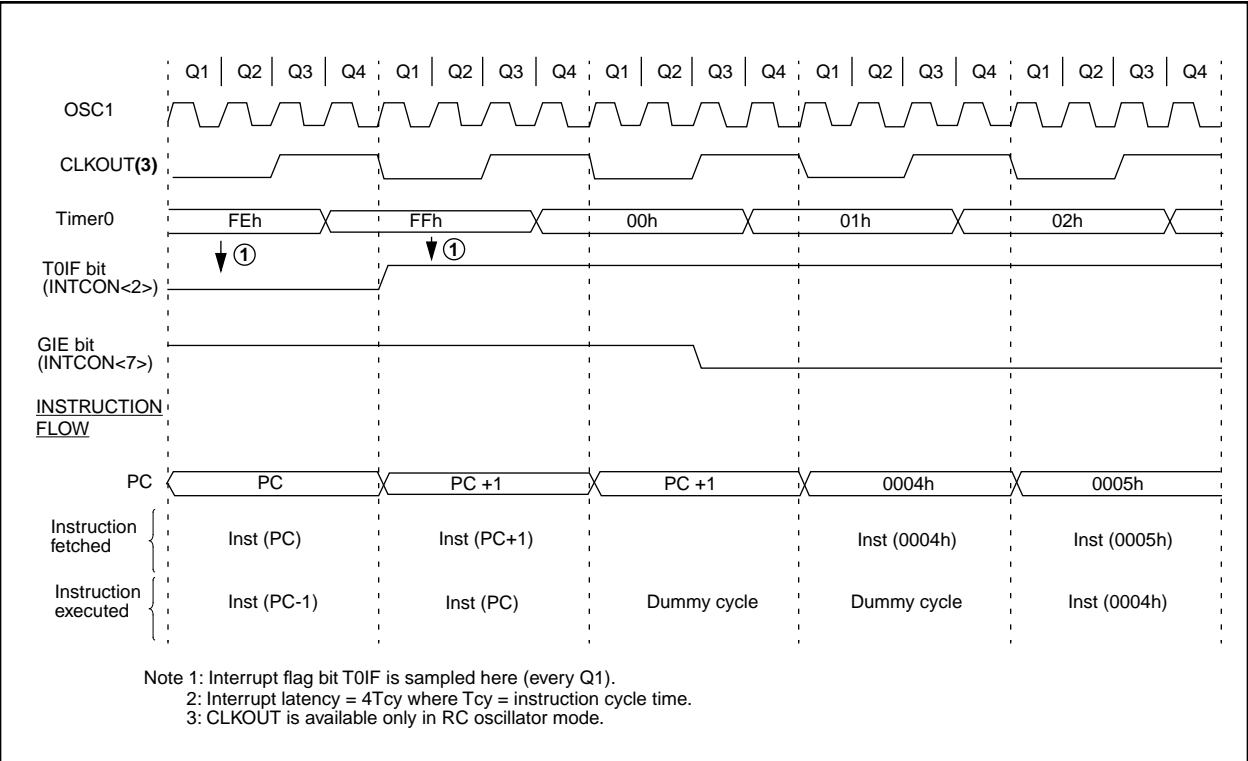


FIGURE 6-4: TIMER0 INTERRUPT TIMING

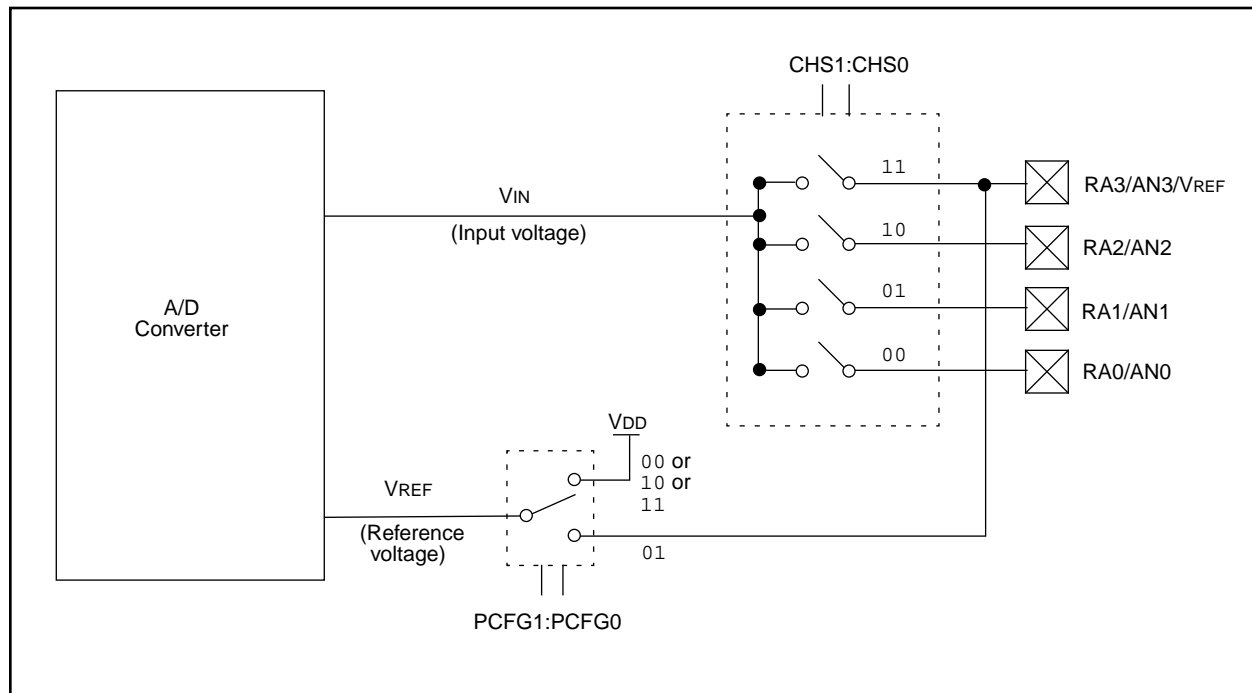


The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 7-4.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 7.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins / voltage reference / and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
 - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

FIGURE 7-4: A/D BLOCK DIAGRAM



PIC16C71X

8.3 Reset

Applicable Devices	710	71	711	715
--------------------	-----	----	-----	-----

The PIC16CXX differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ reset during normal operation
- $\overline{\text{MCLR}}$ reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR) (PIC16C710/711/715)
- Parity Error Reset (PIC16C715)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the $\overline{\text{MCLR}}$ and

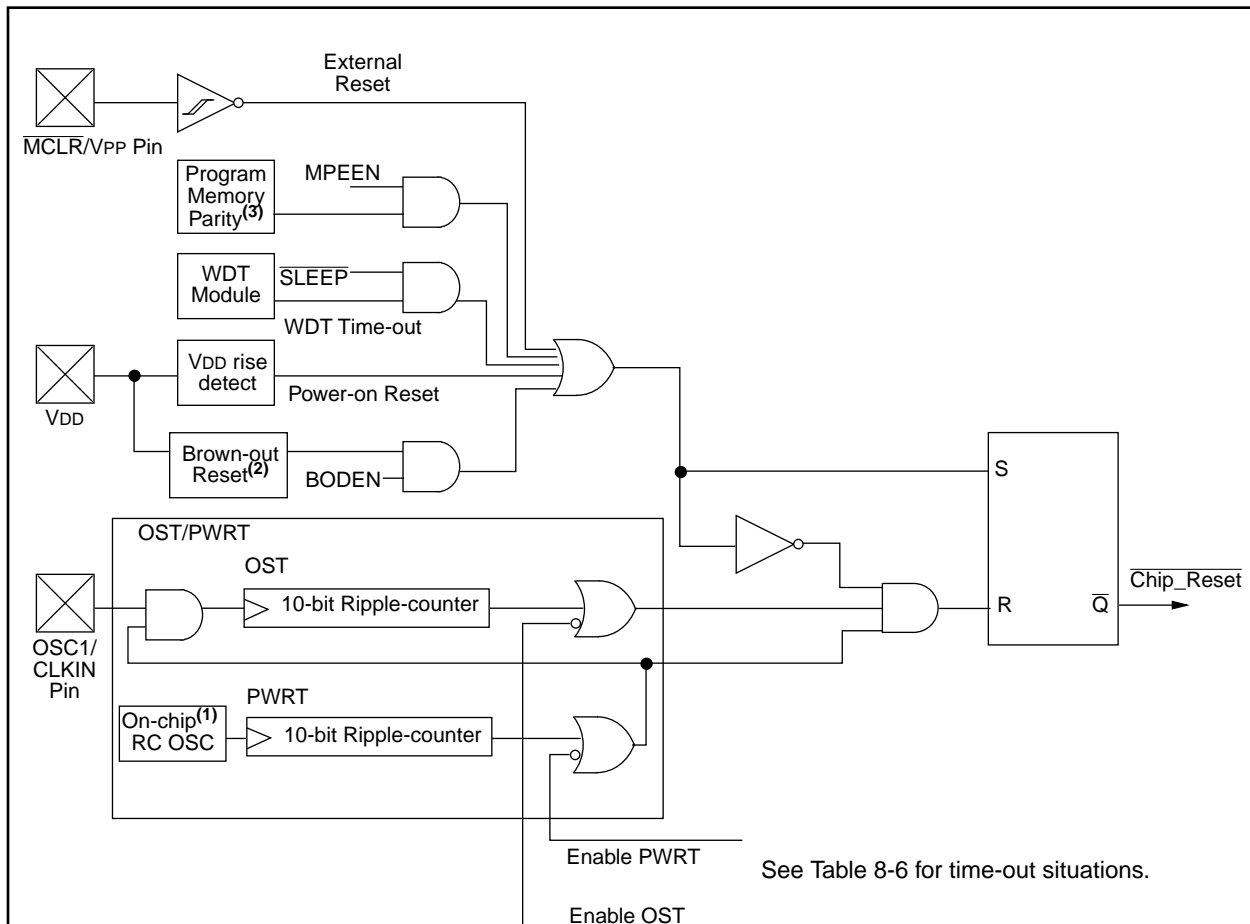
WDT Reset, on $\overline{\text{MCLR}}$ reset during SLEEP, and Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Table 8-7, Table 8-8 and Table 8-9. These bits are used in software to determine the nature of the reset. See Table 8-10 and Table 8-11 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 8-9.

The PIC16C710/711/715 have a $\overline{\text{MCLR}}$ noise filter in the $\overline{\text{MCLR}}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

FIGURE 8-9: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

Note 2: Brown-out Reset is implemented on the PIC16C710/711/715.

Note 3: Parity Error Reset is implemented on the PIC16C715.

PIC16C71X

8.4.5 TIME-OUT SEQUENCE

Applicable Devices	710	71	711	715
---------------------------	-----	----	-----	-----

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 8-11, Figure 8-12, and Figure 8-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 8-12). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 8-10 and Table 8-11 show the reset conditions for some special function registers, while Table 8-12 and Table 8-13 show the reset conditions for all the registers.

8.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices	710	71	711	715
---------------------------	-----	----	-----	-----

The Power Control/Status Register, PCON has up to two bits, depending upon the device.

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred. The $\overline{\text{BOR}}$ bit is a "Don't Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

For the PIC16C715, bit2 is $\overline{\text{PER}}$ (Parity Error Reset). It is cleared on a Parity Error Reset and must be set by user software. It will also be set on a Power-on Reset.

For the PIC16C715, bit7 is MPEEN (Memory Parity Error Enable). This bit reflects the status of the MPEEN bit in configuration word. It is unaffected by any reset of interrupt.

8.4.7 PARITY ERROR RESET (PER)

Applicable Devices	710	71	711	715
---------------------------	-----	----	-----	-----

The PIC16C715 has on-chip parity bits that can be used to verify the contents of program memory. Parity bits may be useful in applications in order to increase overall reliability of a system.

There are two parity bits for each word of Program Memory. The parity bits are computed on alternating bits of the program word. One computation is performed using even parity, the other using odd parity. As a program executes, the parity is verified. The even parity bit is XOR'd with the even bits in the program memory word. The odd parity bit is negated and XOR'd with the odd bits in the program memory word. When an error is detected, a reset is generated and the PER flag bit 2 in the PCON register is cleared (logic '0'). This indication can allow software to act on a failure. However, there is no indication of the program memory location of the failure in Program Memory. This flag can only be set (logic '1') by software.

The parity array is user selectable during programming. Bit 7 of the configuration word located at address 2007h can be programmed (read as '0') to disable parity. If left unprogrammed (read as '1'), parity is enabled.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C71

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT = 1	PWRT = 0	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024 TOSC
RC	72 ms	—	—

TABLE 8-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C710/711/715

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	PWRT = 0	PWRT = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	—	72 ms	—

PIC16C71X

TABLE 8-13: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C715

Register	Power-on Reset, Brown-out Reset Parity Error Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	---x 0000	---u 0000	---u uuuu
PORTB	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
PIR1	-0-- ----	-0-- ----	-u-- ---- ⁽¹⁾
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION	1111 1111	1111 1111	uuuu uuuu
TRISA	---1 1111	---1 1111	---u uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-0-- ----	-0-- ----	-u-- ----
PCON	---- -qbb	---- -1uu	---- -1uu
ADCON1	---- --00	---- --00	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-11 for reset value for specific condition.

PIC16C71X

FIGURE 8-17: INTERRUPT LOGIC, PIC16C710, 71, 711

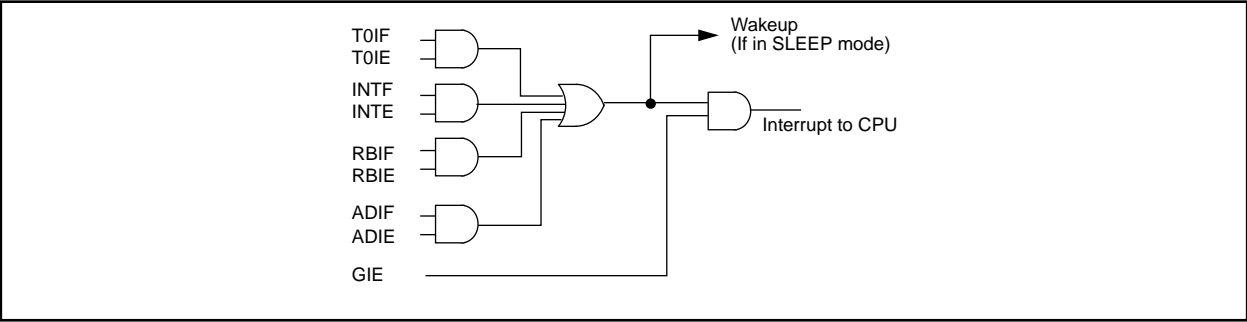
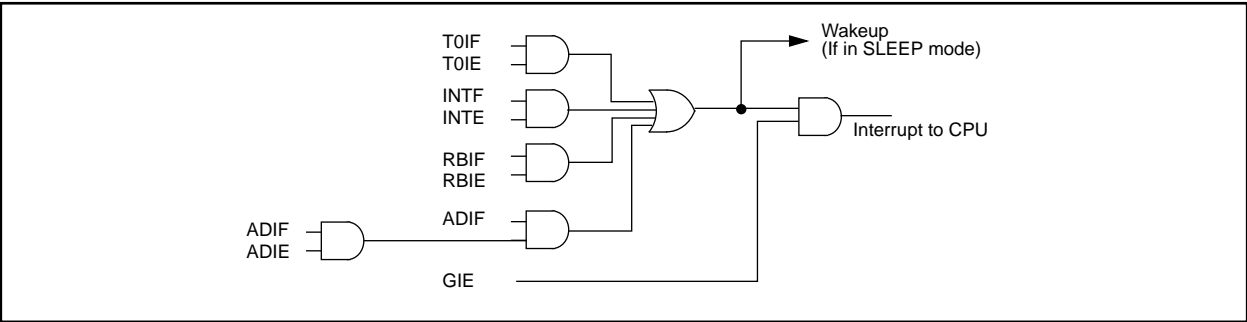


FIGURE 8-18: INTERRUPT LOGIC, PIC16C715



PIC16C71X

8.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 8-1 stores and restores the STATUS and W registers. The user register, STATUS_TEMP, must be defined in bank 0.

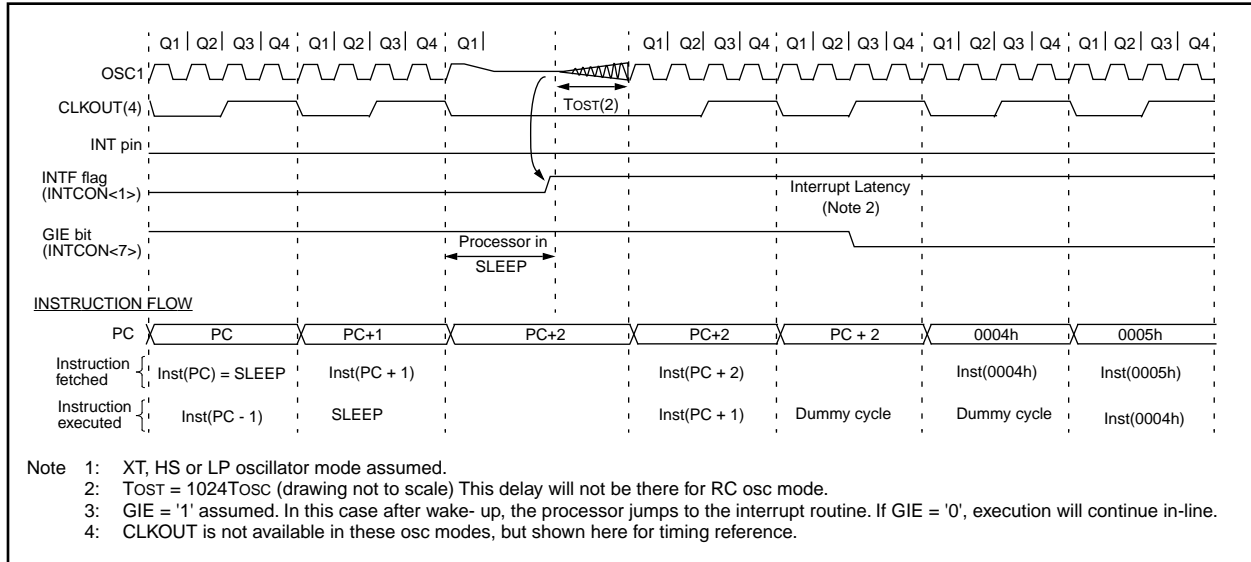
The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Executes the ISR code.
- d) Restores the STATUS register (and bank select bit).
- e) Restores the W register.

EXAMPLE 8-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP          ;Copy W to TEMP register, could be bank one or zero
SWAPF    STATUS,W         ;Swap status to be saved into W
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
: (ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```

FIGURE 8-22: WAKE-UP FROM SLEEP THROUGH INTERRUPT



8.9 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

8.10 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

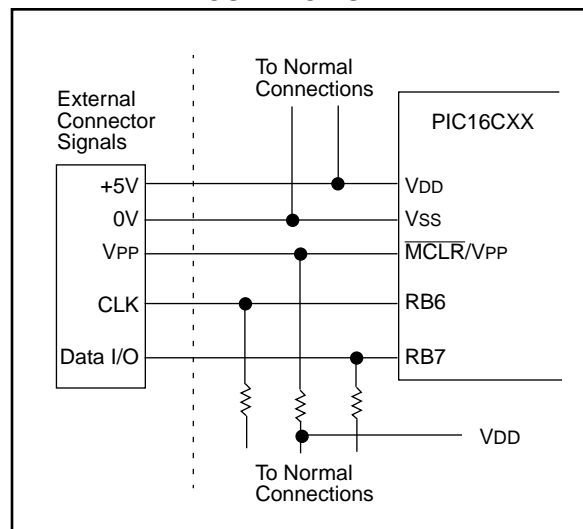
8.11 In-Circuit Serial Programming

PIC16CXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low while raising the MCLR (VPP) pin from V_{IL} to V_{IH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X Programming Specifications (Literature #DS30228).

FIGURE 8-23: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



PIC16C71X

GOTO Unconditional Branch

Syntax: [*label*] GOTO *k*

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow PC<10:0>$
 $PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk
----	------	------	------

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	Process data	Write to PC
2nd Cycle	NOP	NOP	NOP	NOP

Example

```
GOTO THERE
After Instruction
PC = Address THERE
```

INCF Increment f

Syntax: [*label*] INCF *f*,*d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

00	1010	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

Example

```
INCF CNT, 1
```

Before Instruction

```
CNT = 0xFF
Z   = 0
```

After Instruction

```
CNT = 0x00
Z   = 1
```

NOP		No Operation			
Syntax:	[<i>label</i>] NOP				
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	00	0000	0xx0	0000	
Description:	No operation.				
Words:	1				
Cycles:	1				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
	Decode	NOP	NOP	NOP	
Example	NOP				

RETFIE		Return from Interrupt			
Syntax:	[<i>label</i>] RETFIE				
Operands:	None				
Operation:	TOS → PC, 1 → GIE				
Status Affected:	None				
Encoding:	00	0000	0000	1001	
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.				
Words:	1				
Cycles:	2				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
1st Cycle	Decode	NOP	Set the GIE bit	Pop from the Stack	
2nd Cycle	NOP	NOP	NOP	NOP	

Example

```

RETFIE
After Interrupt
    PC = TOS
    GIE = 1

```

OPTION	Load Option Register			
Syntax:	[<i>label</i>] OPTION			
Operands:	None			
Operation:	(W) → OPTION			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.			
Words:	1			
Cycles:	1			
Example	<div>To maintain upward compatibility with future PIC16CXX products, do not use this instruction.</div>			

13.4 Timing Parameter Symbolology

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

T		T	
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	ss	SS
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-1: LOAD CONDITIONS

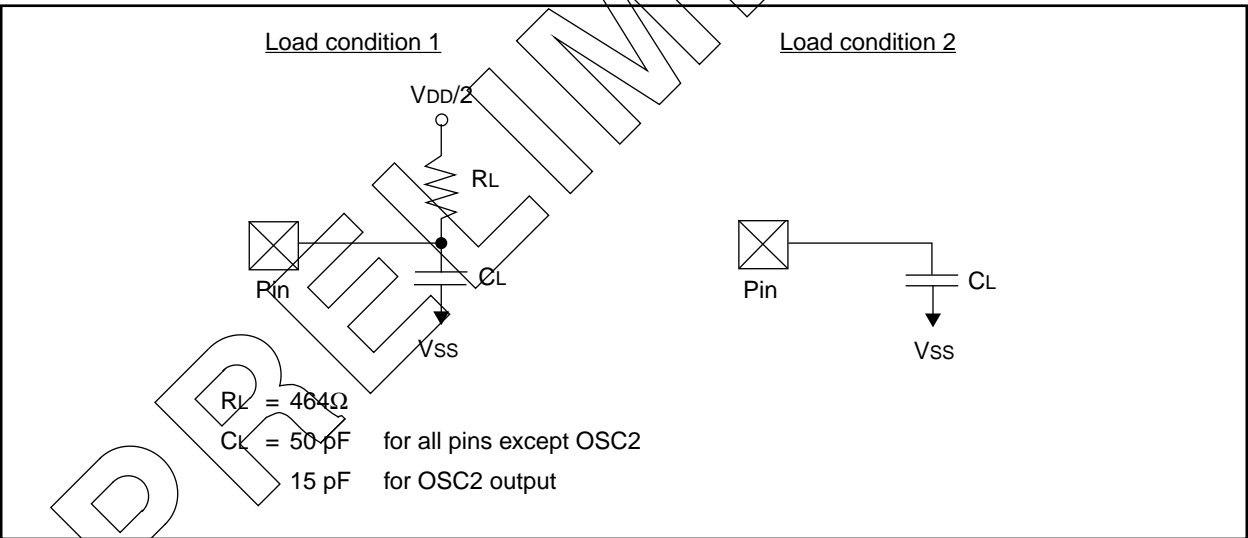


FIGURE 14-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

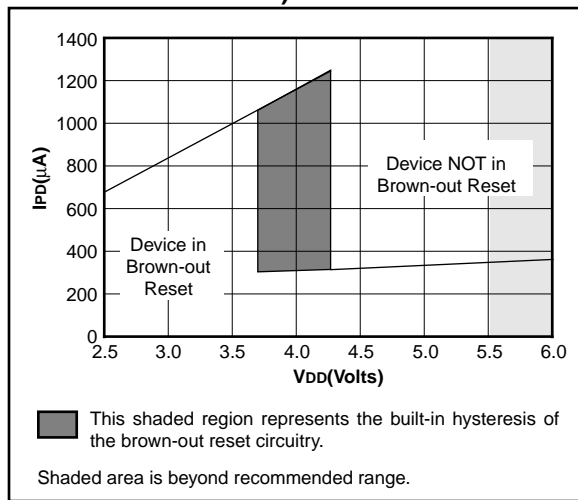


FIGURE 14-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

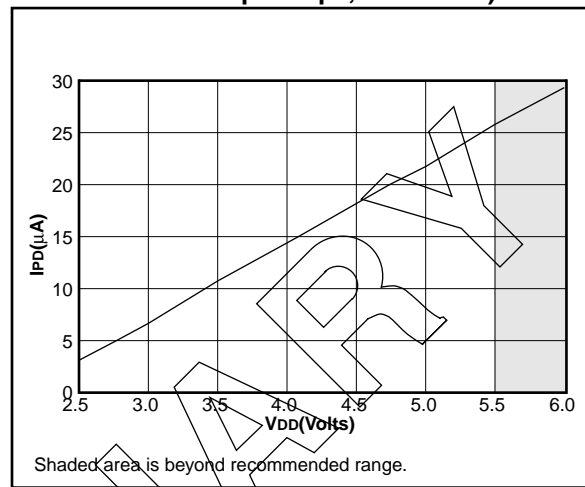


FIGURE 14-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

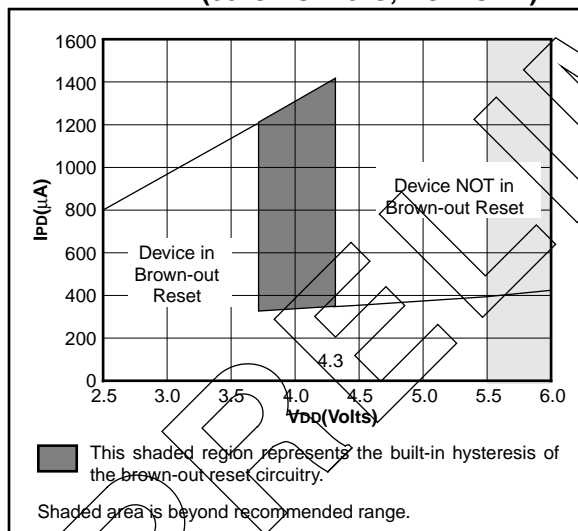
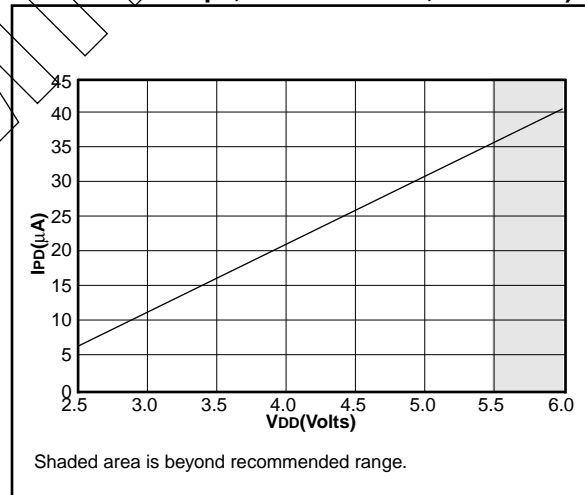


FIGURE 14-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 16-10: V_{IH} , V_{IL} OF \overline{MCLR} , $T0CKI$ AND $OSC1$ (IN RC MODE) vs. V_{DD}

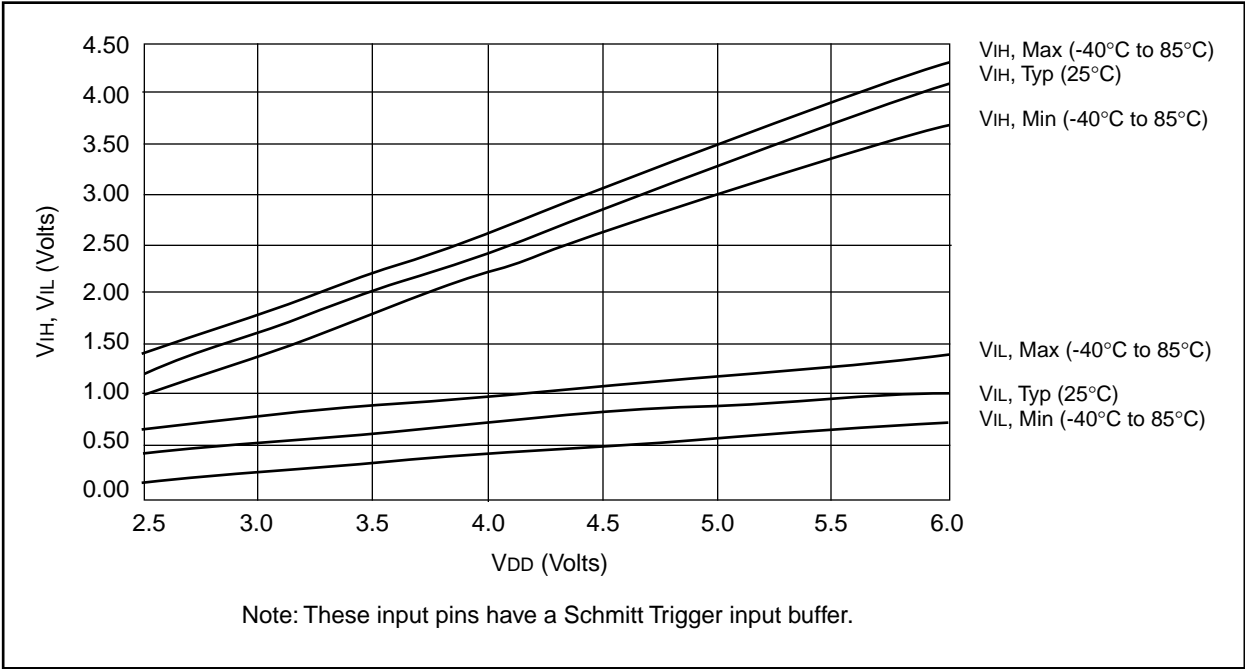
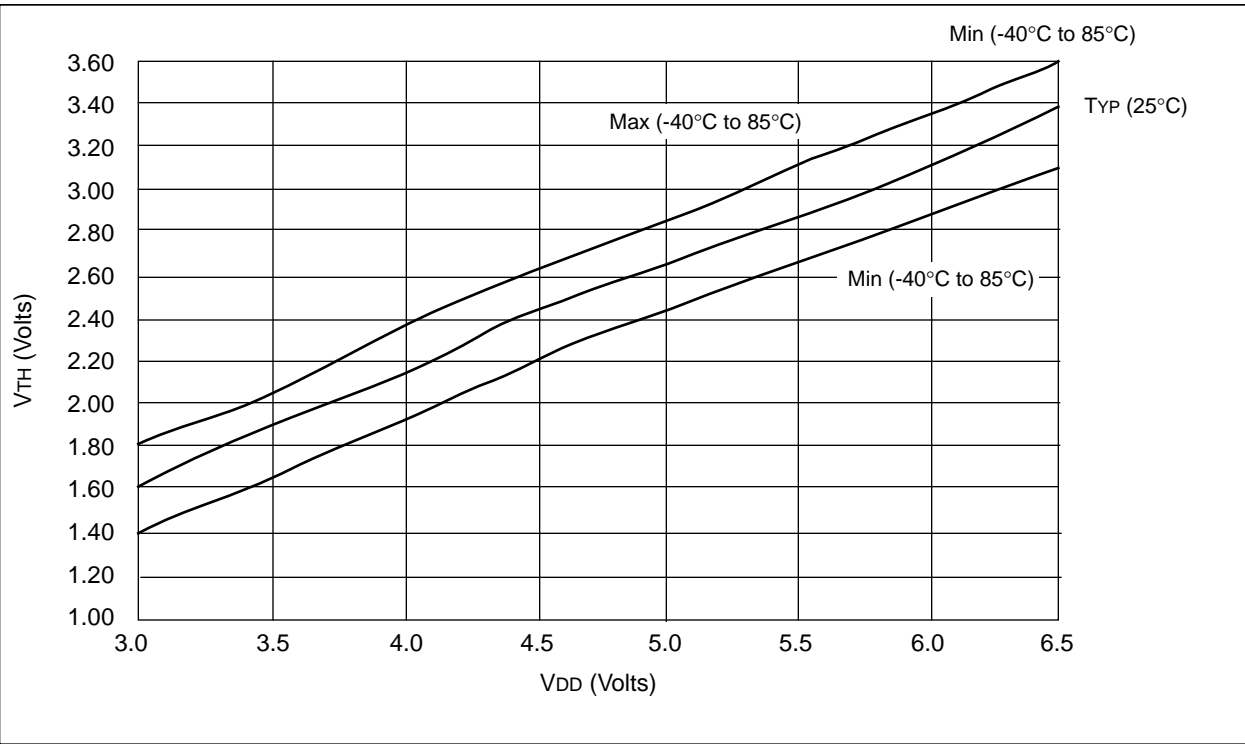


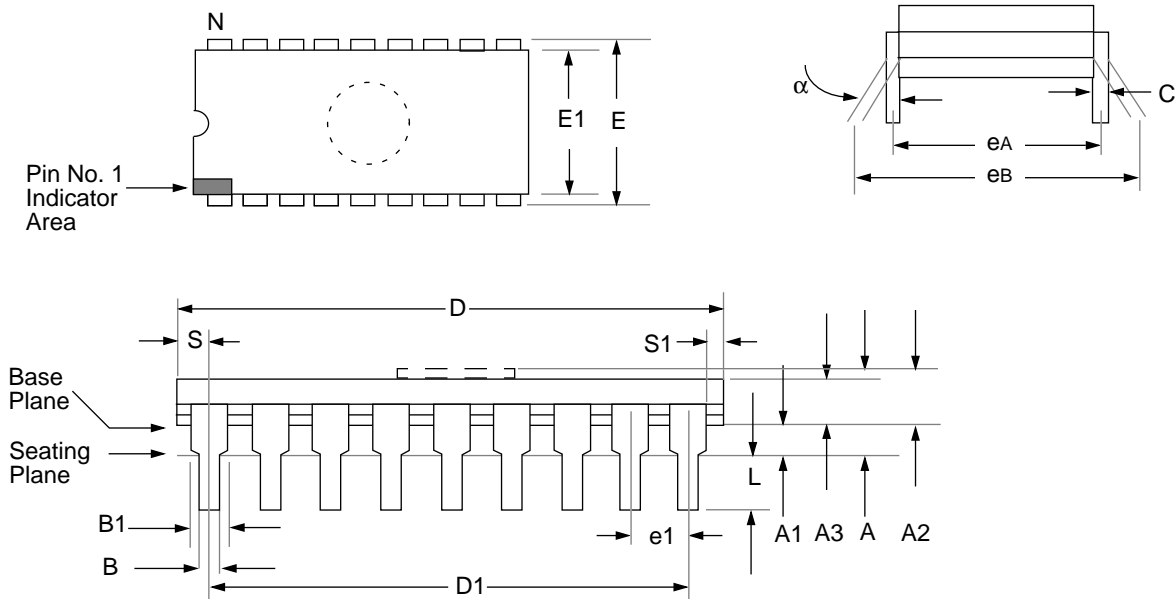
FIGURE 16-11: V_{TH} (INPUT THRESHOLD VOLTAGE) OF $OSC1$ INPUT (IN XT, HS, AND LP MODES) vs. V_{DD}



Data based on matrix samples. See first page of this section for details.

17.0 PACKAGING INFORMATION

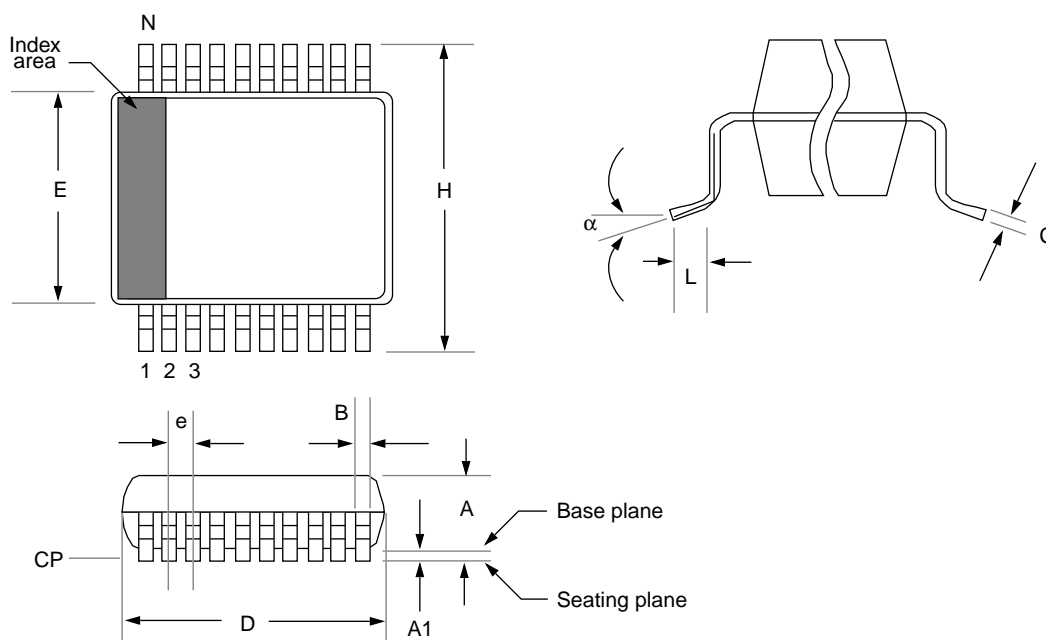
17.1 18-Lead Ceramic Cerdip Dual In-line with Window (300 mil) (JW)



Package Group: Ceramic Cerdip Dual In-Line (CDP)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.7780		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

PIC16C71X

17.4 20-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)



Package Group: Plastic SSOP						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	7.070	7.330		0.278	0.289	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	Reference	0.026	0.026	Reference
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	20	20		20	20	
CP	-	0.102		-	0.004	

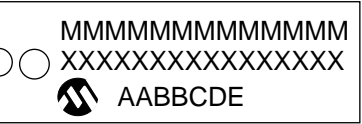
Note 1: Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25m/m (0.010") per side. D1 and E1 dimensions including mold mismatch.

2: Dimension "b" does not include Dambar protrusion, allowable Dambar protrusion shall be 0.08m/m (0.003")max.

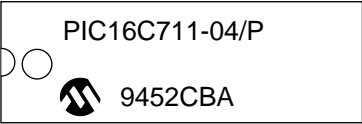
3: This outline conforms to JEDEC MS-026.

17.5 Package Marking Information

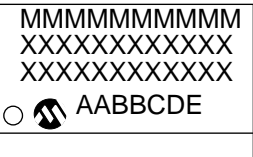
18-Lead PDIP



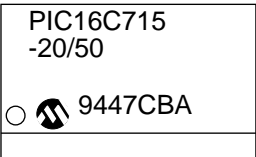
Example



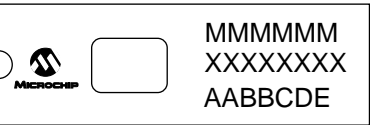
18-Lead SOIC



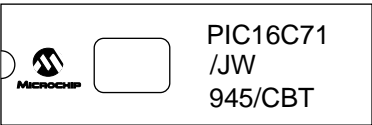
Example



18-Lead CERDIP Windowed



Example



20-Lead SSOP



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calender year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.
	D ₁	Mask revision number for microcontroller
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

RA2/AN2	9
RA3/AN3/VREF	9
RA4/T0CKI	9
RB0/INT	9
RB1	9
RB2	9
RB3	9
RB4	9
RB5	9
RB6	9
RB7	9
VDD	9
VSS	9
Pinout Descriptions	
PIC16C71	9
PIC16C710	9
PIC16C711	9
PIC16C715	9
PIR1 Register	21
POP	23
POR	53, 54
Oscillator Start-up Timer (OST)	47, 53
Power Control Register (PCON)	54
Power-on Reset (POR)	47, 53, 57, 58
Power-up Timer (PWRT)	47, 53
Time-out Sequence	54
Time-out Sequence on Power-up	59
TO	52, 55
POR bit	22, 54
Port RB Interrupt	63
PORTA	57, 58
PORTA Register	14, 15, 25
PORTB	57, 58
PORTB Register	14, 15, 27
Power-down Mode (SLEEP)	66
Prescaler, Switching Between Timer0 and WDT	35
PRO MATE® II Universal Programmer	85
Program Branches	7
Program Memory	
Paging	23
Program Memory Maps	
PIC16C71	11
PIC16C710	11
PIC16C711	11
PIC16C715	11
Program Verification	67
PS0 bit	18
PS1 bit	18
PS2 bit	18
PSA bit	18
PUSH	23
PWRT	
Power-up Timer (PWRT)	53
PWRT bit	47, 48
R	
RBIE bit	19
RBIF bit	19, 27, 63
RBPU bit	18
RC	54
RC Oscillator	51, 54
Read-Modify-Write	30
Register File	12
Registers	
Maps	
PIC16C71	12
PIC16C710	12

PIC16C711	13
PIC16C715	13
Reset Conditions	56
Summary	14-??
Reset	47, 52
Reset Conditions for Special Registers	56
RP0 bit	12, 17
RP1 bit	17
S	
SEEVAL® Evaluation and Programming System	87
Services	
One-Time-Programmable (OTP) Devices	5
Quick-Turnaround-Production (QTP) Devices	5
Serialized Quick-Turnaround Production (SQTP) Devices	5
SLEEP	47, 52
Software Simulator (MPLAB™ SIM)	87
Special Features of the CPU	47
Special Function Registers	
PIC16C71	14
PIC16C710	14
PIC16C711	14
Special Function Registers, Section	14
Stack	23
Overflows	23
Underflow	23
STATUS Register	17
T	
T0CS bit	18
T0IE bit	19
T0IF bit	19
TAD	41
Timer0	
RTCC	57, 58
Timers	
Timer0	
Block Diagram	31
External Clock	33
External Clock Timing	33
Increment Delay	33
Interrupt	31
Interrupt Timing	32
Prescaler	34
Prescaler Block Diagram	34
Section	31
Switching Prescaler Assignment	35
Synchronization	33
T0CKI	33
T0IF	63
Timing	31
TMR0 Interrupt	63
Timing Diagrams	
A/D Conversion	100, 124, 146
Brown-out Reset	53, 97
CLKOUT and I/O	96, 119, 142
External Clock Timing	95, 118, 141
Power-up Timer	97, 143
Reset	97, 143
Start-up Timer	97, 143
Time-out Sequence	59
Timer0	31, 98, 121, 144
Timer0 Interrupt Timing	32
Timer0 with External Clock	33
Wake-up from SLEEP through Interrupt	67
Watchdog Timer	97, 143