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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c715-04e-so

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Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

#### EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

ORG 0x5	500	
BSF	pclath,3	;Select page 1 (800h-FFFh)
BCF	pclath,4	;Only on >4K devices
CALL	SUB1_P1	;Call subroutine in
	:	;page 1 (800h-FFFh)
	:	
	:	
ORG 0x9	900	
SUB1_P1	:	;called subroutine
	:	;page 1 (800h-FFFh)
	:	
RETURN		;return to Call subroutine
		;in page 0 (000h-7FFh)

#### 4.5 <u>Indirect Addressing, INDF and FSR</u> <u>Registers</u>

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-15. However, IRP is not used in the PIC16C71X devices.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

#### EXAMPLE 4-2: INDIRECT ADDRESSING

	movlw	0x20	;initialize pointer
	movwf	FSR	;to RAM
NEXT	clrf	INDF	;clear INDF register
	incf	FSR,F	;inc pointer
	btfss	FSR,4	;all done?
	goto	NEXT	;no clear next
CONTINUE			
	:		;yes continue

#### FIGURE 4-15: DIRECT/INDIRECT ADDRESSING



#### FIGURE 5-4: BLOCK DIAGRAM OF RB7:RB4 PINS (PIC16C71)



#### TABLE 5-3: PORTB FUNCTIONS



Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

#### 6.0 TIMER0 MODULE

#### Applicable Devices71071711715

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- · Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit TOCS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit TOCS (OPTION<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit TOSE (OPTION<4>). Clearing

FIGURE 6-1: TIMER0 BLOCK DIAGRAM

bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

#### 6.1 <u>Timer0 Interrupt</u>

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.



#### FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE



#### 8.5.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 8.8 for details on SLEEP mode.

#### 8.5.2 TMR0 INTERRUPT

An overflow (FFh  $\rightarrow$  00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 6.0)

#### 8.5.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 5.2)

For the PIC16C71 Note: if a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

	Q1   Q2   Q3   Q4	Q1   Q2   Q3   Q4	Q1   Q2   Q3   Q4	Q1   Q2   Q3   Q4	Q1   Q2   Q3   Q4
OSC1 /					
CLKOUT ③	(4)			/	
INT pin		1	1 1 1 1		1 1 1 1 1 1 1 1
INTF flag (INTCON<1>)			Interrupt Latency (2)		
GIE bit (INTCON<7>)					
INSTRUCTION	FLOW		, , , , , , , , , , , , , , , , , , , ,		· · · · · · · · · · · · · · · · · · ·
PC	PC	PC+1	PC+1	X 0004h	X 0005h
Instruction ( fetched	Inst (PC)	Inst (PC+1)	_	Inst (0004h)	Inst (0005h)
Instruction {	Inst (PC-1)	Inst (PC)	Dummy Cycle	Dummy Cycle	Inst (0004h)

#### FIGURE 8-19: INT PIN INTERRUPT TIMING

Note 1: INTF flag is sampled here (every Q1).

2: Interrupt latency = 3-4 Tcy where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in RC oscillator mode. 4: For minimum width of INT pulse, refer to AC specs.

5: INTF is enabled to be set anytime during the Q4-Q1 cycles.

#### 8.7 <u>Watchdog Timer (WDT)</u>

#### Applicable Devices 710 71 711 715

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 8.1).

#### 8.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The  $\overline{\text{TO}}$  bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

#### 8.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

**Note:** When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.



#### FIGURE 8-21: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN <sup>(1)</sup>	CP1	CP0	PWRTE <sup>(1)</sup>	WDTE	FOSC1	FOSC0
81h,181h	OPTION	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 8-1, Figure 8-2 and Figure 8-3 for operation of these bits.

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BTFSS	Bit Test	f, Skip if S	Set		CALL	Call Sub	routine		
Syntax:	[ <i>label</i> ] BTFSS f,b		Syntax:	[ label ]	[ <i>label</i> ] CALL k				
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7			Operands:	$0 \le k \le 2047$				
Operation:	skip if (f <b>) = 1</b>			Operation.	$(PC)+1 \rightarrow TOS, k \rightarrow PC<10:0>, (PC) ATU (4:2; ) \rightarrow PC (42:14).$			·11、	
Status Affected:	None				Status Affastad	None	1<4.32) -	710012	
Encoding:	01	11bb	bfff	ffff	Status Affected:	None			1
Description:	If bit 'b' in register 'f' is '0' then the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.			Encoding: Description:	10         0kkk         kkkk         kkkk           Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loade into PC bits <10.5 The upper bits of			ddress ck. The s loaded r bits of	
Words:	1					the PC are	e loaded fi two cycle	om PCLA	TH.
Cycles:	1(2)				Words	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4	Cvcles:	2			
	Decode	Read register 'f'	Process data	NOP	Q Cycle Activity:	Q1	Q2	Q3	Q4
If Skip:	(2nd Cyc	:le)			1st Cycle	Decode	Read literal 'k',	Process data	Write to PC
	Q1	Q2	Q3	Q4			Push PC to Stack		
	NOP	NOP	NOP	NOP	2nd Cycle	NOP	NOP	NOP	NOP
Example	HERE FALSE	BTFSC GOTO	FLAG,1 PROCESS	CODE	Example	HERE	CALL	THERE	
	TRUE • •				Before In After Inst	struction PC = A ruction	ddress HE	CRE	
	Before In	struction PC = a ruction if FLAG<1> PC = a if FLAG<1>	address $H$ > = 0, address $FT$ > = 1,	IERE			PC = A TOS = A	ddress TH ddress HH	IERE CRE+1

CLRF	Clear f							
Syntax:	[ <i>label</i> ] C	[ <i>label</i> ] CLRF f						
Operands:	$0 \le f \le 127$							
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$							
Status Affected:	Z							
Encoding:	00	0001	lfff	ffff				
Description:	The conter and the Z	nts of regi bit is set.	ster 'f' are	cleared				
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write register 'f'				
Example	CLRF	FLAG	G_REG					
	Before Instruction FLAG_REG = 0x5A							
		Ζ	=	1				

CLRW	Clear W						
Syntax:	[ label ]	CLRW					
Operands:	None						
Operation:	$00h \rightarrow (V)$	V)					
Status Affected	$1 \rightarrow Z$						
Encoding:		0001	0xxx	xxxx			
Description:	W register	is cleare	d Zero bit	(7) is			
Description.	set.	le cleare		(上) 10			
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	NOP	Process data	Write to W			
Example	CLRW						
Example	Before In	struction					
	Boloro	W =	0x5A				
	After Inst	ruction	0.00				
		vv = Z =	0x00 1				
CLRWDT	Clear Wa	tchdog	Timer				
0 1			_				
Syntax:	[ label ]	CLRWD	I				
Syntax: Operands:	[ <i>label</i> ] None	CLRWD	I				
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None 00h $\rightarrow$ W	CLRWD DT	I				
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$	CLRWD DT F presca	l ler,				
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$	CLRWD DT F presca	l ler,				
Syntax: Operands: Operation: Status Affected:	$\begin{bmatrix} label \\ \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ $TO, PD$	CLRWD DT Γpresca	l ler,				
Syntax: Operands: Operation: Status Affected: Encoding:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ $TO, PD$ $00$	CLRWD DT F presca	l  er, 0110	0100			
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ $\boxed{00}$ CLRWDT in	CLRWD DT F presca	l ler, 0110 resets the	0100 Watch-			
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ CLRWDT in dog Timer, of the WDT are set. \end{bmatrix}$	CLRWD DT F presca 0000 struction It also re T. Status I	0110 resets the provide TO and	0100 Watch- rescaler d PD			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I	0110 resets the poits TO and	0100 Watch- re <u>sca</u> ler d PD			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \end{bmatrix}$	CLRWD DT F presca output struction It also re T. Status I	I 0110 resets the set <u>s</u> the pi bits TO and	0100 Watch- rescaler d PD			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set. 1\\ 1\\ 2\\ 1\\ Q1\\ \end{bmatrix}$	CLRWD DT presca 0000 Istruction It also re T. Status I	I 0110 resets the set <u>s the</u> pi bits TO and	0100 Watch- rescaler d PD			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline O0 \\ CLRWDT in \\ dog Timer, of the WD \\ are set. \\ 1 \\ 1 \\ Q1 \\ \hline Decode \\ \end{bmatrix}$	CLRWD DT presca on on struction It also re T. Status I Q2 NOP	I 0110 resets the province of the province of the process Q3 Process	0100 Watch- rescaler d PD Q4 Clear			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WD are set. 11\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca 0000 Istruction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ CLRWDT indog Timer,of the WDare set. 1\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	0110 resets the sets the provide TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set.11Q1\\ \hline Decode\\ \hline CLRWDT\\ \end{bmatrix}$	CLRWD DT presca oooo struction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline OO\\ CLRWDT indog Timer,of the WDare set.11Q1DecodeCLRWDTBefore In$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	I OIIO resets the sets the ploits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix}   abel   \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou	I ler, 0110 resets the provide the providet the provide the providet the p	0100 Watch- rescaler d PD Q4 Clear WDT Counter			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in dog Timer. of the WD are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou ruction WDT cou	I OIIO resets the sets the province of the process data Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00			
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline O0\\ CLRWDT indog Timer,of the WDare set.11Q1CLRWDTBefore InAfter Inst$	CLRWD DT presca r presca struction It also re T. Status I Q2 NOP struction WDT cou WDT cou WDT cou WDT cou	I ler, 0110 resets the provide the providet the	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00 0			

#### 11.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

#### 1. TppS2ppS

2. TppS

Т			
F	Frequency	Т	Time
Lowerc	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	ТОСКІ
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:		
S			
F	Fall	P	Period
H	High	R	Rise
	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

#### FIGURE 11-1: LOAD CONDITIONS



#### FIGURE 11-7: A/D CONVERSION TIMING



#### **TABLE 11-7: A/D CONVERSION REQUIREMENTS**

Param No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
130	TAD	A/D clock period	PIC16 <b>C</b> 710/711	1.6	_	_	μs	Tosc based, VREF ≥ 3.0V
			PIC16LC710/711	2.0	_	_	μs	Tosc based, VREF full range
			PIC16 <b>C</b> 710/711	2.0*	4.0	6.0	μs	A/D RC mode
			PIC16 <b>LC</b> 710/711	3.0*	6.0	9.0	μs	A/D RC mode
131	TCNV	Conversion time (not including S/H time). (Note 1)		—	9.5	_	TAD	
132	TACQ	Acquisition time		Note 2	20	_	μs	
				5*	_	_	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to AD clock start			Tosc/2§		_	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	Tswc	Switching from co	nvert $\rightarrow$ sample time	1.5§	_	—	TAD	

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

This specification ensured by design. §

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 7.1 for min conditions.



#### TABLE 12-1: RC OSCILLATOR FREQUENCIES

Cevt	Rovt	Average				
UEAL	Next	Fosc @ 5V, 25°C				
22 pF	5k	4.12 MHz	± 1.4%			
	10k	2.35 MHz	± 1.4%			
	100k	268 kHz	± 1.1%			
100 pF	3.3k	1.80 MHz	± 1.0%			
	5k	1.27 MHz	± 1.0%			
	10k	688 kHz	± 1.2%			
	100k	77.2 kHz	± 1.0%			
300 pF	3.3k	707 kHz	± 1.4%			
	5k	501 kHz	± 1.2%			
	10k	269 kHz	± 1.6%			
	100k	28.3 kHz	±1.1%			

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is  $\pm 3$  standard deviation from average value for VDD = 5V.

#### FIGURE 12-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. VDD



#### FIGURE 12-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. VDD



#### FIGURE 12-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. VDD



		$\sim$								
OSC		PIC16C715-04		<pre>PIC16C715-10</pre>		PIC16C715-20		PIC16LC715-04		PIC16C715/JW
	VDD:	4.0V to 5.5V	VDD:	4.5V to 5.5V	VDD:	4.5V to 5.5V	VDD:	2.5V to 5.5V	VDD:	4.0V to 5.5V
PC	IDD:	5 mA max. at 5.5V	IDD:	2.7 mA typ. at \$.5)	IDD:	2.7 mA typ. at 5.5V	IDD:	2.0 mA typ. at 3.0V	IDD:	5 mA max. at 5.5V
	IPD:	21 μA max. at 4V	IPD:	1.5 μA typ. at 4V	IPD:	1.5 μA typ. at 4V	IPD:	0.9 μA typ. at 3V	IPD:	21 μA max. at 4V
	Freq:	4 MHz max.	Freq:	4 MHz max. >	Freq:	4 MHz max.	Freq:	4 MHz max.	Freq:	4 MHz max.
	VDD:	4.0V to 5.5V	VDD:	4.5V to 5.5V /	VDD:	4.5V to 5.5V	VDD:	2.5V to 5.5V	VDD:	4.0V to 5.5V
VT	IDD:	5 mA max. at 5.5V	IDD:	2.7 mA typ. at 5.5V	IDD:	2.7/mA typ. at 5.5V	IDD:	2.0 mA typ. at 3.0V	IDD:	5 mA max. at 5.5V
	IPD:	21 μA max. at 4V	IPD:	1.5 μA typ. at 4V	NgD:	1.5 µA typ at 4V	IPD:	0.9 μA typ. at 3V	IPD:	21 μA max. at 4V
	Freq:	4 MHz max.	Freq:	4 MHz max.	Freq.	4 MHz max.	Freq:	4 MHz max.	Freq:	4 MHz max.
	VDD:	4.5V to 5.5V	VDD:	4.5V to 5.5V	V6p:	4.5V/to 5,5V/			Vdd:	4.5V to 5.5V
це	IDD:	13.5 mA typ. at 5.5V	IDD:	30 mA max. at 5.5V	IDD:	30 mA max. at 5.5V		tuco in US modo	IDD:	30 mA max. at 5.5V
	IPD:	1.5 μA typ. at 4.5V	IPD:	1.5 μA typ. at 4.5V	IPD:	1.5 μA typ. at 4.5V		d use in HS mode	IPD:	1.5 μA typ. at 4.5V
	Freq:	4 MHz max.	Freq:	10 MHz max.	Freq:	20 MHz max.	$\langle \rangle$		Freq:	10 MHz max.
	VDD:	4.0V to 5.5V					YOD:	2.5V to 5.5V	Vdd:	2.5V to 5.5V
	IDD:	52.5 μA typ. at 32 kHz, 4.0V	Dong	tuso in LP modo	Dono		IDD:/	48 μA max. at 32 kHz, 3.0V	IDD:	48 μA max. at 32 kHz, 3.0V
	IPD:	0.9 μA typ. at 4.0V					IPG: /	/5.Ø μA max. at 3.0V	IPD:	5.0 μA max. at 3.0V
	Freq:	200 kHz max.				/	Freq:	/ 200 kHz max.	Freq:	200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

**TABLE 13-1:** 

CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

# 13.1 DC Characteristics: PIC16C715-04 (Commercial, Industrial, Extended) PIC16C715-10 (Commercial, Industrial, Extended) PIC16C715-20 (

			Stand	lard O	oerati	ng Con	ditions (unless otherwise stated)
	PACTERISTICS		Opera	ating te	mpera	ture (	$D^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial)
	RACIERISTICS					-	$40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)
						-	$40^{\circ}$ C $\leq$ TA $\leq$ +125 $^{\circ}$ C (extended)
Param.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
No.							
D001	Supply Voltage	Vdd	4.0	-	5.5	V	XT, RC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002*	RAM Data Retention	Vdr	-	1.5	-	V	Device in SLEEP mode
	Voltage (Note 1)						
D003	VDD start voltage to	VPOR	-	Vss	-	V	See section on Power-on Reset for details
	ensure internal Power-						
	on Reset signal						
D004*	VDD rise rate to ensure	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
	internal Power-on Reset						
	signal						$\langle \rangle \rangle \langle \rangle \sim$
D005	Brown-out Reset Voltage	Bvdd	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.7	5	mA .	XT, RC osc configuration (PIC16C715-04)
						$\land$	Fosc = 4 MHz, VDD = 5.5V (Note 4)
D010				40.5/			
D013			-	13.5	30	AMA	$HS_0SC$ configuration (PIC16C715-20) $E_{OSC} = 20 \text{ MHz}$ $V_{DD} = 5.5V$
DOAL						$\land$	
D015	Brown-out Reset Current		-<	300."	200	K MA	BOR enabled VDD = 5.0V
			$\wedge$				
D020	Power-down Current	IPD `	<u> </u>	10.5	42/	μΑ	VDD = $4.0V$ , WDT enabled, $-40^{\circ}$ C to $+85^{\circ}$ C
D021	(Note 3)			1.5	21	μΑ	$VDD = 4.0V$ , $VDT$ disabled, $-0^{\circ}C$ to $+70^{\circ}C$
D021A		$\land$			30	μΑ	VDD = 4.0V, $VDT$ disabled, -40 C to +85 C
00210				200*	500		
0023	Note 5)	TIROK	/-/	300"	500	μΑ	
		1					

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 51, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which Vod can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

(The)test conditions for all IDD measurements in active operation mode are:

OSCT = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

 $\overline{MCLR}$  = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

#### Applicable Devices 710 71 711 715



#### FIGURE 13-3: CLKOUT AND I/O TIMING

#### TABLE 13-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter	Sym	Characteristic	. <	Min	Typ†	Max	Units	Conditions
No.			$ \longrightarrow $	$\searrow$				
10*	TosH2ckL	OSC1↑ to CLKOUT↓		$\searrow$	15	30	ns	Note 1
11*	TosH2ckH	OSC1 <sup>↑</sup> to CLKOUT <sup>↑</sup>	$\langle \rangle   \rangle$	<u> </u>	15	30	ns	Note 1
12*	TckR	CLKOUT rise time	/ / / / /	V –	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	$\land \land \land \land \land \land$	—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valio	$\land \land \lor$		_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOU	Т	0.25Tcy + 25	_	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT	$\uparrow \swarrow$	0	—	—	ns	Note 1
17*	TosH2ioV	OSC11 (Q1) cycle) to		—	_	80 - 100	ns	
		Port out valid						
18*	TosH2iol	OSC11 (Q2 cycle) to		TBD	_	—	ns	
		Port input invalid (1/9 in hol	d time)					
19*	TioV20sH	Port input valid to OSC11 (	I/O in setup time)	TBD	_	—	ns	
20*	TioR	Port output rise time	PIC16C715	—	10	25	ns	
	$  \setminus \vee$	$\frown$	PIC16LC715		_	60	ns	
21*	Tiok	Port output fall time	PIC16C715		10	25	ns	
	$\left[ \right) \right]$		PIC16LC715	—	—	60	ns	
22	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trisp	RB7:RB4 change INT high	or low time	20	—	_	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

these parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

### FIGURE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING





### TABLE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

Parameter	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
No.	$ \setminus \lor $	$\langle \frown \rangle$					
30	TmcL	MCLR Pulse Width (low)	2	—	_	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	< Tost	Oscillation Start-up Timer Period	-	1024Tosc		-	Tosc = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tıoz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	_	—	2.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—		μs	$VDD \le BVDD (D005)$
36	TPER	Parity Error Reset	_	TBD	_	μs	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



20 MHz

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± 30 PPM

EPSON CA-301 20.000M-C

6.0

#### 15.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

#### 1. TppS2ppS

2. TppS

Т				
F	Frequency	Т	Time	
Lower	case letters (pp) and their meanings:			
рр				
сс	CCP1	OSC	OSC1	
ck	CLKOUT	rd	RD	
cs	CS	rw	RD or WR	
di	SDI	sc	SCK	
do	SDO	SS	SS	
dt	Data in	tO	TOCKI	
io	I/O port	t1	T1CKI	
mc	MCLR	wr	WR	
Uppero	case letters and their meanings:			
S				
F	Fall	P	Period	
н	High	R	Rise	
1	Invalid (Hi-impedance)	V	Valid	
L	Low	Z	Hi-impedance	
FIGURE	15-1: LOAD CONDITIONS			





FIGURE 16-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS VS. VDD



### **APPENDIX C: WHAT'S NEW**

1. Consolidated all pin compatible 18-pin A/D based devices into one data sheet.

### **APPENDIX D: WHAT'S CHANGED**

- 1. Minor changes, spelling and grammatical changes.
- 2. Low voltage operation on the PIC16LC710/711/ 715 has been reduced from 3.0V to 2.5V.
- 3. Part numbers of the PIC16C70 and PIC16C71A have changed to PIC16C710 and PIC16C711, respectively.

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