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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c715-20-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16c715-20-p</a>

## 4.0 MEMORY ORGANIZATION

### 4.1 Program Memory Organization

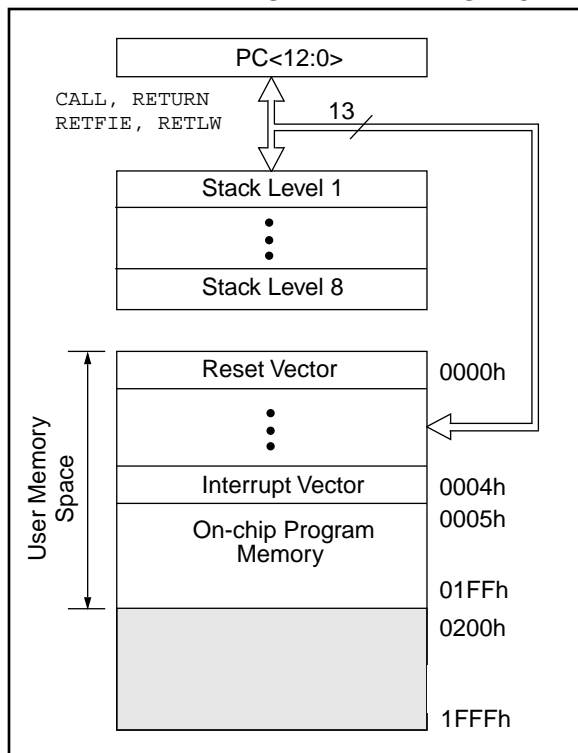
The PIC16C71X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C710	512 x 14	0000h-01FFh
PIC16C71	1K x 14	0000h-03FFh
PIC16C711	1K x 14	0000h-03FFh
PIC16C715	2K x 14	0000h-07FFh

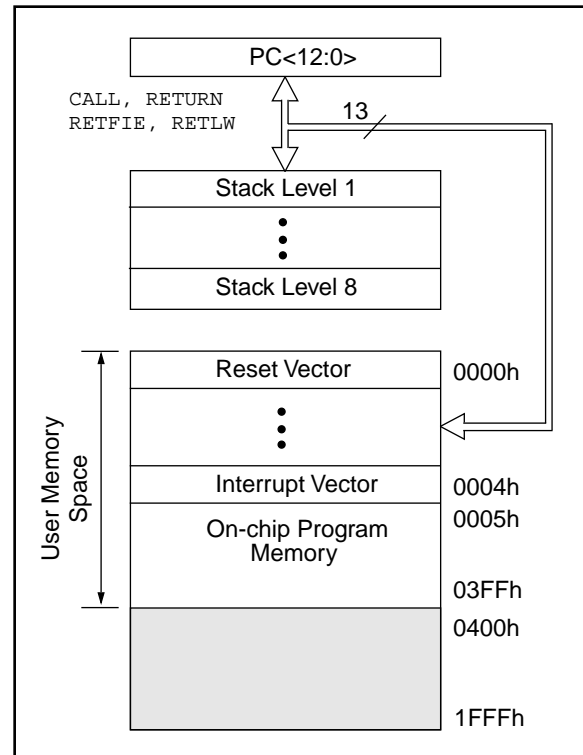
For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

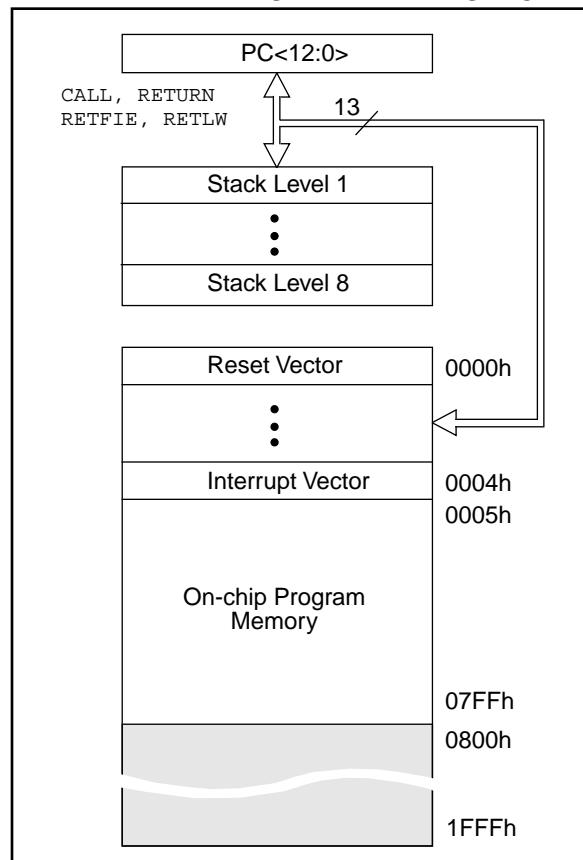
**FIGURE 4-1: PIC16C710 PROGRAM MEMORY MAP AND STACK**



**FIGURE 4-2: PIC16C71/711 PROGRAM MEMORY MAP AND STACK**



**FIGURE 4-3: PIC16C715 PROGRAM MEMORY MAP AND STACK**



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[illegible]

The diagram illustrates the internal circuitry of the RB7:RB6 pins during serial programming. Key components and connections include:

- Inputs:** RBPu(2), Data bus, WR Port, WR TRIS, RD TRIS, RD Port, Set RBIF, and From other RB7:RB4 pins.
- Logic Elements:** Data Latch, TRIS Latch, two 3-state buffers (ST Buffer and TTL Input Buffer), and two D-type flip-flops (Q1 and Q3).
- Outputs:** I/O pin(1), Q1, and Q3.
- Mode:** RB7:RB6 in serial programming mode.

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

# PIC16C71X

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

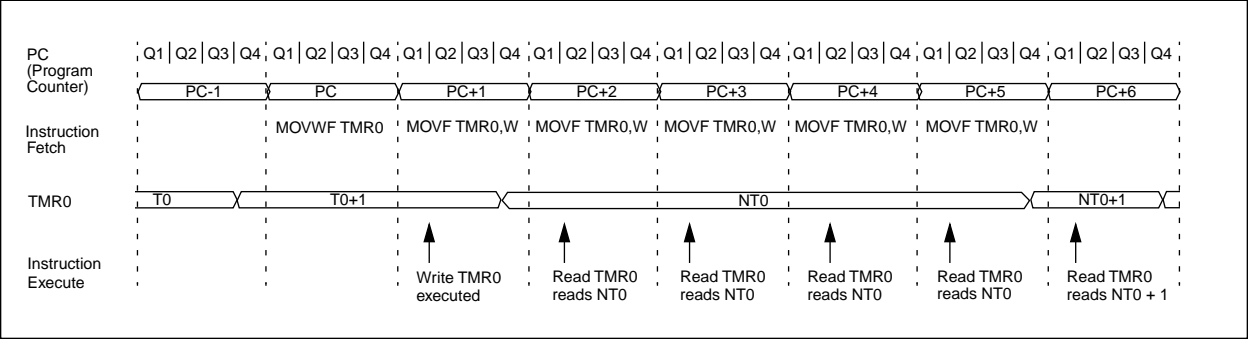
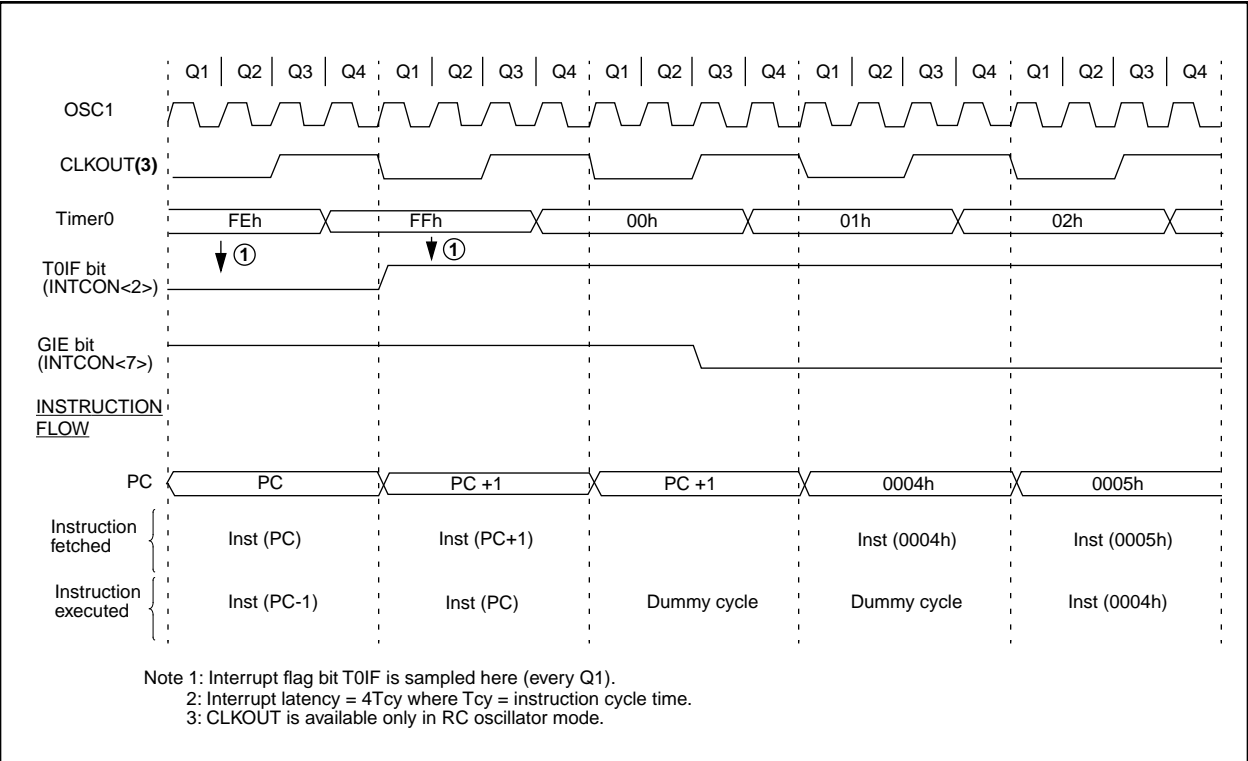


FIGURE 6-4: TIMER0 INTERRUPT TIMING



# PIC16C71X

**FIGURE 8-2: CONFIGURATION WORD, PIC16C710/711**

CP0	CP0	CP0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	PWRT $\overline{\text{E}}$	WDTE	FOSC1	FOSC0	Register: CONFIG Address 2007h
bit13										bit0				
bit 13-7 <b>CP0:</b> Code protection bits <sup>(2)</sup>														
5-4: 1 = Code protection off														
0 = All memory is code protected, but 00h - 3Fh is writable														
bit 6: <b>BODEN:</b> Brown-out Reset Enable bit <sup>(1)</sup>														
1 = BOR enabled														
0 = BOR disabled														
bit 3: <b>PWRT<math>\overline{\text{E}}</math>:</b> Power-up Timer Enable bit <sup>(1)</sup>														
1 = PWRT disabled														
0 = PWRT enabled														
bit 2: <b>WDTE:</b> Watchdog Timer Enable bit														
1 = WDT enabled														
0 = WDT disabled														
bit 1-0: <b>FOSC1:FOSC0:</b> Oscillator Selection bits														
11 = RC oscillator														
10 = HS oscillator														
01 = XT oscillator														
00 = LP oscillator														
Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRT}}\text{E}$ . Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.														
2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.														

**FIGURE 8-3: CONFIGURATION WORD, PIC16C715**

CP1	CP0	CP1	CP0	CP1	CP0	MPEEN	BODEN	CP1	CP0	PWRT $\overline{\text{E}}$	WDTE	FOSC1	FOSC0	Register: CONFIG Address 2007h
-----	-----	-----	-----	-----	-----	-------	-------	-----	-----	----------------------------	------	-------	-------	-----------------------------------

bit13

bit0

bit 13-8    **CP1:CP0:** Code Protection bits <sup>(2)</sup>

5-4:    11 = Code protection off  
10 = Upper half of program memory code protected  
01 = Upper 3/4th of program memory code protected  
00 = All memory is code protected

bit 7:    **MPEEN:** Memory Parity Error Enable  
1 = Memory Parity Checking is enabled  
0 = Memory Parity Checking is disabled

bit 6:    **BODEN:** Brown-out Reset Enable bit <sup>(1)</sup>  
1 = BOR enabled  
0 = BOR disabled

bit 3:    **PWRT $\overline{\text{E}}$ :** Power-up Timer Enable bit <sup>(1)</sup>  
1 = PWRT disabled  
0 = PWRT enabled

bit 2:    **WDTE:** Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled

bit 1-0:    **FOSC1:FOSC0:** Oscillator Selection bits  
11 = RC oscillator  
10 = HS oscillator  
01 = XT oscillator  
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit  $\overline{\text{PWRT}}\text{E}$ . Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.

2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

## 8.4 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST), and Brown-out Reset (BOR)

### 8.4.1 POWER-ON RESET (POR)

Applicable Devices	710	71	711	715
--------------------	-----	----	-----	-----

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

### 8.4.2 POWER-UP TIMER (PWRT)

Applicable Devices	710	71	711	715
--------------------	-----	----	-----	-----

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

### 8.4.3 OSCILLATOR START-UP TIMER (OST)

Applicable Devices	710	71	711	715
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The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

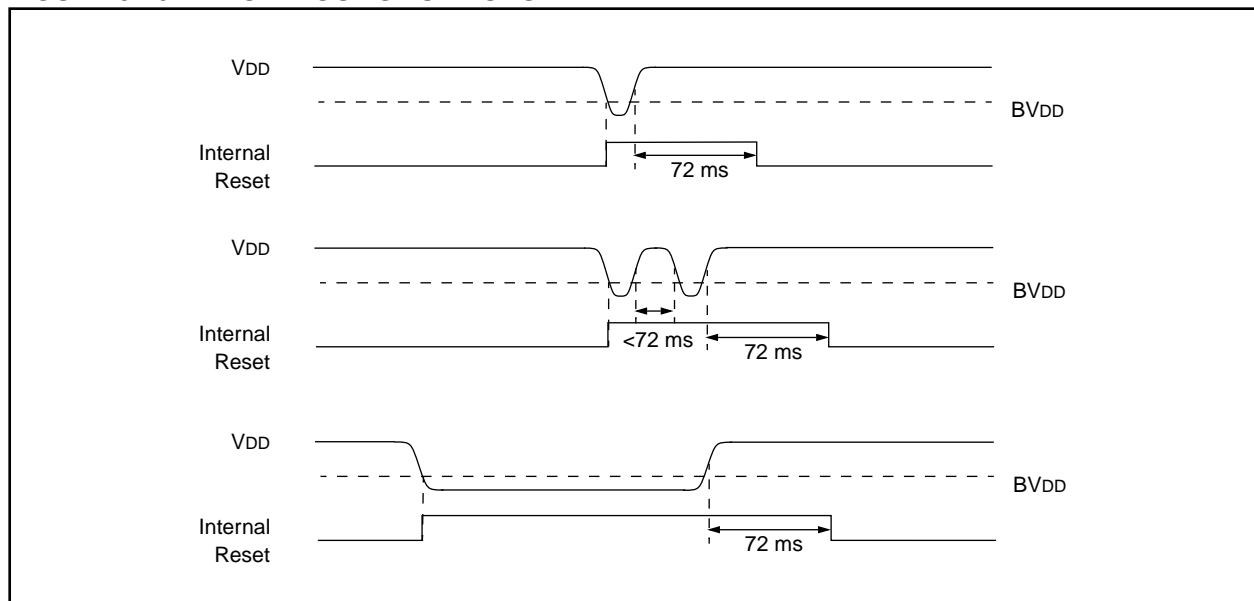
The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

### 8.4.4 BROWN-OUT RESET (BOR)

Applicable Devices	710	71	711	715
--------------------	-----	----	-----	-----

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (3.8V - 4.2V range) for greater than parameter #35, the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 8-10 shows typical brown-out situations.

**FIGURE 8-10: BROWN-OUT SITUATIONS**



BTFSS		Bit Test f, Skip if Set										
Syntax:	[label] BTFSS f,b											
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7											
Operation:	skip if (f<b) = 1											
Status Affected:	None											
Encoding:	<table><tr><td>01</td><td>11bb</td><td>bfff</td><td>ffff</td></tr></table>				01	11bb	bfff	ffff				
01	11bb	bfff	ffff									
Description:	If bit 'b' in register 'f' is '0' then the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.											
Words:	1											
Cycles:	1(2)											
Q Cycle Activity:	<table><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process data</td><td>NOP</td></tr></table>				Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process data	NOP
Q1	Q2	Q3	Q4									
Decode	Read register 'f'	Process data	NOP									
If Skip:	(2nd Cycle)											
	<table><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>NOP</td><td>NOP</td><td>NOP</td><td>NOP</td></tr></table>				Q1	Q2	Q3	Q4	NOP	NOP	NOP	NOP
Q1	Q2	Q3	Q4									
NOP	NOP	NOP	NOP									

**Example**

```

HERE    BTFSC  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •

```

Before Instruction  
PC = address HERE

After Instruction  
if FLAG<1> = 0,  
PC = address FALSE  
if FLAG<1> = 1,  
PC = address TRUE

CALL		Call Subroutine							
Syntax:	[ label ] CALL k								
Operands:	0 ≤ k ≤ 2047								
Operation:	(PC)+ 1 → TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>								
Status Affected:	None								
Encoding:	<table><tr><td>10</td><td>0kkk</td><td>kkkk</td><td>kkkk</td></tr></table>					10	0kkk	kkkk	kkkk
10	0kkk	kkkk	kkkk						
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.								
Words:	1								
Cycles:	2								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
1st Cycle	Decode	Read literal 'k', Push PC to Stack	Process data	Write to PC					
2nd Cycle	NOP	NOP	NOP	NOP					

**Example**

```

HERE    CALL   THERE

```

Before Instruction  
PC = Address HERE

After Instruction  
PC = Address THERE  
TOS = Address HERE+1

# PIC16C71X

## XORLW Exclusive OR Literal with W

Syntax: `[label] XORLW k`

Operands:  $0 \leq k \leq 255$

Operation:  $(W) \text{ .XOR. } k \rightarrow (W)$

Status Affected: Z

Encoding: 

11	1010	kkkk	kkkk
----	------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example: `XORLW 0xAF`  
Before Instruction  
W = 0xB5  
After Instruction  
W = 0x1A

## XORWF Exclusive OR W with f

Syntax: `[label] XORWF f,d`

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:  $(W) \text{ .XOR. } (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding: 

00	0110	dfff	ffff
----	------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity: 

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

Example `XORWF REG 1`  
Before Instruction  
REG = 0xAF  
W = 0xB5  
After Instruction  
REG = 0x1A  
W = 0xB5



## 10.6 PICDEM-1 Low-Cost PIC16/17 Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

## 10.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I<sup>2</sup>C bus and separate headers for connection to an LCD module and a keypad.

## 10.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include

an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

## 10.9 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

## 10.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from PICMASTER, Microchip's Universal Emulator System.

## 11.2 DC Characteristics: PIC16LC710-04 (Commercial, Industrial, Extended) PIC16LC711-04 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated)							
DC CHARACTERISTICS							
Operating temperature							
0°C ≤ TA ≤ +70°C (commercial)							
-40°C ≤ TA ≤ +85°C (industrial)							
-40°C ≤ TA ≤ +125°C (extended)							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage						
	Commercial/Industrial	VDD	2.5	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
	Extended	VDD	3.0	-	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	μA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3)	IPD	-	7.5	30	μA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	μA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	μA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D021B			-	0.9	10	μA	VDD = 3.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = VDD/2R_{ext}$  (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

12.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C710 AND PIC16C711

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

**Note:** The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 12-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

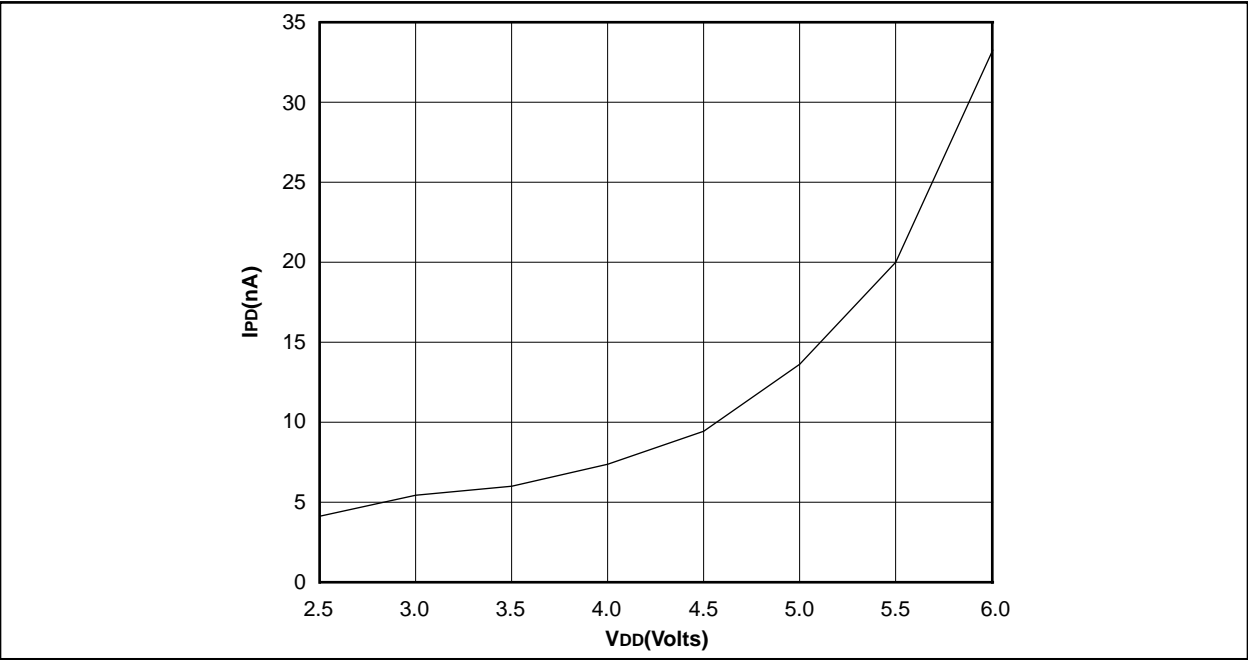
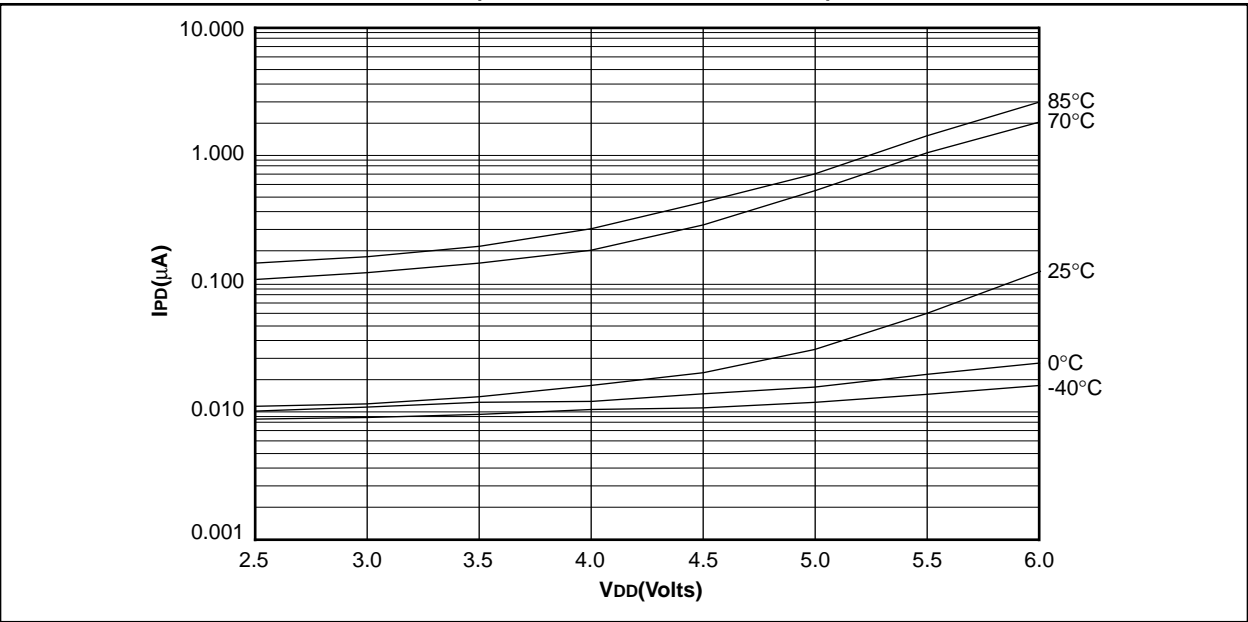


FIGURE 12-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)



# PIC16C71X

Applicable Devices 71071711715

FIGURE 12-29: TYPICAL I<sub>DD</sub> vs. FREQUENCY  
(HS MODE, 25°C)

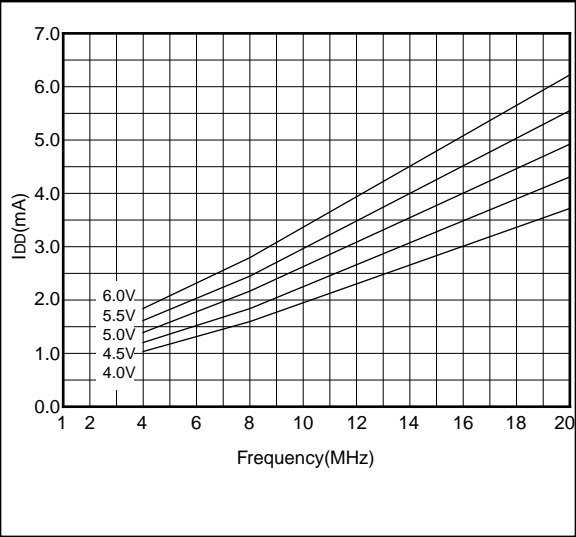
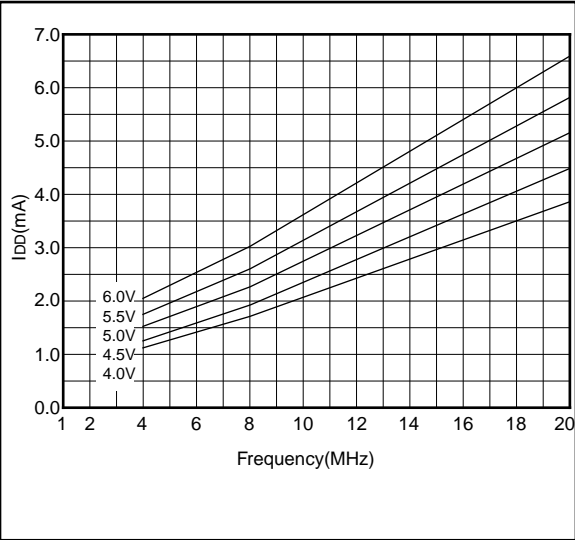


FIGURE 12-30: MAXIMUM I<sub>DD</sub> vs. FREQUENCY  
(HS MODE, -40°C TO 85°C)



# PIC16C71X

Applicable Devices 710 71 711 715

<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.							
<b>DC CHARACTERISTICS</b>							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D090	<b>Output High Voltage</b> I/O ports (Note 3)	VOH	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD - 0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD - 0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D100	<b>Capacitive Loading Specs on Output Pins</b> OSC2 pin	COSC2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

- The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- Negative current is defined as coming out of the pin.

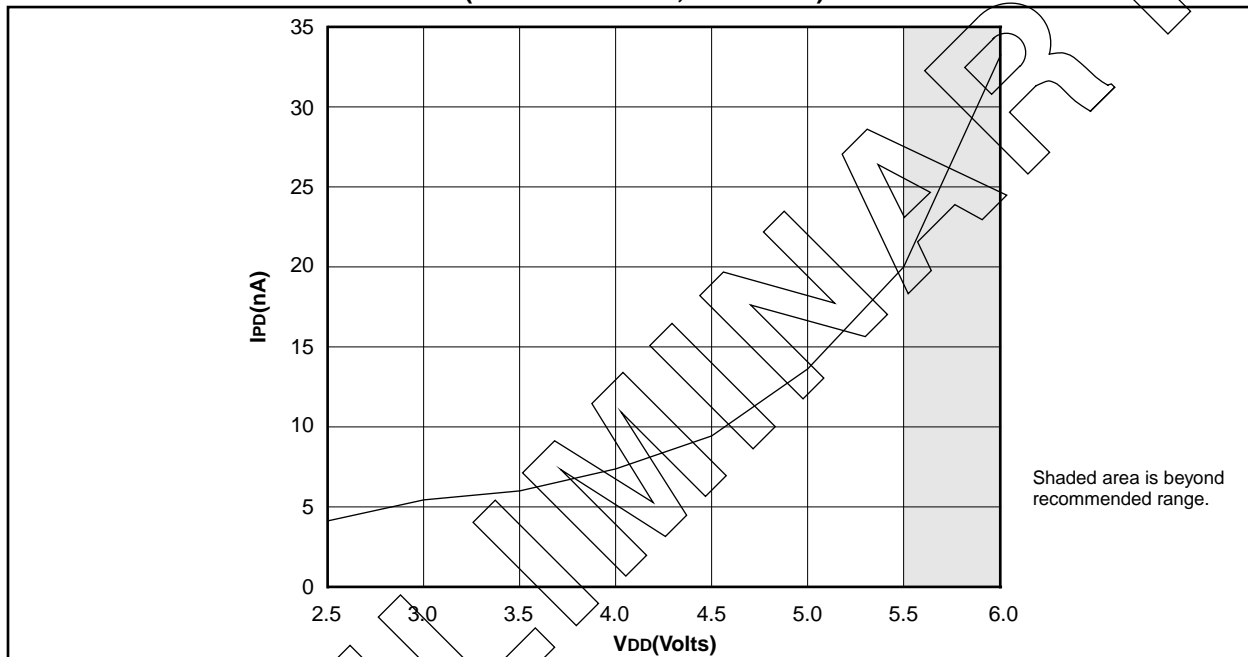
## 14.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C715

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

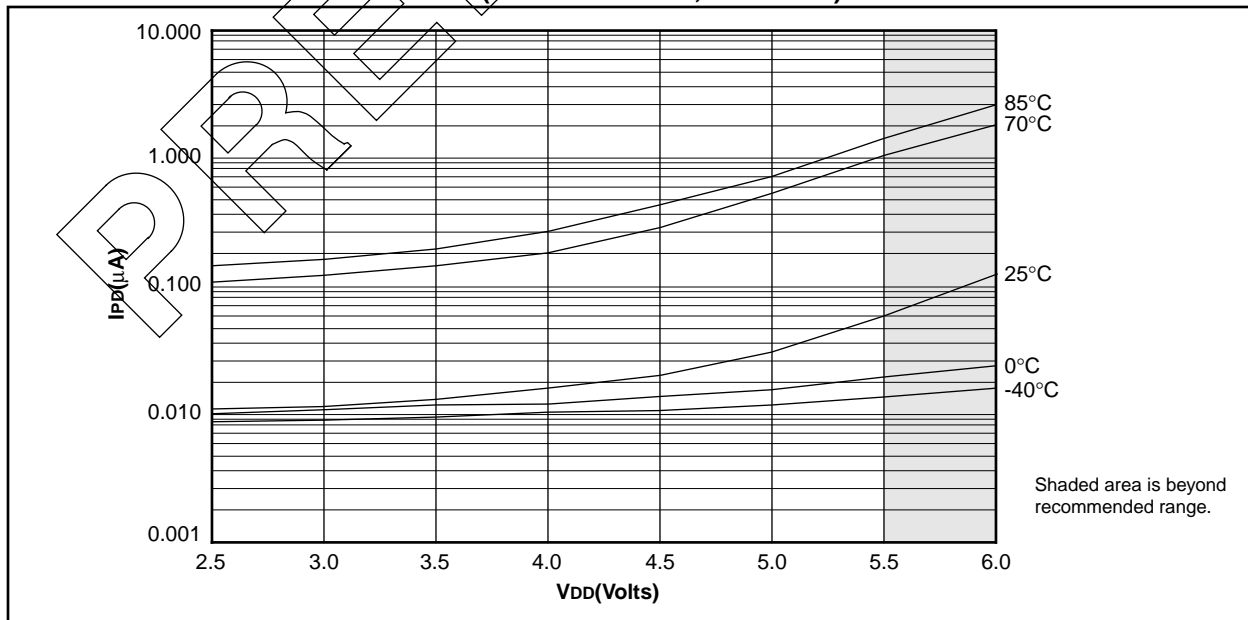
In some graphs or tables the data presented are outside specified operating range (i.e., outside specified  $V_{DD}$  range). This is for information only and devices are guaranteed to operate properly only within the specified range.

**Note:** The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C, while 'max' or 'min' represents (mean +3 $\sigma$ ) and (mean -3 $\sigma$ ) respectively where  $\sigma$  is standard deviation.

**FIGURE 14-1: TYPICAL  $I_{PD}$  vs.  $V_{DD}$  (WDT DISABLED, RC MODE)**



**FIGURE 14-2: MAXIMUM  $I_{PD}$  vs.  $V_{DD}$  (WDT DISABLED, RC MODE)**



# PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 14-12: TYPICAL  $I_{DD}$  vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

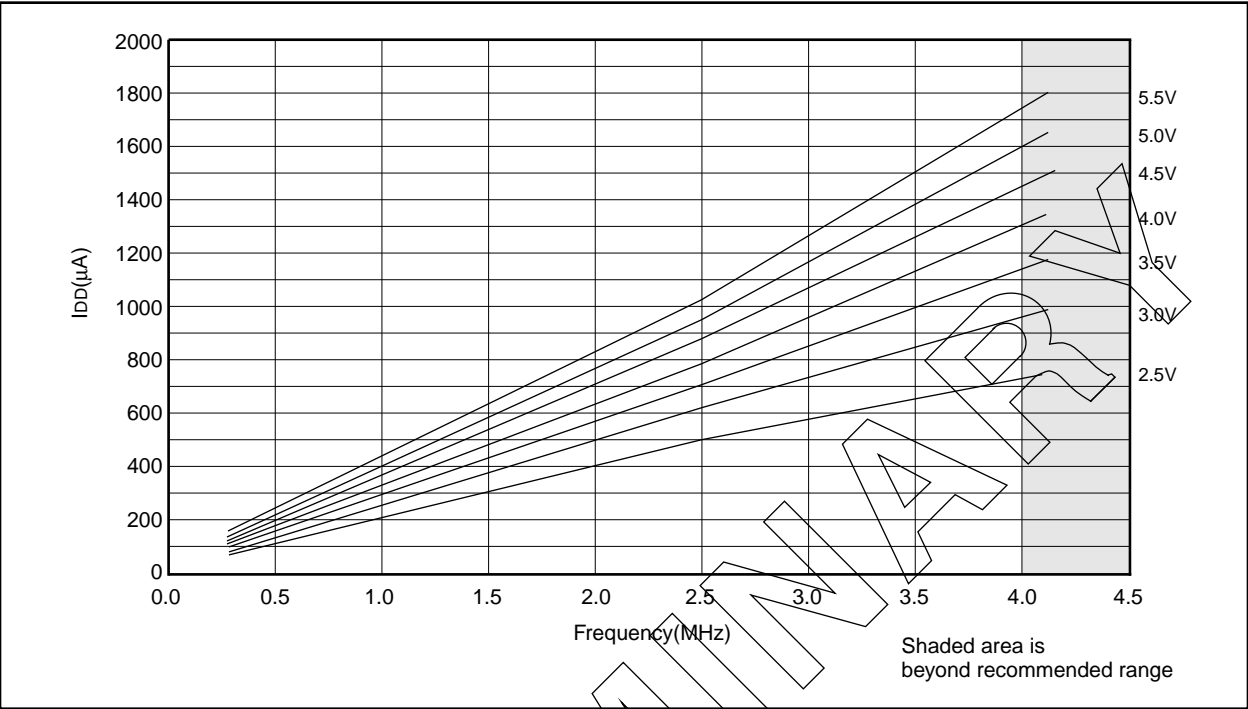
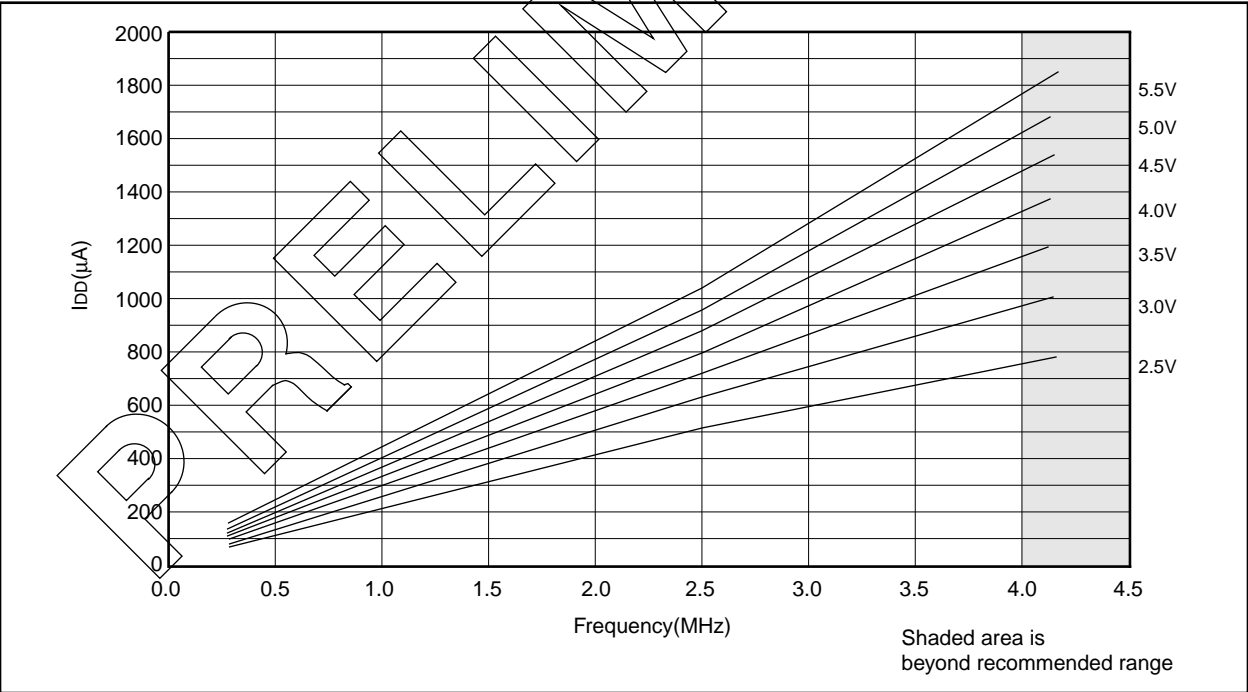


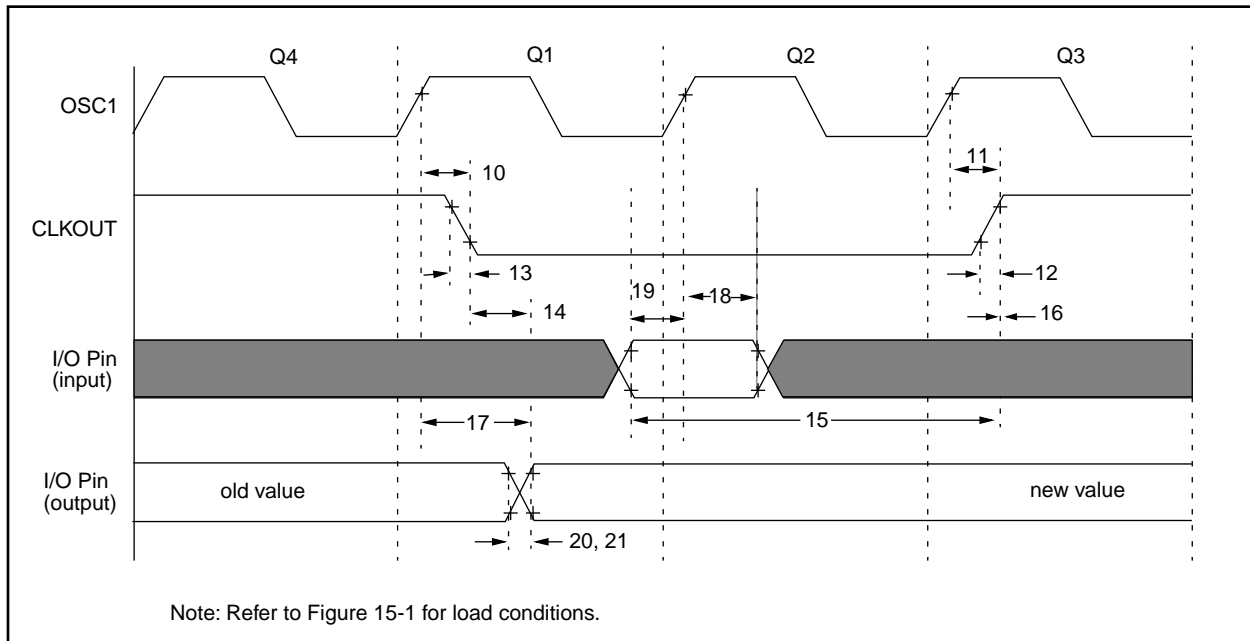
FIGURE 14-13: MAXIMUM  $I_{DD}$  vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)



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**FIGURE 15-3: CLKOUT AND I/O TIMING**



**TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5T <sub>cy</sub> + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	0.25T <sub>cy</sub> + 25	—	—	ns	Note 1
16*	TckH2ioL	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	
18*	TosH2ioL	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C71	100	—	ns	
			PIC16LC71	200	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	PIC16C71	—	10	ns	
			PIC16LC71	—	—	60	ns
21*	TioF	Port output fall time	PIC16C71	—	10	ns	
			PIC16LC71	—	—	60	ns
22††*	Tinp	INT pin high or low time	20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time	20	—	—	ns	

\* These parameters are characterized but not tested.

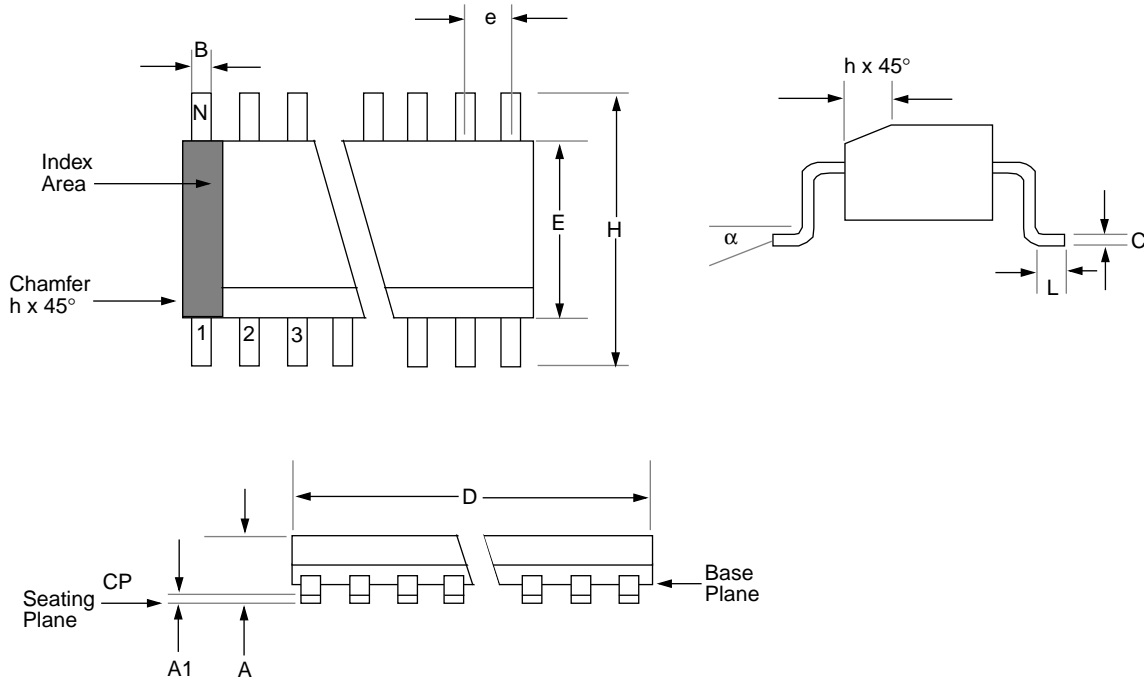
†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x T<sub>osc</sub>.



## 17.3 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)(SO)



Package Group: Plastic SOIC (SO)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	18	18		18	18	
CP	—	0.102		—	0.004	

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