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## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5КВ (2К х 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c715-20e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## FIGURE 3-1: PIC16C71X BLOCK DIAGRAM



IADLL	· +-2.	FICTOCI	13 SFLC			KL0131						
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR, PER	Value on all other resets (3)	
Bank 0				•	<u>.</u>	•	•					
00h <sup>(1)</sup>	INDF	Addressing	this location	uses conter	nts of FSR to	address dat	a memory (n	ot a physical	register)	0000 0000	0000 0000	
01h	TMR0	Timer0 mod	er0 module's register xxxx xxxx uuuu									
02h <sup>(1)</sup>	PCL	Program Co	ounter's (PC)	Least Signi	ficant Byte					0000 0000	0000 0000	
03h <sup>(1)</sup>	STATUS	IRP <sup>(4)</sup>	RP1 <sup>(4)</sup>	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu	
04h <sup>(1)</sup>	FSR	Indirect data	a memory ac	dress pointe	er					XXXX XXXX	uuuu uuuu	
05h	PORTA	—	—	—	PORTA Dat	ta Latch whe	n written: PC	RTA pins wh	nen read	x 0000	u 0000	
06h	PORTB	PORTB Dat	ta Latch whe	n written: PC	ORTB pins w	hen read				XXXX XXXX	uuuu uuuu	
07h	-	Unimpleme	nted							-	—	
08h	-	Unimpleme	nted							-	—	
09h	_	Unimpleme	nted		_					_	_	
0Ah <b>(1,2)</b>	PCLATH	_	—	_	Write Buffe	r for the uppe	er 5 bits of th	e Program C	ounter	0 0000	0 0000	
0Bh <sup>(1)</sup>	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u	
0Ch	PIR1	_	ADIF	_	_					-0	-0	
0Dh		Unimpleme	nted								_	
0Eh		Unimpleme	nted							_	_	
0Fh	-	Unimpleme	nted							_	_	
10h		Unimpleme	nted								_	
11h		Unimpleme	nted							_	_	
12h	-	Unimpleme	nted							_	_	
13h	-	Unimpleme	nted							-	—	
14h		Unimpleme	nted							_	_	
15h	-	Unimpleme	nted							_	_	
16h	-	Unimpleme	nted							-	—	
17h		Unimpleme	nted							_	_	
18h	-	Unimpleme	nted							_	_	
19h	-	Unimpleme	nted							-	—	
1Ah	-	Unimpleme	nted							-	—	
1Bh	_	Unimpleme	nted							-	_	
1Ch	—	Unimpleme	nted							—	—	
1Dh	—	Unimpleme	nted							_	—	
1Eh	ADRES	A/D Result	Register							XXXX XXXX	uuuu uuuu	
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	0000 00-0	

TABLE 4-2: PIC16C715 SPECIAL FUNCTION REGISTER SUMMARY

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C715, always maintain these bits clear.

## 4.2.2.5 PIR1 REGISTER

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This register contains the individual flag bits for the Peripheral interrupts.

# **Note:** Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

## FIGURE 4-11: PIR1 REGISTER (ADDRESS 0Ch)



## 4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The upper bits (PC<12:8>) are not readable, but are indirectly writable through the PCLATH register. On any reset, the upper bits of the PC will be cleared. Figure 4-14 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0>  $\rightarrow$  PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3>  $\rightarrow$  PCH).

## FIGURE 4-14: LOADING OF PC IN DIFFERENT SITUATIONS



## 4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note *"Implementing a Table Read"* (AN556).

## 4.3.2 STACK

The PIC16CXX family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instruc- tions, or the vectoring to an interrupt address.	Note 1:	There are no status bits to indicate stack overflow or stack underflow conditions.
	Note 2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

## 4.4 <u>Program Memory Paging</u>

The PIC16C71X devices ignore both paging bits (PCLATH<4:3>, which are used to access program memory when more than one page is available. The use of PCLATH<4:3> as general purpose read/write bits for the PIC16C71X is not recommended since this may affect upward compatibility with future products.

## 7.5 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

## 7.6 <u>A/D Accuracy/Error</u>

The absolute accuracy specified for the A/D converter includes the sum of all contributions for quantization error, integral error, differential error, full scale error, offset error, and monotonicity. It is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the A/D converter is specified at <  $\pm$ 1 LSb for VDD = VREF (over the device's specified operating range). However, the accuracy of the A/D converter will degrade as VDD diverges from VREF.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. Quantization error is typically  $\pm$  1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to increase the resolution of the A/D converter.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. Integral non-linearity error measures the actual code transition versus the ideal code transition adjusted by the gain error for each code.

Differential non-linearity measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator. TAD must not violate the minimum and should be  $\leq 8 \ \mu s$  for preferred operation. This is because TAD, when derived from TOSC, is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

## 7.7 Effects of a RESET

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted.

The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.

## 7.8 Connection Considerations

If the input voltage exceeds the rail values (VSS or VDD) by greater than 0.2V, then the accuracy of the conversion is out of specification.

Note:	Care must be taken when using the RA0
	pin in A/D conversions due to its proximity
	to the OSC1 pin.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 k $\Omega$  recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

## 11.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

## 1. TppS2ppS

2. TppS

Т			
F	Frequency	Т	Time
Lowerc	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	ТОСКІ
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:		
S			
F	Fall	P	Period
H	High	R	Rise
	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

## FIGURE 11-1: LOAD CONDITIONS



## TABLE 11-6:A/D CONVERTER CHARACTERISTICS:<br/>PIC16C710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16C710/711-10 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16LC710/711-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)<br/>PIC16LC710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
A01	NR	Resolution			8-bits	bit	$VREF=VDD,VSS\leqAIN\leqVREF$
A02	EABS	Absolute error	_	_	< ± 1	LSb	$VREF = VDD,  VSS \leq AIN \leq VREF$
A03	EIL	Integral linearity error	_	—	< ± 1	LSb	$VREF=VDD,VSS\leqAIN\leqVREF$
A04	Edl	Differential linearity error	_	—	< ± 1	LSb	$VREF=VDD,VSS\leqAIN\leqVREF$
A05	Efs	Full scale error	_	—	< ± 1	LSb	$VREF = VDD,  VSS \leq AIN \leq VREF$
A06	EOFF	Offset error	_	—	< ± 1	LSb	$VREF = VDD,  VSS \leq AIN \leq VREF$
A10	—	Monotonicity	—	guaranteed	-	—	$VSS \leq VAIN \leq VREF$
A20	Vref	Reference voltage	2.5V	_	Vdd + 0.3	V	
A25	VAIN	Analog input voltage	Vss - 0.3	_	Vref + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	_	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	_	180	_	μA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	_	1000	μΑ	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1. During A/D Conversion cycle

These parameters are characterized but not tested.

\*

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current.

The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

FIGURE 12-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)



FIGURE 12-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



## FIGURE 12-25: TYPICAL IDD vs. FREQUENCY (LP MODE, 25°C)







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FIGURE 12-27: TYPICAL IDD vs. FREQUENCY (XT MODE, 25°C)



FIGURE 12-28: MAXIMUM IDD vs. FREQUENCY (XT MODE, -40°C TO 85°C)



## FIGURE 12-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)



## FIGURE 12-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)



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## 13.0 ELECTRICAL CHARACTERISTICS FOR PIC16C715

## Absolute Maximum Ratings †

Ambient temperature under bias	
Storage temperature	65°C\to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.3V to (VDR + 0.3V)
Voltage on VDD with respect to Vss	
Voltage on MCLR with respect to Vss	
Voltage on RA4 with respect to Vss	0 to +14V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into Vod pin	
Input clamp current, Iικ (VI < 0 or VI > VDD)	
Output clamp current, Ioк (Vo < 0 or Vo > Voo)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA	200 mA
Maximum current sourced by PORTA	200 mA
Maximum current sunk by PORTB	200 mA
Maximum current sourced by PORTB	200 mA
<b>Note 1:</b> Power dissipation is calculated as follows: Rdis = VDD x {IDD - $\Sigma$ IOH} + $\Sigma$ {	(VDD - VOH) x IOH} + $\Sigma$ (VOI x IOL).
+ NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cau	ise permanent damage to the

TNOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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	Standard Operating Conditions (unless otherwise stated)										
		O of the standard operating conditions (unless other wise stated)									
		Operati	ng tempe	latur	e UC	<u> </u>	$TA \leq +70 \text{ C}$ (commercial)				
DC CHAR	RACTERISTICS				-40		$TA \leq +85 C$ (industrial)				
		<b>.</b> .			-40	C _≤	$IA \leq +125 C$ (extended)				
		Operati	ng voltage	e VDI	D range	as des	cribed in DC spec Section 13.1				
		and Se	ction 13.2	•							
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions				
No.				†							
	Output High Voltage										
D090	I/O ports (Note 3)	Voн	VDD - 0.7	-	-	V	IOH = -3.0 mA. VDØ =\4.5V.				
			_				-40°C to +85°C				
			Vpp - 0 7		_		$10 = -25 \text{ m/s} \sqrt{108} + 15 \text{ V}$				
DUSUA			0.7			V V	$-10^{\circ}$ C to $\pm 125^{\circ}$ C				
<b>D</b> 000			V								
D092	OSC2/CLKOUT (RC osc coniig)		0.7	-	-	V	10H = -1.3  IIIA,  VDD = 4.5V,				
							-40°C to +85°C				
D092A			VDD - 0.7	] -	-		$IOP_{=} - 1.0 \text{ mA}, VDD_{=} 4.5V,$				
							-40°C to +(25°C				
	Capacitive Loading Specs on					$\frown$					
	Output Pins					/ r					
D100	OSC2 pin	Cosc <sub>2</sub>	-	-	15		IPXT, HS and LP modes when				
					$\wedge$	' \	external clock is used to drive				
					$\langle \rangle$	$ \setminus $	0801				
D101	All $I/O$ pips and OSC2 (in RC mode)	Cio	_		-50-						
			· · ·	Ķ	-30-						

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin:

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## 13.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS



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## 13.5 <u>Timing Diagrams and Specifications</u>

## FIGURE 13-2: EXTERNAL CLOCK TIMING



## TABLE 13-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fos	External CI KIN Frequency	DC		4	MHZ	XTosc mode
	100	(Note 1)		_	4		HS osc mode (PIC16C715-04)
			DC	_	20	MHZ	HS osc mode (PIC16C715-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	—		MHz	RC osc mode
		(Note 1)	0.1		4	MHz	XT osc mode
			4	$  \langle \rangle$	4	MHz	HS osc mode (PIC16C715-04)
			4	$\wedge - \land$	10	MHz	HS osc mode (PIC16C715-10)
			4		20	MHz	HS osc mode (PIC16C715-20)
		<	5	$\bigvee \downarrow \setminus$	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	$\searrow$	_	ns	XT osc mode
		(Note 1)	250	Ň	—	ns	HS osc mode (PIC16C715-04)
			100	$  $	—	ns	HS osc mode (PIC16C715-10)
			50	—	-	ns	HS osc mode (PIC16C715-20)
			> 5	—		μs	LP osc mode
		Oscillator Period	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (PIC16C715-04)
			100	_	250	ns	HS osc mode (PIC16C715-10)
		$() \subset ($	50	_	250	ns	HS osc mode (PIC16C715-20)
		$\bigvee \land \searrow$	5	_	_	μs	LP osc mode
2 /	TGY	Instruction Cycle Time (Note 1)	200	—	DC	ns	Tcy = 4/Fosc
3/	ŢosĻ,	External Clock in (OSC1) High	50	—	—	ns	XT oscillator
$  \setminus \setminus$	TosH	or Low Time	2.5	—	—	μs	LP oscillator
	$\leq$		10			ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise		—	25	ns	XT oscillator
	TosF	or Fall Time	—	—	50	ns	LP oscillator
			-	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C715.

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FIGURE 14-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)



FIGURE 14-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



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## 15.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial)

DC CHARACTERISTICS				ard Op ing terr	eratin perati	<b>g Cond</b> ure 0° -4	litions (unless otherwise stated) $^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $^{\circ}O^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	-	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.8	3.3	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3)	IPD	- - -	7 1.0 1.0	28 14 16	μΑ μΑ μΑ	$VDD = 4.0V, WDT enabled, -40^{\circ}C to +85^{\circ}C$ $VDD = 4.0V, WDT disabled, -0^{\circ}C to +70^{\circ}C$ $VDD = 4.0V, WDT disabled, -40^{\circ}C to +85^{\circ}C$

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD  $\overline{MCLR} = VDD$ ; WDT enabled/disabled as specified.

The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

## FIGURE 15-3: CLKOUT AND I/O TIMING



TABLE 10 0. CERCOT AND 10 THINKS REGOLIERIENTS
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Parameter	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
NO.								
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time			5	15	ns	Note 1
13*	TckF	CLKOUT fall time		5	15	ns	Note 1	
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid	b		_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOU	0.25Tcy + 25	—	—	ns	Note 1	
16*	TckH2iol	Port in hold after CLKOUT	0	_	—	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		_	_	80 - 100	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to	PIC16 <b>C</b> 71	100	—	_	ns	
		Port input invalid (I/O in hold time)	PIC16 <b>LC</b> 71	200	—	_	ns	
19*	TioV2osH	Port input valid to OSC11 (	(I/O in setup time)	0	_	—	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 71		10	25	ns	
			PIC16 <b>LC</b> 71	—	—	60	ns	
21*	TioF	Port output fall time	PIC16 <b>C</b> 71	—	10	25	ns	
			PIC16 <b>LC</b> 71		_	60	ns	
22††*	Tinp	INT pin high or low time		20	—		ns	
23††*	Trbp	RB7:RB4 change INT high	or low time	20	_	_	ns	

\* These parameters are characterized but not tested.

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

these parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

## FIGURE 16-14: MAXIMUM IDD vs. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)



TO bit	
TOSE bit	
TRISA Register	
TRISB Register	
Two's Complement	7
U	

0	
Upward Compatibility	
UV Erasable Devices	

## W

W Register	
ALU	7
Wake-up from SLEEP	
Watchdog Timer (WDT)	
WDT	
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Timeout	
WDT Period	65
WDTE bit	
Z	

Z bit .		
Zero b	bit	7

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