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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c715t-04e-ss

TABLE 3-1: **PIC16C710/71/711/715 PINOUT DESCRIPTION**

Pin Name	DIP Pin#	SSOP Pin#[4]	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	16	I	ST/CMOS[3]	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	4	4	4	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	17	19	17	I/O	TTL	RA0 can also be analog input0
RA1/AN1	18	20	18	I/O	TTL	RA1 can also be analog input1
RA2/AN2	1	1	1	I/O	TTL	RA2 can also be analog input2
RA3/AN3/VREF	2	2	2	I/O	TTL	RA3 can also be analog input3 or analog reference voltage
RA4/T0CKI	3	3	3	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	7	6	I/O	TTL/ST[1]	RB0 can also be the external interrupt pin.
RB1	7	8	7	I/O	TTL	
RB2	8	9	8	I/O	TTL	
RB3	9	10	9	I/O	TTL	
RB4	10	11	10	I/O	TTL	Interrupt on change pin.
RB5	11	12	11	I/O	TTL	Interrupt on change pin.
RB6	12	13	12	I/O	TTL/ST[2]	Interrupt on change pin. Serial programming clock.
RB7	13	14	13	I/O	TTL/ST[2]	Interrupt on change pin. Serial programming data.
VSS	5	4, 6	5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input   O = output   I/O = input/output   P = power
          — = Not used   TTL = TTL input   ST = Schmitt Trigger input

Note 1:   This buffer is a Schmitt Trigger input when configured as the external interrupt.
      2:   This buffer is a Schmitt Trigger input when used in serial programming mode.
      3:   This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.
      4:   The PIC16C71 is not available in SSOP package.

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.
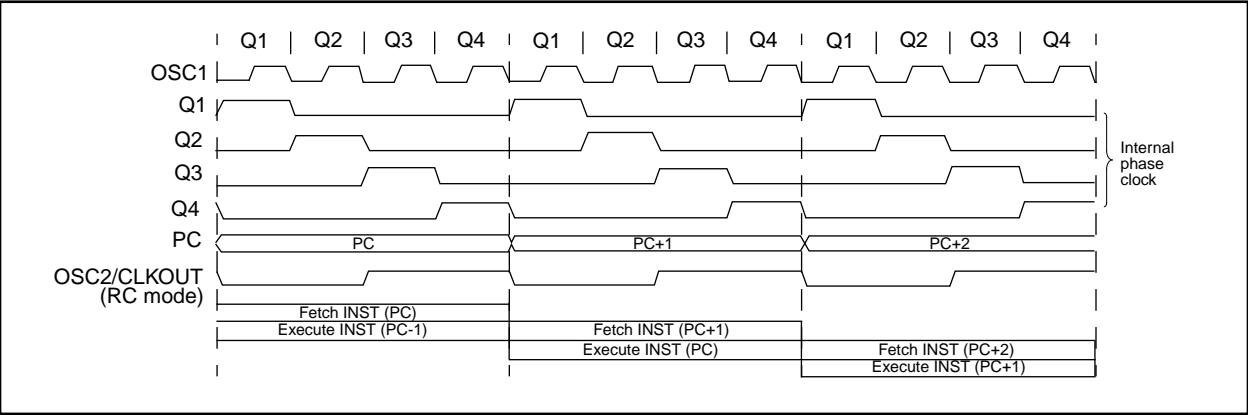
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.
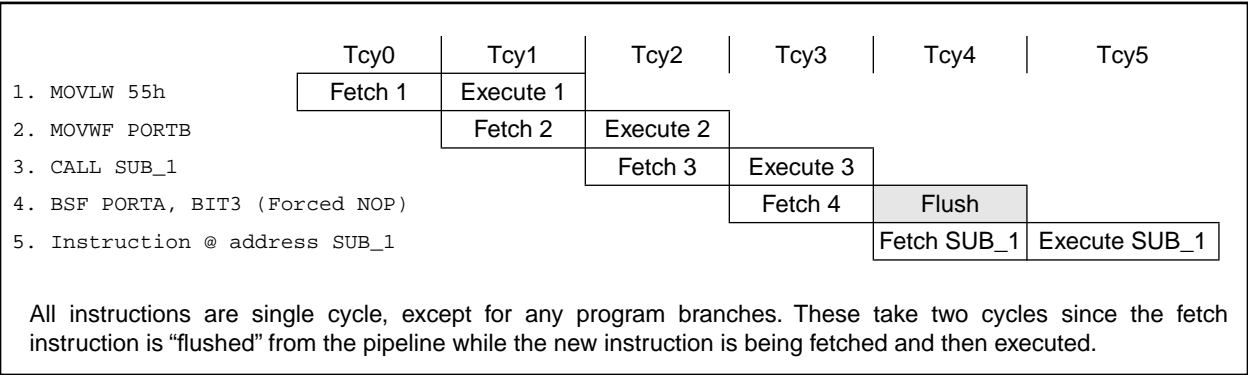
7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

| Applicable Devices | 710 | 71 | 711 | 715 |

The analog-to-digital (A/D) converter module has four analog inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 7-1 and Figure 7-2, controls the operation of the A/D module. The ADCON1 register, shown in Figure 7-3 configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

FIGURE 7-1: ADCON0 REGISTER (ADDRESS 08h), PIC16C710/71/711

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	__ (1)	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADIF	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from an RC oscillation)

bit 5: **Unimplemented:** Read as '0'.

bit 4-3: **CHS1:CHS0:** Analog Channel Select bits
00 = channel 0, (RA0/AN0)
01 = channel 1, (RA1/AN1)
10 = channel 2, (RA2/AN2)
11 = channel 3, (RA3/AN3)

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **ADIF:** A/D Conversion Complete Interrupt Flag bit
1 = conversion is complete (must be cleared in software)
0 = conversion is not complete

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Note 1: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

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8.6   Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 8-1 stores and restores the STATUS and W registers. The user register, STATUS_TEMP, must be defined in bank 0.

The example:

a)   Stores the W register.
b)   Stores the STATUS register in bank 0.
c)   Executes the ISR code.
d)   Restores the STATUS register (and bank select bit).
e)   Restores the W register.

EXAMPLE 8-1:   SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP              ;Copy W to TEMP register, could be bank one or zero
SWAPF    STATUS,W           ;Swap status to be saved into W
MOVWF    STATUS_TEMP        ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W      ;Swap STATUS_TEMP register into W
                           ;(sets bank to original state)
MOVWF    STATUS             ;Move W into STATUS register
SWAPF    W_TEMP,F           ;Swap W_TEMP
SWAPF    W_TEMP,W           ;Swap W_TEMP into W
```

8.7   Watchdog Timer (WDT)

| Applicable Devices | 710 | 71 | 711 | 715 |

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit WDTE (Section 8.1).

8.7.1   WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

8.7.2   WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

> **Note:** When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 8-20:   WATCHDOG TIMER BLOCK DIAGRAM
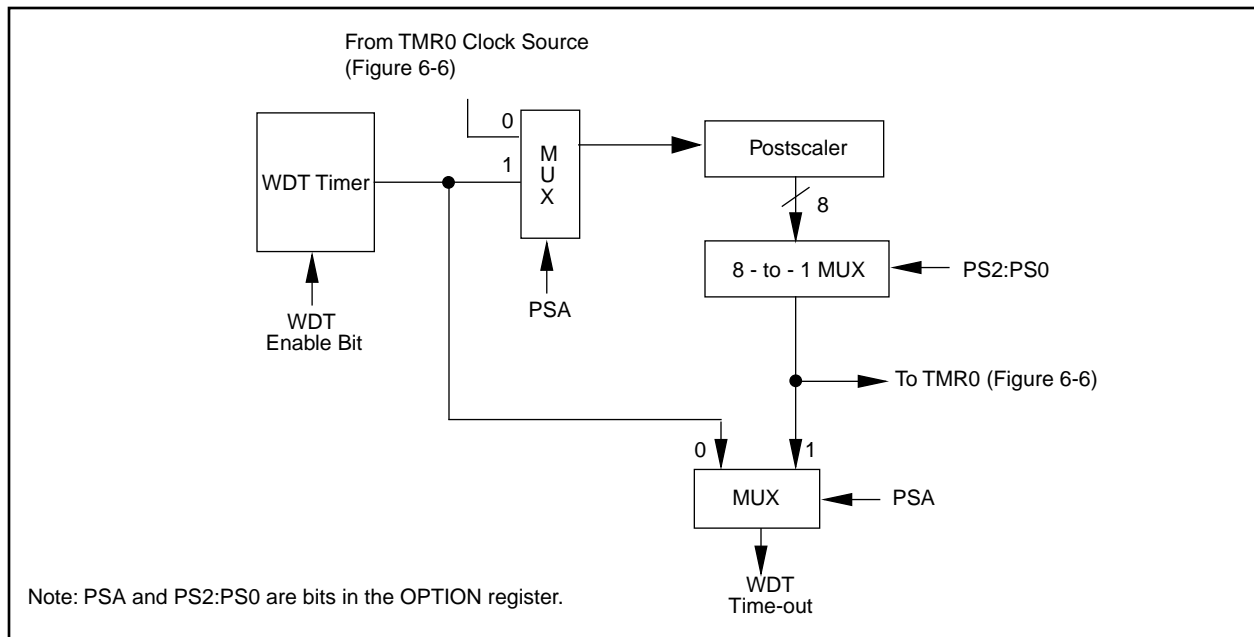
FIGURE 8-21:   SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN[1]	CP1	CP0	PWRTE[1]	WDTE	FOSC1	FOSC0
81h,181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Figure 8-1, Figure 8-2 and Figure 8-3 for operation of these bits.

PIC16C71X

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Encoding:	01 00bb bfff ffff
Description:	Bit 'b' in register 'f' is cleared.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write register 'f'

Example   BCF   FLAG_REG, 7

Before Instruction
        FLAG_REG = 0xC7
After Instruction
        FLAG_REG = 0x47

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Encoding:	01 01bb bfff ffff
Description:	Bit 'b' in register 'f' is set.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write register 'f'

Example   BSF   FLAG_REG,   7

Before Instruction
        FLAG_REG = 0x0A
After Instruction
        FLAG_REG = 0x8A

BTFSC	Bit Test, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Encoding:	01 10bb bfff ffff
Description:	If bit 'b' in register 'f' is '1' then the next instruction is executed. If bit 'b', in register 'f', is '0' then the next instruction is discarded, and a NOP is executed instead, making this a 2T$_{CY}$ instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	NOP

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
NOP	NOP	NOP	NOP

Example
```
HERE    BTFSC  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
        PC =   address HERE
After Instruction
        if FLAG<1> = 0,
        PC =   address TRUE
        if FLAG<1>=1,
        PC =   address FALSE

BTFSS	**Bit Test f, Skip if Set**
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$
Operation:	skip if (f\<b\>) = 1
Status Affected:	None

Encoding:

01	11bb	bfff	ffff

Description:	If bit 'b' in register 'f' is '0' then the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	NOP

If Skip: (2nd Cycle)

Q1	Q2	Q3	Q4
NOP	NOP	NOP	NOP

Example

```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
        PC =   address HERE
After Instruction
        if FLAG\<1\> = 0,
        PC =   address FALSE
        if FLAG\<1\> = 1,
        PC =   address TRUE

CALL	**Call Subroutine**
Syntax:	[*label*] CALL k
Operands:	$0 \leq k \leq 2047$
Operation:	(PC)+ 1$\rightarrow$ TOS, k $\rightarrow$ PC\<10:0\>, (PCLATH\<4:3\>) $\rightarrow$ PC\<12:11\>
Status Affected:	None

Encoding:

10	0kkk	kkkk	kkkk

Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits \<10:0\>. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.
Words:	1
Cycles:	2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k', Push PC to Stack	Process data	Write to PC
2nd Cycle	NOP	NOP	NOP	NOP

Example

```
HERE    CALL    THERE
```

Before Instruction
        PC = Address HERE
After Instruction
        PC = Address THERE
        TOS = Address HERE+1

SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) - (W) $\rightarrow$ (dest)
Status Affected:	C, DC, Z

Encoding:

00	0010	dfff	ffff

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

Example 1:   SUBWF   REG1,1

Before Instruction

REG1	=	3
W	=	2
C	=	?
Z	=	?

After Instruction

REG1	=	1
W	=	2
C	=	1; result is positive
Z	=	0

Example 2:   Before Instruction

REG1	=	2
W	=	2
C	=	?
Z	=	?

After Instruction

REG1	=	0
W	=	2
C	=	1; result is zero
Z	=	1

Example 3:   Before Instruction

REG1	=	1
W	=	2
C	=	?
Z	=	?

After Instruction

REG1	=	0xFF
W	=	2
C	=	0; result is negative
Z	=	0

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f<3:0>) $\rightarrow$ (dest<7:4>), (f<7:4>) $\rightarrow$ (dest<3:0>)
Status Affected:	None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest

Example   SWAPF REG,   0

Before Instruction

REG1	=	0xA5

After Instruction

REG1	=	0xA5
W	=	0x5A

TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	$5 \leq f \leq 7$
Operation:	(W) $\rightarrow$ TRIS register f;
Status Affected:	None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

11.0   ELECTRICAL CHARACTERISTICS FOR PIC16C710 AND PIC16C711

Absolute Maximum Ratings †

Ambient temperature under bias..-55 to +125°C

Storage temperature .... -65°C to +150°C

Voltage on any pin with respect to VSS (except VDD, $\overline{MCLR}$, and RA4)..-0.3V to (VDD + 0.3V)

Voltage on VDD with respect to VSS .... -0.3 to +7.5V

Voltage on $\overline{MCLR}$ with respect to VSS...0 to +14V

Voltage on RA4 with respect to Vss ....0 to +14V

Total power dissipation (Note 1)...1.0W

Maximum current out of VSS pin ....300 mA

Maximum current into VDD pin ....250 mA

Input clamp current, IIK (VI < 0 or VI > VDD)..± 20 mA

Output clamp current, IOK (VO < 0 or VO > VDD) ....± 20 mA

Maximum output current sunk by any I/O pin...25 mA

Maximum output current sourced by any I/O pin ....25 mA

Maximum current sunk by PORTA ....200 mA

Maximum current sourced by PORTA ....200 mA

Maximum current sunk by PORTB..200 mA

Maximum current sourced by PORTB..200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD - VOH) x IOH} + Σ(VOl x IOL)

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 11-1:   CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C710-04 PIC16C711-04	PIC16C710-10 PIC16C711-10	PIC16C710-20 PIC16C711-20	PIC16LC710-04 PIC16LC711-04	PIC16C710/JW PIC16C711/JW
RC	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA typ. at 3.0V IPD: 5.0 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq:4 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 µA typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 6.0V IDD: 3.8 mA typ. at 3.0V IPD: 5.0 µA typ. at 3V Freq: 4 MHz max.	VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 21 µA max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq:20 MHz max.	Not recommended for use in HS mode	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 µA typ. at 4.5V Freq: 10 MHz max.
LP	VDD: 4.0V to 6.0V IDD: 52.5 µA typ. at 32 kHz, 4.0V IPD: 0.9 µA typ. at 4.0V Freq: 200 kHz max.	Not recommended for use in LP mode	Not recommended for use in LP mode	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.	VDD: 2.5V to 6.0V IDD: 48 µA max. at 32 kHz, 3.0V IPD: 5.0 µA max. at 3.0V Freq: 200 kHz max.

12.0   DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C710 AND PIC16C711

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (i.e., outside specified V$_{DD}$ range). This is for information only and devices are guaranteed to operate properly only within the specified range.

> **Note:** The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at, 25°C, while 'max' or 'min' represents (mean +3σ) and (mean -3σ) respectively where σ is standard deviation.

FIGURE 12-1:   TYPICAL I$_{PD}$ vs. V$_{DD}$ (WDT DISABLED, RC MODE)
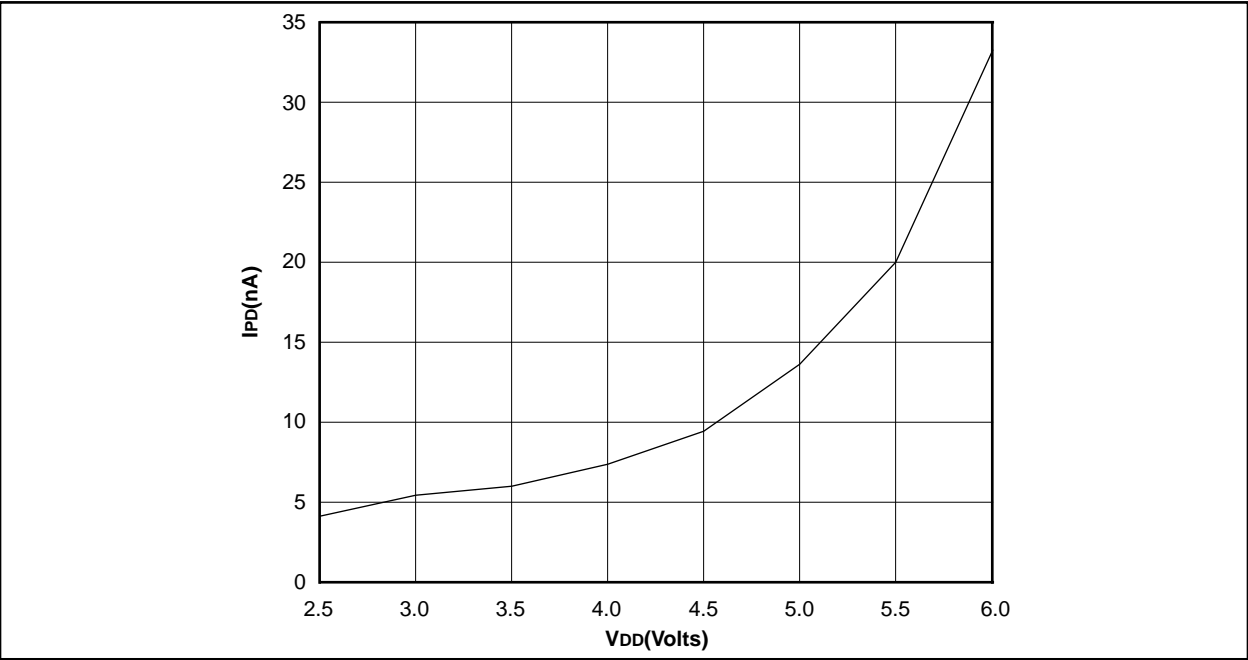
FIGURE 12-2:   MAXIMUM I$_{PD}$ vs. V$_{DD}$ (WDT DISABLED, RC MODE)
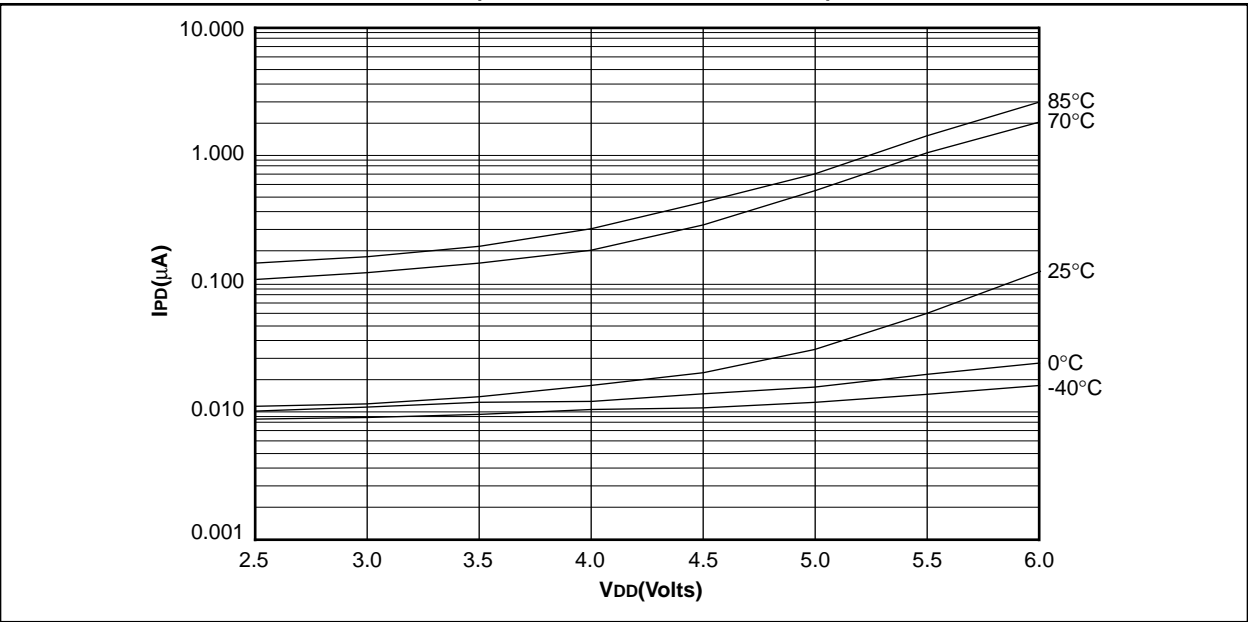
FIGURE 12-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)
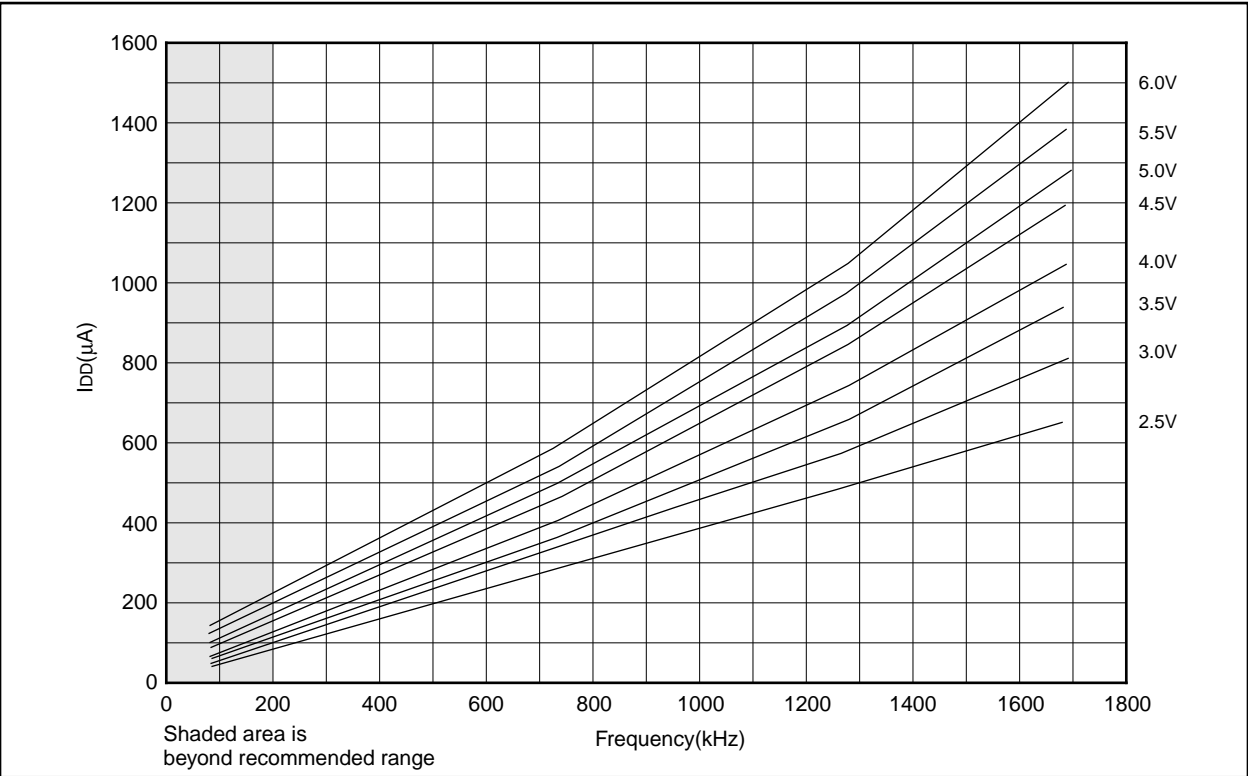
FIGURE 12-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)
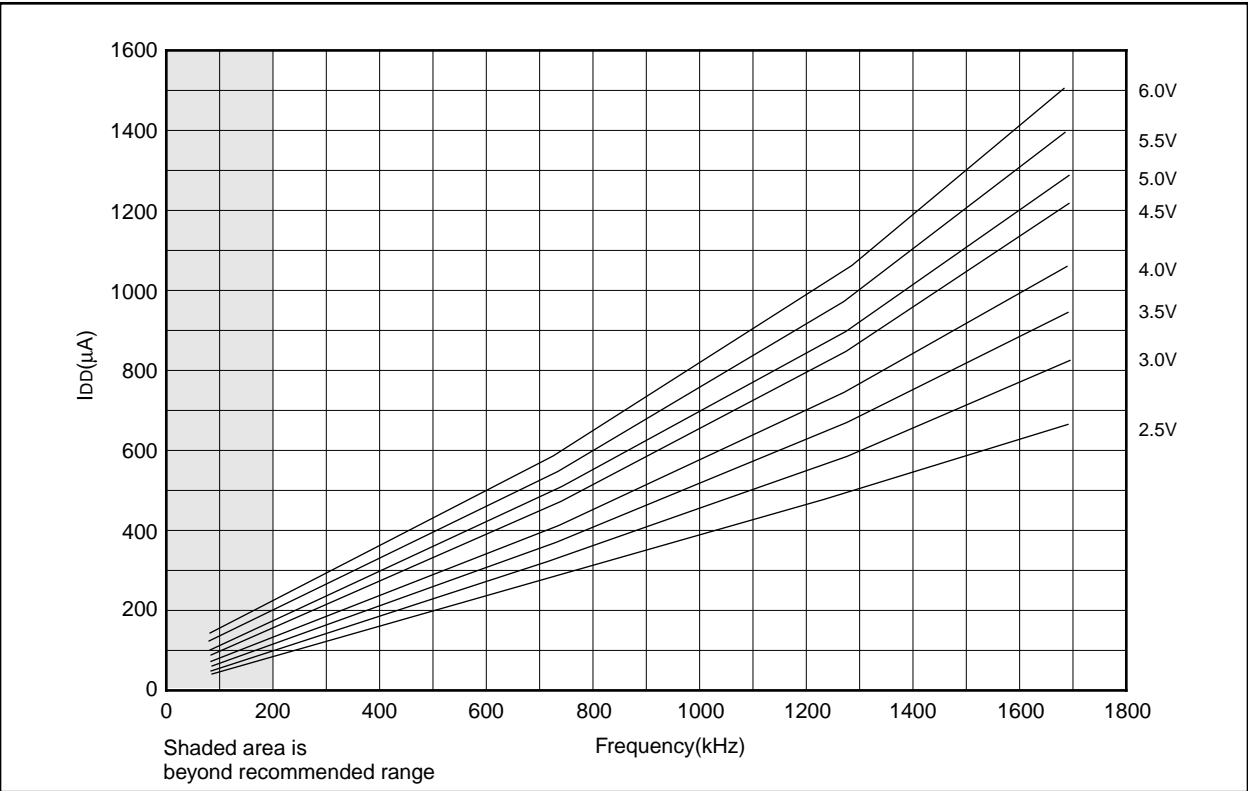
PIC16C71X

FIGURE 12-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

FIGURE 12-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

FIGURE 12-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)
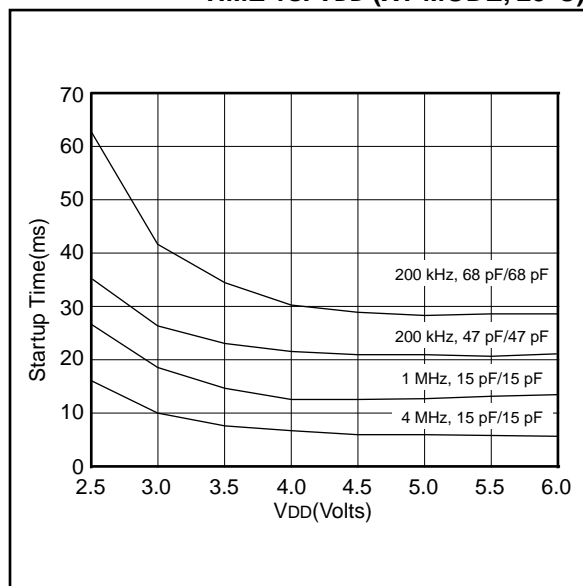
TABLE 12-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Crystals Used		
32 kHz	Epson C-001R32.768K-A	± 20 PPM
200 kHz	STD XTL 200.000KHz	± 20 PPM
1 MHz	ECS ECS-10-13-1	± 50 PPM
4 MHz	ECS ECS-40-20-1	± 50 PPM
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM

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TABLE 13-6: A/D CONVERTER CHARACTERISTICS:
PIC16C715-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C715-10 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C715-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	N$_R$	Resolution	—	—	8-bits	—	V$_{REF}$ = V$_{DD}$, V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	N$_{INT}$	Integral error	—	—	less than ±1 LSb	—	V$_{REF}$ = V$_{DD}$, V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	N$_{DIF}$	Differential error	—	—	less than ±1 LSb	—	V$_{REF}$ = V$_{DD}$, V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	N$_{FS}$	Full scale error	—	—	less than ±1 LSb	—	V$_{REF}$ = V$_{DD}$, V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	N$_{OFF}$	Offset error	—	—	less than ±1 LSb	—	V$_{REF}$ = V$_{DD}$, V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	—	Monotonicity	—	guaranteed	—	—	V$_{SS}$ ≤ A$_{IN}$ ≤ V$_{REF}$
	V$_{REF}$	Reference voltage	2.5V	—	V$_{DD}$ + 0.3	V	
	V$_{AIN}$	Analog input voltage	V$_{SS}$ - 0.3	—	V$_{REF}$ + 0.3	V	
	Z$_{AIN}$	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
	I$_{AD}$	A/D conversion current (V$_{DD}$)	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
	I$_{REF}$	V$_{REF}$ input current (Note 2)	—	—	1 / 10	mA / μA	During sampling / All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: V$_{REF}$ current is from RA3 pin or V$_{DD}$ pin, whichever is selected as reference input.

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FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)

Shaded area is beyond recommended range.
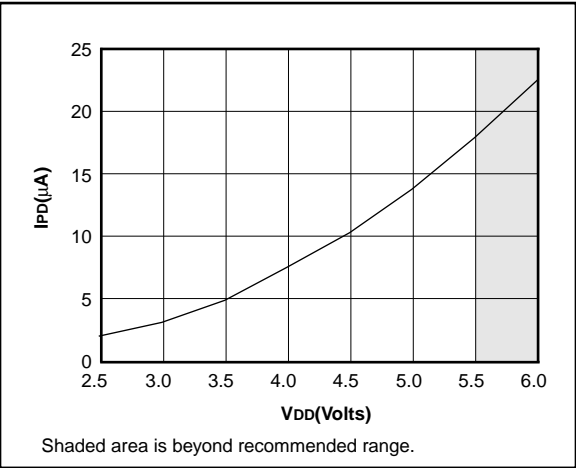
FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)

Shaded area is beyond recommended range.
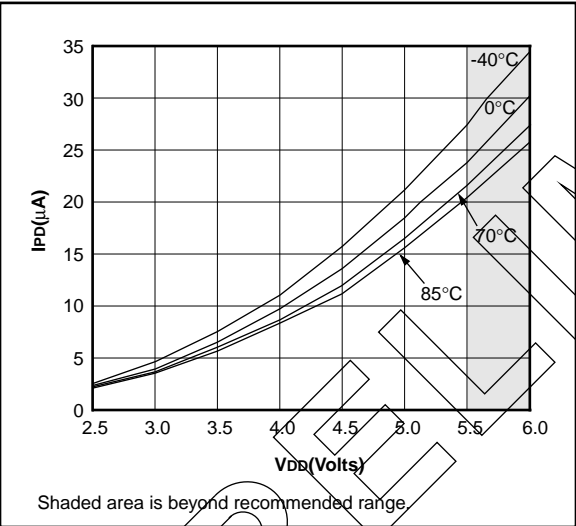
FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

Shaded area is beyond recommended range.
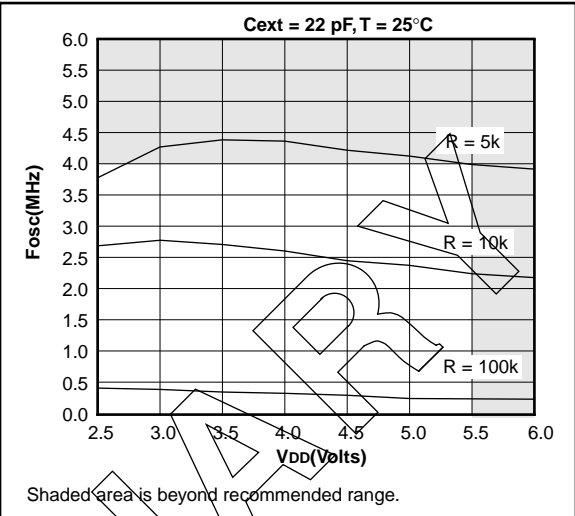
FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

Shaded area is beyond recommended range.
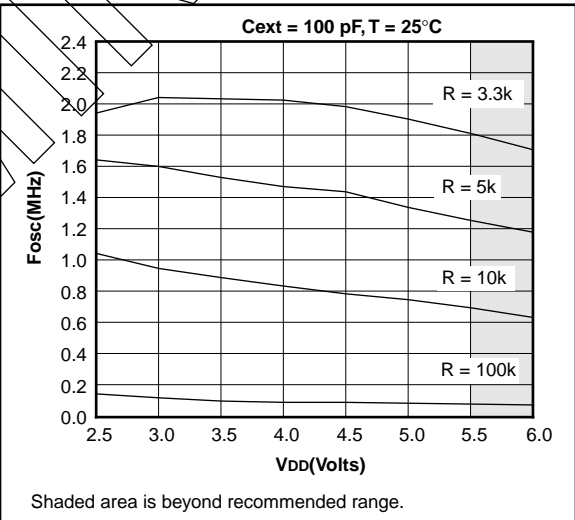
FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

Shaded area is beyond recommended range.

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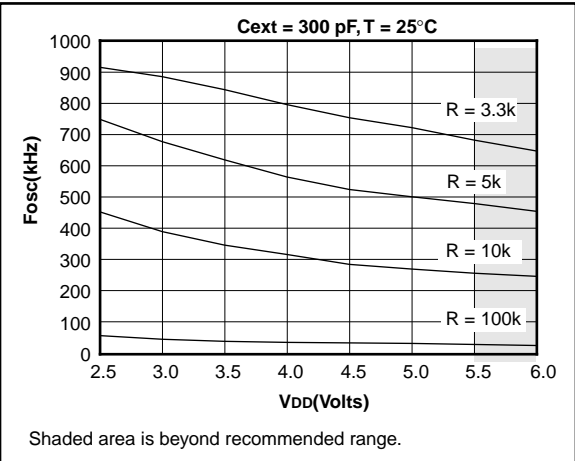
FIGURE 14-8: TYPICAL IPD vs. VDD BROWN-OUT DETECT ENABLED (RC MODE)

This shaded region represents the built-in hysteresis of the brown-out reset circuitry.

Shaded area is beyond recommended range.

FIGURE 14-9: MAXIMUM IPD vs. VDD BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

This shaded region represents the built-in hysteresis of the brown-out reset circuitry.

Shaded area is beyond recommended range.

FIGURE 14-10: TYPICAL IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

Shaded area is beyond recommended range.
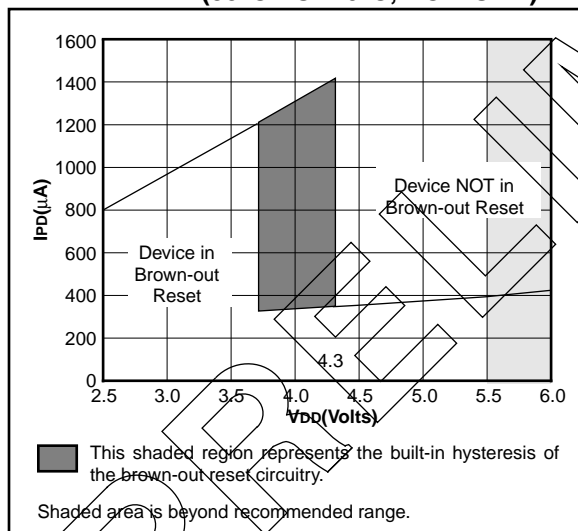
FIGURE 14-11: MAXIMUM IPD vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

Shaded area is beyond recommended range.
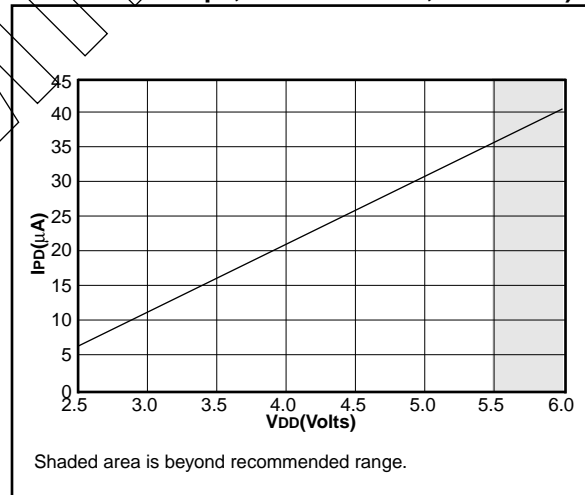
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15.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial)
PIC16C71-20 (Commercial, Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0˚C $\leq$ TA $\leq$ +70˚C (commercial) -40˚C $\leq$ TA $\leq$ +85˚C (industrial)				
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	- -	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010 D013	Supply Current (Note 2)	IDD	- -	1.8 13.5	3.3 30	mA mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4) HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3)	IPD	- - -	7 1.0 1.0	28 14 16	µA µA µA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C

    *   These parameters are characterized but not tested.

    †   Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1:   This is the limit to which VDD can be lowered without losing RAM data.

      2:   The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

      3:   The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

      4:   For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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FIGURE 16-14: MAXIMUM IDD VS. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)

Curves labeled: 6.0, 5.5, 5.0, 4.5, 4.0, 3.5, 3.0

Axes: IDD (µA) vs. Frequency (Hz)
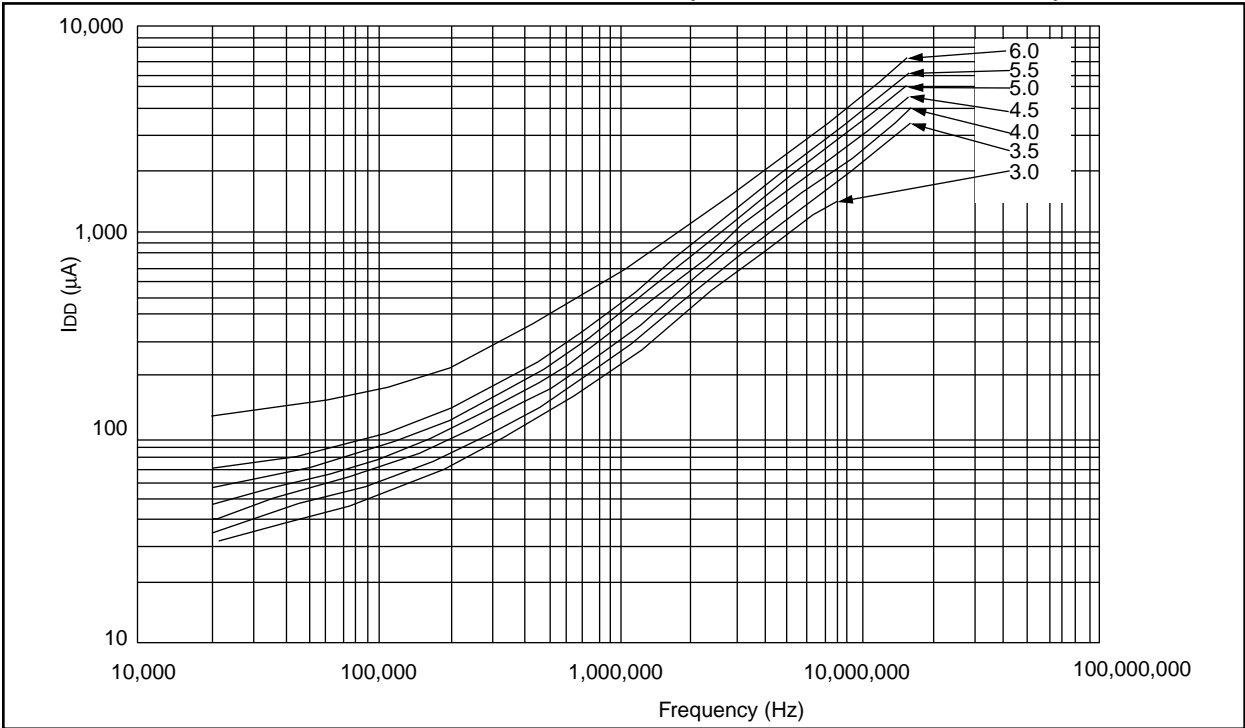
FIGURE 16-15: WDT TIMER TIME-OUT PERIOD VS. VDD

Curves labeled: Max, 85°C; Max, 70°C; Min, 0°C; Min, -40°C; Typ, 25°C

Axes: WDT Period (ms) vs. VDD (Volts)
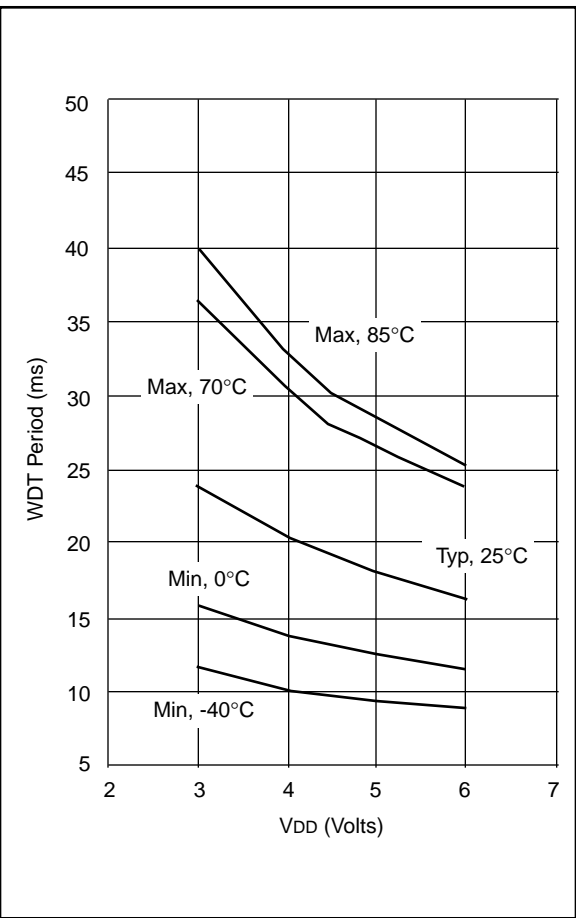
FIGURE 16-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR VS. VDD

Curves labeled: Max, -40°C; Typ, 25°C; Min, 85°C

Axes: gm (µA/V) vs. VDD (Volts)
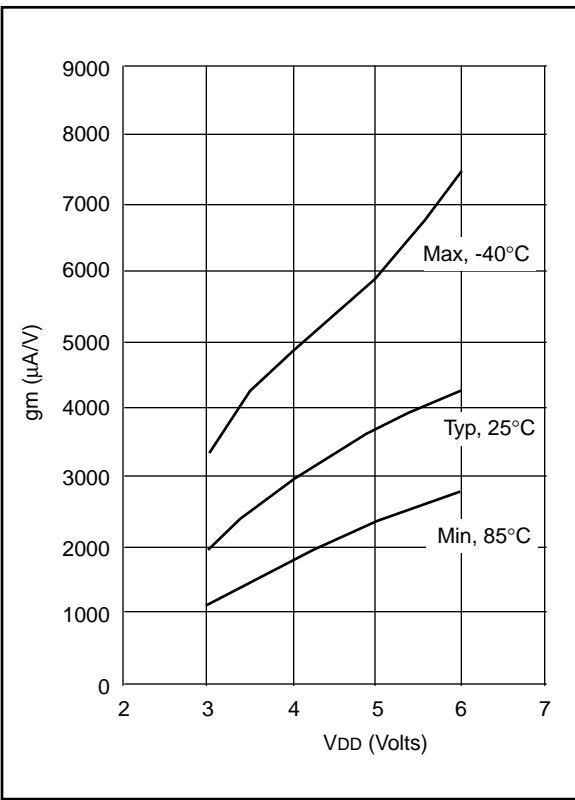
Data based on matrix samples. See first page of this section for details.

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