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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 × 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c715t-20-so

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FIGURE 3-1: PIC16C71X BLOCK DIAGRAM



4.2.2.1 STATUS REGISTER

Applicable Devices 710 71 711 715

The STATUS register, shown in Figure 4-7, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

- Note 1: For those devices that do not use bits IRP and RP1 (STATUS<7:6>), maintain these bits clear to ensure upward compatibility with future products.
- Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

	R/W-0	R/W-0	<u>R-1</u>	<u>R-1</u>	R/W-x	R/W-x	R/W-x	
bit7	RP1	RP0	ТО	PD	Z	DC	C bit0	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset
bit 7:	IRP: Regi 1 = Bank 0 = Bank	ster Bank 2, 3 (100h 0, 1 (00h -	Select bit - 1FFh) FFh)	(used for	indirect ad	dressing)		
bit 6-5:	RP1:RP0 11 = Banl 10 = Banl 01 = Banl 00 = Banl Each ban	: Register < 3 (180h - < 2 (100h - < 1 (80h - I < 0 (00h - 7 k is 128 by	Bank Sel 1FFh) 17Fh) FFh) 7Fh) ⁄tes	ect bits (u	sed for dire	ct address	ing)	
bit 4:	TO: Time- 1 = After 0 = A WD	-out bit power-up, T time-out	CLRWDT ir	nstruction,	or sleep ii	nstruction		
bit 3:	PD : Powe 1 = After 0 = By ex	er-down bit power-up o ecution of	or by the othe street	CLRWDT ins	struction			
bit 2:	Z: Zero bi 1 = The re 0 = The re	t esult of an esult of an	arithmetio arithmetio	c or logic o c or logic o	operation is	zero not zero		
bit 1:	DC: Digit 1 = A carr 0 = No ca	carry/borro ry-out from rry-out fro	ow bit (AD the 4th le m the 4th	DWF, ADDL Dw order b low order	w,SUBLW,S bit of the res bit of the re	UBWF instru Sult occurre Soult	uctions)(for ed	borrow the polarity is reversed)
bit 0:	C: Carry/I 1 = A carr 0 = No ca Note: For the secon bit of the	porrow bit ry-out from arry-out from borrow the od operand source reg	(ADDWF, A the most m the mo e polarity l. For rota ister.	DDLW, SUB t significar st significa is reverse te (RRF, RL	LW, SUBWF at bit of the ant bit of the d. A subtra F) instruction	instruction result occu result occu ction is ex ons, this bi	s) urred curred ecuted by a t is loaded	adding the two's complement of with either the high or low order

FIGURE 4-7: STATUS REGISTER (ADDRESS 03h, 83h)

4.2.2.3 INTCON REGISTER

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The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

FIGURE 4-9: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	R. – Roodoblo hit				
bit7				KDIE			bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset				
bit 7:	GIE:⁽¹⁾ GI 1 = Enabl 0 = Disab	lobal Inter es all un-r les all inte	rupt Enabl nasked int rrupts	e bit errupts								
bit 6:	 ADIE: A/D Converter Interrupt Enable bit 1 = Enables A/D interrupt 0 = Disables A/D interrupt 											
bit 5:	TOIE: TM 1 = Enabl 0 = Disab	R0 Overflo les the TM les the TM	ow Interrup R0 interru 1R0 interru	ot Enable I pt upt	oit							
bit 4:	INTE: RB 1 = Enabl 0 = Disab	0/INT Exte les the RB les the RE	ernal Inter 0/INT exte 30/INT ext	rupt Enabl ernal interr ernal inter	le bit upt rupt							
bit 3:	RBIE: RB 1 = Enabl 0 = Disab	B Port Cha les the RB les the RB	nge Interr port char 3 port chai	upt Enable ige interru nge interru	e bit pt ıpt							
bit 2:	TOIF: TMI 1 = TMRC 0 = TMRC	R0 Overflo) register ł) register o	ow Interrup has overflo did not ove	ot Flag bit wed (mus erflow	t be cleare	d in softwa	re)					
bit 1:	INTF: RB 1 = The R 0 = The R	0/INT Exte 80/INT ex 80/INT ex	ernal Inter aternal inte aternal inte	rupt Flag b errupt occu errupt did r	oit urred (must not occur	be cleared	d in softwar	e)				
bit 0:	RBIF: RB 1 = At lea 0 = None	Port Cha ist one of t of the RB	nge Interro he RB7:R 7:RB4 pin	upt Flag bi B4 pins ch s have cha	it nanged sta anged state	te (must be	e cleared in	software)				
Note 1:	For the P tionally re for a deta	IC16C71, -enabled I iled descr	if an interr by the RET iption.	upt occurs	s while the ction in the	GIE bit is t user's Inter	being cleare rrupt Servic	ed, the GIE bit may be uninten- e Routine. Refer to Section 8.5				
Interru global enabli	upt flag bits I enable bit, ing an interr	get set whe GIE (INTC	en an interru ON<7>). Us	pt condition er software	n occurs reg should ens	ardless of th ure the appr	e state of its opriate interr	corresponding enable bit or the rupt flag bits are clear prior to				

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

Applicable Devices 710 71 711 715

The analog-to-digital (A/D) converter module has four analog inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 7-1 and Figure 7-2, controls the operation of the A/D module. The ADCON1 register, shown in Figure 7-3 configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
ADCS1	ADCS0	(1)	CHS1	CHS0	GO/DONE	ADIF	ADON	R = Readable bit			
bit7	1						bit0	W = Writable bit U = Unimplemented bit. read as '0'			
								- n =Value at POR reset			
bit 7-6:	ADCS1:A	DCS0: A/D	Conversi	on Clock S	Select bits						
	00 = FOS	C/2									
	10 = FOS	c/32									
	11 = FRC	(clock deriv	ed from a	n RC oscil	lation)						
bit 5:	Unimple	mented: Re	ad as '0'.								
bit 4-3:	CHS1:CHS0: Analog Channel Select bits 00 = channel 0, (RA0/AN0) 01 = channel 1, (RA1/AN1) 10 = channel 2, (RA2/AN2) 11 = channel 3, (RA3/AN3)										
bit 2:	GO/DON	E: A/D Con	version Sta	atus bit							
	$\frac{\text{If ADON}}{1 = A/D c}$ $0 = A/D c$ sion is co	<u>= 1</u> : onversion ir onversion n mplete)	n progress lot in prog	(setting th ress (This	his bit starts th bit is automat	ie A/D con ically cleai	version) ed by hardw	are when the A/D conver-			
bit 1:	ADIF: A/E 1 = conve 0 = conve	D Conversio ersion is con ersion is not	n Comple nplete (mu complete	te Interrup ist be clea	t Flag bit red in softwar	e)					
bit 0:	ADON: A	/D On bit									
	1 = A/D c 0 = A/D c	onverter mo onverter mo	odule is op odule is sh	erating utoff and o	consumes no	operating	current				
Note 1:	Bit5 of Al	DCON0 is a nented, read	l General I d as '0'.	Purpose R	R/W bit for the	PIC16C71	0/711 only. F	For the PIC16C71, this bit is			
	ampen	ionieu, iea									

FIGURE 7-1: ADCON0 REGISTER (ADDRESS 08h), PIC16C710/71/711

8.0 SPECIAL FEATURES OF THE CPU

Applicable Devices 710 71 711 715

What sets a microcontroller apart from other processors are special circuits to deal with the needs of realtime applications. The PIC16CXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR) (PIC16C710/711/715)
 - Parity Error Reset (PER) (PIC16C715)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16CXX has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 8-1: CONFIGURATION WORD FOR PIC16C71

bit13		—	—	—	_	_	—	CP0	PWRTE	WDTE	FOSC1	FOSC0 bit0	Register: Address	CONFIG 2007h
bit 13-5:	Unimplen	nented	: Read	as '1'										
bit 4:	CP0: Code 1 = Code 0 = All me	e prote protecti mory is	ction bi ion off 3 code p	t protecte	ed, but	00h - 3	Fh is w	vritable						
bit 3:	PWRTE: F 1 = Power 0 = Power	Power-u -up Tim -up Tim	up Time ner ena ner disa	er Enabl bled Ibled	e bit									
bit 2:	WDTE: Wa 1 = WDT e 0 = WDT e	atchdog enablec disablec	g Timer 1 d	Enable	e bit									
bit 1-0:	FOSC1:F0 11 = RC o 10 = HS o 01 = XT o 00 = LP o	OSC0: oscillato oscillato scillato scillato	Oscillat or or r r	tor Sele	ction b	its								

FIGURE 8-2: CONFIGURATION WORD, PIC16C710/711

CP0	CF	0 C	P0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	PWRTE	WDTE	FOSC1	FOSC0	Register:	CONFIG
oit13														bit0	Address	2007h
bit 13- 5- bit 6:	-7 4:	CP0: 1 = C 0 = Al BODE 1 = B 0 = B	Cod ode II me E N: I OR (OR (le prote protec emory i Brown- enable disable	ection b tion off is code out Re d	protec set En	ted, bu able bi	ut 00h - 3 _t (1)	Fh is w	vritable						
bit 3:		PWR 1 = P' 0 = P'	TE: WR1 WR1	Power- Γ disab Γ enab	up Tim led led	er Ena	ble bit	(1)								
bit 2:		WDTI 1 = W 0 = W	E: W /DT /DT	/atchdo enable disable	og Time d ed	er Enab	le bit									
bit 1-C):	FOSC 11 = 10 = 01 = 2 00 =	C1:F RC o HS o XT o LP o	OSCO oscillat oscillat oscillato	: Oscilla or or or or or	ator Se	lection	bits								
Note	1:	Enabl Ensur	ling l re th	Brown∙ e Powe	out Re er-up T	set aut imer is	omatic enable	ally enated anytim	oles Po ne Brov	wer-up vn-out f	Timer (F Reset is	WRT) enabled	regardle d.	ess of the	e value of bit \overline{F}	PWRTE.

2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.

FIGURE 8-3: CONFIGURATION WORD, PIC16C715

CP1	CP0	CP1	CP0	CP1	CP0	MPEEN	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	Register:	CONFIG
bit13													bit0	Address	2007h
bit 13- 5-	•8 CI 4: 11 10 01 00	P1:CP0 L = Coo D = Upp L = Upp D = All r): Cod de prot ber hal ber 3/4 memoi	e Prote ection f of pro th of p ry is co	ection off ogram rogran ode pro	bits ⁽²⁾ memory n memor ptected	code pro y code p	otected	l ed						
bit 7:	M 1 0	PEEN: = Mem = Mem	Memo ory Pa ory Pa	ory Par arity Ch arity Ch	ity Erre necking necking	or Enabl g is enab g is disat	e Ied Died								
bit 6:	B (1 0	oden: = Bor = Bor	Browr enabl disabl	n-out R ed led	Reset E	nable bi	it (1)								
bit 3:	P 1 0	WRTE: = PWR = PWR	Powe T disa T enal	r-up Ti bled bled	mer Ei	nable bit	(1)								
bit 2:	W 1 0	DTE: V = WDT = WDT	Vatchd enabl disabl	log Tin ed led	ner En	able bit									
bit 1-(D: F(11 10 01 00	DSC1:F L = RC D = HS L = XT D = LP	F OSCI oscilla oscilla oscilla oscilla	D: Osci ator ator tor tor tor	llator S	Selectior	i bits								
Note	1: Er Er 2: Al	nabling nsure th I of the	Browr he Pov CP1:0	n-out R ver-up CP0 pa	teset a Timer airs har	utomatio is enable ve to be	cally enal ed anytin given the	oles Po ne Brov e same	wer-up wn-out value	o Timer (f Reset is to enable	PWRT) enable the co	regardle d. de prote	ess of the	value of bit l eme listed.	PWRTE.

Register	Power-on Reset, Brown-out Reset Parity Error Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	นนนน นนนน	นนนน นนนน
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	นนนน นนนน	นนนน นนนน
PCL	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	นนนน นนนน	นนนน นนนน
PORTA	x 0000	u 0000	u uuuu
PORTB	xxxx xxxx	นนนน นนนน	นนนน นนนน
PCLATH	0 0000	0 0000	u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu (1)
PIR1	-0	-0	_u(1)
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION	1111 1111	1111 1111	นนนน นนนน
TRISA	1 1111	1 1111	u uuuu
TRISB	1111 1111	1111 1111	นนนน นนนน
PIE1	-0	-0	-u
PCON	qqq	luu	luu
ADCON1	00	00	uu

TABLE 8-13: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C715

Legend: u = unchanged, x = unknown, -= unimplemented bit, read as '0', q = value depends on condition Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-11 for reset value for specific condition.

FIGURE 8-17: INTERRUPT LOGIC, PIC16C710, 71, 711



FIGURE 8-18: INTERRUPT LOGIC, PIC16C715



TABLE 9-2: PIC16CXX INSTRUCTION SET

Mnemonic,		Description	Cycles		14-Bit	Opcode	Э	Status	Notes
Operands				MSb			LSb	Affected	
BYTE-ORIE	NTED	FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS						-	
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL A	ND CO	NTROL OPERATIONS							
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

PIC16C71X

CLRF	Clear f			
Syntax:	[<i>label</i>] C	LRF f		
Operands:	$0 \le f \le 12$	27		
Operation:	$00h \rightarrow (f)$ 1 $\rightarrow Z$)		
Status Affected:	Z			
Encoding:	00	0001	lfff	ffff
Description:	The conter and the Z	nts of regi bit is set.	ster 'f' are	cleared
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	Read register 'f'	Process data	Write register 'f'
Example	CLRF	FLAG	G_REG	
	Before In	struction	l	
	After least	FLAG_RE	EG =	0x5A
	AITELINST	FLAG RF	EG =	0x00
		Ζ	=	1

CLRW	Clear W			
Syntax:	[label]	CLRW		
Operands:	None			
Operation:	$00h \rightarrow (V)$	V)		
Status Affected	$1 \rightarrow Z$			
Encoding:		0001	0xxx	xxxx
Description:	W register	is cleare	d Zero bit	(7) is
Description.	set.	le cleare		(上) 10
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	NOP	Process data	Write to W
Example	CLRW			
Example	Before In	struction		
	Boloro III	W =	0x5A	
	After Inst	ruction	0.00	
		vv = Z =	0x00 1	
CLRWDT	Clear Wa	tchdog	Timer	
0 1			_	
Syntax:	[label]	CLRWD	I	
Syntax: Operands:	[<i>label</i>] None	CLRWD	I	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None 00h \rightarrow W	CLRWD DT	I	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$	CLRWD DT F presca	l ler,	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$	CLRWD DT F presca	l ler,	
Syntax: Operands: Operation: Status Affected:	$\begin{bmatrix} label \\ \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD	CLRWD DT Γpresca	l ler,	
Syntax: Operands: Operation: Status Affected: Encoding:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00	CLRWD DT F presca	l er, 0110	0100
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ $\boxed{00}$ CLRWDT in	CLRWD DT F presca	l ler, 0110 resets the	0100 Watch-
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ $\boxed{00}$ CLRWDT in dog Timer, of the WDT are set.	CLRWD DT F presca 0000 struction It also re T. Status I	0110 resets the provide TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I	0110 resets the poits TO and	0100 Watch- re <u>sca</u> ler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \end{bmatrix}$	CLRWD DT F presca output struction It also re T. Status I	I 0110 resets the set <u>s</u> the pi bits TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set. 1\\ 1\\ 2\\ 1\\ Q1\\ \end{bmatrix}$	CLRWD DT presca 0000 Istruction It also re T. Status I	I 0110 resets the set <u>s the</u> pi bits TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline O0 \\ CLRWDT in \\ dog Timer, of the WD \\ are set. \\ 1 \\ 1 \\ Q1 \\ \hline Decode \\ \end{bmatrix}$	CLRWD DT presca on on struction It also re T. Status I Q2 NOP	I 0110 resets the province of the province of the process Q3 Process	0100 Watch- rescaler d PD Q4 Clear
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WD are set. 11\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca oooo struction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ CLRWDT indog Timer,of the WDare set. 1\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	0110 resets the sets the provide TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set.11Q1\\ \hline Decode\\ \hline CLRWDT\\ \end{bmatrix}$	CLRWD DT presca oooo struction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline OO\\ CLRWDT indog Timer,of the WDare set.11Q1DecodeCLRWDTBefore In$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	I OIIO resets the sets the ploits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} abel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou	I ler, 0110 resets the provide the providet the provide the providet the p	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in dog Timer. of the WD are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou ruction WDT cou	I OIIO resets the sets the province of the process data Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline O0\\ CLRWDT indog Timer,of the WDare set.11Q1CLRWDTBefore InAfter Inst$	CLRWD DT presca r presca struction It also re T. Status I Q2 NOP struction WDT cou WDT cou WDT cou WDT cou	I ler, 0110 resets the provide the providet the	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00 0

PIC16C71X

Inclusive	e OR W v	with f	
[label]	IORWF	f,d	
$\begin{array}{l} 0 \leq f \leq 12 \\ d \in \ [0,1] \end{array}$	27		
(W) .OR.	$(f) \rightarrow (de)$	est)	
Z			
00	0100	dfff	ffff
Inclusive C ter 'f'. If 'd' the W regi placed bac	OR the W is 0 the re ster. If 'd' ck in regis	register wi esult is pla is 1 the res ster 'f'.	th regis- ced in sult is
1			
1			
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to dest
IORWF		RESULT,	0
Before In	struction	1	
	RESULT	= 0x13	3
After Inst	ruction	- 0791	
	RESULT	= 0x13	3
	W Z	= 0x93 = 1	3
	Inclusive [label] $0 \le f \le 12$ $d \in [0,1]$ (W) .OR. \overline{Z} Inclusive C ter 'f'. If 'd' the W reginst placed base 1 1 Q1 Decode IORWF Before In After Inst	Inclusive OR Wy $[label]$ IORWF $0 \le f \le 127$ $d \in [0,1]$ (W) .OR. $(f) \rightarrow (de)$ \overline{Z} 00 0100Inclusive OR the Wter 'f'. If 'd' is 0 the rethe W register. If 'd'placed back in regist1Q1Q2DecodeReadregister'f'IORWFBefore InstructionRESULTWAfter InstructionRESULTW7	Inclusive OR W with f[label]IORWFf,d $0 \le f \le 127$ $d \in [0,1]$ (W) .OR. $(f) \rightarrow (dest)$ \overline{Z} 00 0100 dfffInclusive OR the W register without the W register. If 'd' is 0 the result is plat the W register. If 'd' is 1 the result placed back in register 'f'.11Q1Q2Q3DecodeRead register 'f'IORWFRESULT ,Before Instruction RESULT =0x13 WQ1Q2Q3DecodeRead register 'f'IORWFRESULT ,Before Instruction RESULT =0x13 WW=Q1Q3Q1Q2Q2Q3DecodeRead register 'f'IORWFRESULT ,Before Instruction RESULT =0x13 WQ1Q2Q3Q3Q4Q3Q4Q4Q5Q4Q7=Q6Q4Q7=Q6Q4Q7=Q7=

MOVLW	Move Literal to W										
Syntax:	[label]	MOVLW	/ k								
Operands:	$0 \le k \le 28$	$0 \le k \le 255$									
Operation:	$k \to (W)$										
Status Affected:	None										
Encoding:	11	00xx	kkkk	kkkk							
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.										
Words:	1										
Cycles:	1										
Q Cycle Activity:	Q1	Q2	Q3	Q4							
	Decode	Read literal 'k'	Process data	Write to W							
Example	MOVLW After Inst	0x5A									
		W =	0x5A								

MOVF	Move f									
Syntax:	[label] MOVF f,d									
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$									
Operation:	(f) \rightarrow (dest)									
Status Affected:	Z									
Encoding:	00 1000 dfff ffff									
Description:	The contents of register f is moved to a destination dependant upon the sta- tus of d. If $d = 0$, destination is W reg- ister. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected									
Words:	1									
Cycles:	1									
Q Cycle Activity:	Q1 Q2 Q3 Q4									
	Decode Read register 'f' Vrite to data dest									
Example	MOVF FSR, 0									
	After Instruction W = value in FSR register Z = 1									

MOVWF	Move W	to f								
Syntax:	[label]	MOVW	F f							
Operands:	$0 \le f \le 127$									
Operation:	$(W) \rightarrow (f)$									
Status Affected:	None									
Encoding:	00 0000 1fff ffff									
Description:	Move data from W register to register									
Words:	1									
Cycles:	1									
Q Cycle Activity:	Q1	Q2	Q3	Q4						
	Decode	Read register 'f'	Process data	Write register 'f'						
Example	MOVWF	OPTIC	ON_REG							
	Before In	struction	1							
			= 0xFI	=						
	After Inst	ruction	- 0,41							
		OPTION	= 0x4	=						
		W	= 0x4F	=						

Applicable Devices 710 71 711 715

		Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ (commercial)							
DC CHAI	DC CHARACTERISTICS				-40°C	; ≤I	$A \leq +85^{\circ}C$ (industrial)		
		Operati	ing voltage) 04- 2 range a	∠ ≤ I s descr	$A \leq +125$ C (extended)		
		Section	11.2.	, 101	o lange a	3 06301	ibed in DO spec Dection 11.1 and		
Param No.	Characteristic	Sym	Min	Тур †	Max	Units	Conditions		
	Output Low Voltage								
D080	I/O ports	Vol	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C		
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C		
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C		
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C		
	Output High Voltage								
D090	I/O ports (Note 3)	Vон	Vdd - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°С to +85°С		
D090A			Vdd - 0.7	-	-	V	Юн = -2.5 mA, VDD = 4.5V, -40°C to +125°C		
D092	OSC2/CLKOUT (RC osc config)		Vdd - 0.7	-	-	V	ІОН = -1.3 mA, VDD = 4.5V, -40°С to +85°С		
D092A			Vdd - 0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C		
D130*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin		
	Capacitive Loading Specs on Output Pins								
D100	OSC2 pin	Cosc2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Сю	-	-	50	pF			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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11.4 <u>Timing Parameter Symbology</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS

Т				
F	Frequency	Т	Time	
Lower	case letters (pp) and their meanings:			
рр				
сс	CCP1	osc	OSC1	
ck	CLKOUT	rd	RD	
cs	CS	rw	RD or WR	
di	SDI	sc	SCK	
do	SDO	SS	SS	
dt	Data in	tO	TOCKI	
io	I/O port	t1	T1CKI	
mc	MCLR	wr	WR	
Upperc	case letters and their meanings:			
S				
F	Fall	P	Period	
Н	High	R	Rise	
	Invalid (Hi-impedance)	V	Valid	
L	Low	Z	Hi-impedance	

FIGURE 11-1: LOAD CONDITIONS



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$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	13.3	DC Characteristics: PIC16C7 PIC16C7 PIC16C7 PIC16C7 PIC16LC	15-04 15-10 15-20 715-04	(Comme (Comme (Comme (Comme	ercia ercia ercia ercia	al, Indus al, Indus al, Indus al, Indus	strial, strial, strial, strial))	Extended) Extended) Extended))				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			Standa	rd Opera	ting	Conditi	ons (u	nless otherwise stated)				
40 C40 C40 C40 C40 C40 C40 C40 C40 C41 C40 C41 C40 C41 C40 C41 C41 C40 C40 C <th cols<="" td=""><td></td><td colspan="10">Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial)</td></th>	<td></td> <td colspan="10">Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial)</td>		Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial)									
Operating voltage VbD range as described in DC spec Section 13.ParamCharacteristicSymMinTypMaxUnitsNo.Input Low VoltageI/O portsVILVis-0.5VVD030with TTL bufferVisVis-0.5VVD031with Schmitt Trigger bufferVss-0.2VbbVD032MCLR, RA4/TOCKI,OSC1Vss-0.3VbbVD033OSC1 (in XT, HS and LP)Vss-0.3VbbVD0404with Schmitt Trigger buffer0.8Vbb-VbbVD0424MCLR, RA4/TOCKI RB0/INT0.8Vbb-VbbVD0424MCLR, RA4/TOCKI RB0/INT0.8VbbVbbVobVD0424MCLR, RA4/TOCKI RB0/INT0.8VbbVbbVbbVD043OSC1 (in RC mode)0.8VbbVbbVbbVD040Input Leakage Current (Notes 2, 3)Int-±1 μA Vss \leq VPIN \leq Vbb, PIn $=$ VssD060I/O portsVobVob0.6VVbb \leq Vbb, Vbb, PIn $=$ VssD061MCLR, RA4/TOCKI±5 μA Vss \leq VPIN \leq Vbb, XT, HS and osc configurationD080I/O portsVob0.6VIoL = 8.5 mA, Vbb = 4.5V, -40°C to +85°CD080AI/O portsVob0.6V<	DC CHA	RACTERISTICS				-40 -40°		$TA \leq +85 C$ (industrial) $TA \leq +125^{\circ}C$ (extended)				
Description of the large biolectrice in the space of each line in t			Onerating voltage Von range as described in DC spec Section 13.1									
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	and Section 13.2.											
No. t Input Low Voltage VIL D030 with TTL buffer D031 with Schmitt Trigger buffer D032 MCLR, RA4/T0CKI,OSC1 (in RC mode) VIL D033 OSC1 (in XT, HS and LP) VIH - Input High Voltage I/O ports VIH D040 with Schmitt Trigger buffer D041 with TTL buffer D042 MCLR, RA4/T0CKI RB0/INT D043 OSC1 (in RC mode) D044 with Schmitt Trigger buffer D042 MCLR, RA4/T0CKI RB0/INT D043 OSC1 (in RC mode) D070 PORTB weak pull-up current Input Leakage Current (Notes 2, 3) D060 I/O ports D061 MCLR, RA4/T0CKI D063 OSC1 D064 MCLR, RA4/T0CKI D070 PORTB weak pull-up current Input Leakage Current (Notes 2, 3) UL - D061 MCLR, RA4/T0CKI D063 OSC1	Param	Characteristic	Svm	Min	σνΤ	Max	Units	Conditions				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	No.				†							
V/O portsVILVILVSS-0.5VVD030with TTL bufferVSS-0.2VDDVD032MCLR, RA4/T0CKI,OSC1VSS-0.2VDDVD033OSC1 (in XT, HS and LP)VSS-0.3VDDVD040with TTL bufferVIHVDDVD040Awith Schmitt Trigger buffer0.8VDD-VDDVD041with Schmitt Trigger buffer0.8VDD-VDDVD042MCLR, RA4/T0CKI RB0/INT0.8VDD-VDDVD043OSC1 (XT, HS and LP)0.8VDD-VDDVD043OSC1 (In RC mode)0.8VDD-VDDVD040OSC1 (In RC mode)0.8VDD-VDDVD040OSC1 (In RC mode)0.8VDD-VDDVD043OSC1 (IN RC mode)0.8VDD-VDDVD060I/O portsIIL- ± 1 μA VSS \leq VIN \leq VDD, Pin at hi-D061MCLR, RA4/T0CKI ± 5 μA VSS \leq VIN \leq VDD, XT, HS and osc configurationD080I/O portsVOL0.6VIOL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080AOSC2/CLK/2UT (RC osc config)0.6VIOL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083AOSC2/CLK/2UT (RC osc config)0.6VIOL = 1.2 mA, VDD = 4.5V, -40°C to +155°C		Input Low Voltage										
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		I/O ports	VIL									
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D030	with TTL buffer		Vss	-	0.5V	V					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D031	with Schmitt Trigger buffer		Vss	-	0.2Vdd	V	$ \langle \vee \rangle \rangle$				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D032	MCLR, RA4/T0CKI,OSC1		Vss	-	0.2Vdd	V					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		(in RC mode)						$\langle \rangle$				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D033	OSC1 (in XT, HS and LP)		Vss	-	0.3Vdd	7 V/	Note1				
I/O portsVIH-VIH-D040with TTL buffer0.8 VDDV $4.5 \le VDD \le 5.5V$ or VDD < 4.5V		Input High Voltage				\land	$\left[\right]$					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		I/O ports	Vih		-	$ \langle \rangle$	$ \rangle$					
D040A D041with Schmitt Trigger buffer D042 $0.8 V DD$ $V DD$ $V DD$ V D042MCLR, RA4/T0CKI RB0/INT D042A $0.8 V DD$ $0.8 V DD$ V $V DD$ V D043OSC1 (XT, HS and LP) D043 $0.7 V DD$ $V DD$ V $V DD$ V D043OSC1 (in RC mode) $0.8 V DD$ $V DD$ V $V DD$ V D070PORTB weak pull-up current I^{PURB} 50 250 400 μA $V DD = 5V, VPIN = VSS$ D060I/O portsInput Leakage Current (Notes 2, 3) D063Int IIL $ \pm 1$ μA $V SS \leq VPIN \leq V DD$, Pin at hi- impedanceD061MCLR, RA4/T0CKI D063 $ \pm 5$ μA $V SS \leq VPIN \leq V DD$, XT, HS and osc configurationD080I/O ports $V OL$ $ 0.6$ V $I OL = 8.5 mA, V DD = 4.5 V,$ $-40°C to + 85°CD083OSC2/CLKØUT (RC osc config) 0.6VI OL = 7.0 mA, V DD = 4.5 V,-40°C to + 85°CD083A 0.6VI OL = 1.2 mA, V DD = 4.5 V,-40°C to + 85°C$	D040	with TTL buffer		2.0	~	VDD	<u>v</u>	$4.5 \leq VDD \leq 5.5V$				
D041with Schmitt Trigger buffer D042 $0.8 Vob$ $-Vbb$ V For entire VDD rangeD042MCLR, RA4/T0CKI RB0/INT D043 $0.8 Vob$ Vob V Note1D043OSC1 (in RC mode) $0.7 Vob$ V V Note1D070PORTB weak pull-up current $PURB$ 50 250 400 μA $VDD = 5V$, $VPIN = VSS$ Input Leakage Current (Notes 2, 3)IIIL $ \pm 1$ μA $Vss \leq VPIN \leq VDD$, Pin at hi- impedanceD060I/O portsIIIL $ \pm 5$ μA $Vss \leq VPIN \leq VDD$, Pin at hi- impedanceD061MCLR, RA4/T0CKI $ \pm 5$ μA $Vss \leq VPIN \leq VDD$, XT, HS and osc configurationD080I/O ports VoL $ 0.6$ V $IoL = 8.5 mA, VDD = 4.5V,$ $-40°C to +85°CD083OSC2/CLKOUT (RC osc config) 0.6VIoL = 1.6 mA, VDD = 4.5V,-40°C to +85°CD083A 0.6VIoL = 1.2 mA, VDD = 4.5V,-40°C to +85°C$	D040A			0.8Vdd	<u> </u>	VDD	N 4	For VDD > 5.5V or VDD < 4.5V				
D042MCLR, RA4/T0CKI RB0/INT D042A0.8VbbVop VVD043OSC1 (XT, HS and LP) OSC1 (in RC mode)0.7VpD VVDDVD070PORTB weak pull-up currentIPURB50250400 μ AVDD = 5V, VPIN = VSSInput Leakage Current (Notes 2, 3) D060I/O portsIIIL- ± 1 μ AVSs \leq VPIN \leq VDD, Pin at hi- impedanceD061MCLR, RA4/T0CKI OSC1 ± 5 μ AVSs \leq VPIN \leq VDD, XT, HS and osc configurationD083OSC2/CLKØUT (RC osc config)Vol0.6VIoL = 8.5 mA, VDD = 4.5V, -40°C to +125°CD083AOSC2/CLKØUT (RC osc config)0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +125°C	D041	with Schmitt Trigger buffer		0.8100	- \	VBp	$\neg \checkmark$	For entire VDD range				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	D042	MCLR, RA4/T0CKI RB0/INT		0.8VDD		VqD>	V					
D043OSC1 (in RC mode) 0.9 VD070PORTB weak pull-up currentIPURB 50 250 400 μA VDD = 5V, VPIN = VSSInput Leakage Current (Notes 2, 3)IIIL ± 1 μA Vss \leq VPIN \leq VDD, Pin at hi-D060I/O portsIIIL ± 1 μA Vss \leq VPIN \leq VDD, Pin at hi-D061MCLR, RA4/T0CKI ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVoL0.6VIoL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080AOSC2/CLKØUT (RC osc config)0.6VIoL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083AOSC2/CLKØUT (RC osc config)0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +85°CD083A0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +85°C	D042A	OSC1 (XT, HS and LP)			<u> </u>	VDY	V	Note1				
D070PORTB weak pull-up currentPORE50250400 μA VDD = 5V, VPIN = VSSInput Leakage Current (Notes 2, 3)IIIL ± 1 μA Vss \leq VPIN \leq VDD, Pin at himpedanceD060I/O portsIIIL ± 5 μA Vss \leq VPIN \leq VDD, Pin at himpedanceD061MCLR, RA4/T0CKI ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVoL0.6VIoL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080AOSC2/CLKØUT (R& osc config)0.6VIoL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083A0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +85°C	D043	OSC1 (in RC mode)		0.9XDD	- \	<i>∕</i> ∛dd	V					
Input Leakage Current (Notes 2, 3)IIL- ± 1 μA Vss \leq VPIN \leq VDD, Pin at hi- impedanceD061MCLR, RA4/T0CKI ± 5 μA Vss \leq VPIN \leq VDDD063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVol0.6VIOL = 8.5 mA, VDD = 4.5V, -40° C to $+85^{\circ}$ CD080AOSC2/CLKØUT (RC osc config)0.6VIOL = 7.0 mA, VDD = 4.5V, -40° C to $+125^{\circ}$ CD083AOSC2/CLKØUT (RC osc config)0.6VIOL = 1.6 mA, VDD = 4.5V, -40° C to $+85^{\circ}$ CD083A0.6VIOL = 1.2 mA, VDD = 4.5V, -40° C to $+125^{\circ}$ C	D070	PORTB weak pull-up current	PURB	50	250	400	μΑ	VDD = 5V, VPIN = VSS				
D060I/O portsIIL ± 1 μA Vss \leq VPIN \leq VDD, Pin at hi- impedanceD061MCLR, RA4/T0CKI ± 5 μA Vss \leq VPIN \leq VDDD063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVOL0.6VIOL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080AI/O portsVOL0.6VIOL = 7.0 mA, VDD = 4.5V, -40°C to +125°CD083AOSC2/CLKOUT (RC osc config)0.6VIOL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083A0.6VIOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C		Input Leakage Current (Notes 2, 3		\bigvee	\sim							
D061MCLR, RA4/T0CKI ± 5 μA Vss \leq VPIN \leq VDDD063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVol0.6VIoL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080A0.6VIoL = 7.0 mA, VDD = 4.5V, -40°C to +125°CD083OSC2/CLKOUT (RC osc config)0.6VIoL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083A0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +85°C-	D060	I/O ports			-	±1	μA	$Vss \leq VPIN \leq VDD$, Pin at hi-impedance				
D063OSC1 ± 5 μA Vss \leq VPIN \leq VDD, XT, HS and osc configurationD080I/O portsVol0.6VIoL = 8.5 mA, VDD = 4.5V, -40°C to +85°CD080A0.6VIoL = 7.0 mA, VDD = 4.5V, -40°C to +125°CD083OSC2/CLKOUT (RC osc config)0.6VIoL = 1.6 mA, VDD = 4.5V, -40°C to +85°CD083A0.6VIoL = 1.2 mA, VDD = 4.5V, -40°C to +85°C	D061	MCLR, RA4/T0CKI		-	-	±5	μA	$Vss \le VPIN \le VDD$				
Output Low Voltage Vol - 0.6 V IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C D080A - - 0.6 V IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C D083A - - 0.6 V IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C	D063	OSC1	\land	-	-	±5	μA	$Vss \leq VPIN \leq VDD, XT, HS and LP$				
Output Low Voltage Vol - - 0.6 V IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C D080A - - 0.6 V IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C D083A OSC2/CLKOUT (RC osc config) - - 0.6 V IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C D083A OSC2/CLKOUT (RC osc config) - - 0.6 V IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C		$ \land \land \land \land$	X					osc configuration				
D080 I/O ports Vol - - 0.6 V IoL = 8.5 mA, VDD = 4.5V, -40°C to +85°C D080A - - 0.6 V IoL = 7.0 mA, VDD = 4.5V, -40°C to +125°C D083A OSC2/CLKOUT (RC osc config) - - 0.6 V IoL = 7.0 mA, VDD = 4.5V, -40°C to +125°C D083A - - 0.6 V IoL = 1.6 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IoL = 1.2 mA, VDD = 4.5V, -40°C to +125°C		Output Low Voltage	X									
D080A - - 0.6 V IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C D083 OSC2/CLKOUT (RC osc config) - - 0.6 V IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C	D080	I/O ports	Vol	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C				
D083 OSC2/CLKOUT (RC osc config) - - 0.6 V IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C D083A - - 0.6 V IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C	D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C				
D083A 0.6 V $IOL = 1.2 \text{ mA}, \text{ VDD} = 4.5 \text{ V}, -40^{\circ}\text{C to } +125^{\circ}\text{C}$	D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C				
	D083A	(b) > (b)		-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C				

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

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FIGURE 14-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)



FIGURE 14-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



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15.2 DC Characteristics: PIC16LC71-04 (Commercial, Industrial)

DC CHA	RACTERISTICS		Standard Operating Conditions (unless otherwise stated)OOperating temperature $0^{\circ}C$ $\leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C$ $\leq TA \leq +85^{\circ}C$ (industrial)							
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions			
D001	Supply Voltage	Vdd	3.0	-	6.0	V	XT, RC, and LP osc configuration			
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V				
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details			
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details			
D010	Supply Current (Note 2)	IDD	-	1.4	2.5	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4)			
D010A			-	15	32	μA	LP osc configuration Fosc = 32 kHz, VDD = 3.0V, WDT disabled			
D020	Power-down Current	IPD	-	5	20	μA	VDD = 3.0V, WDT enabled, -40°C to +85°C			
D021	(Note 3)		-	0.6	9	μA	VDD = $3.0V$, WDT disabled, $0^{\circ}C$ to $+70^{\circ}C$			
D021A			-	0.6	12	μA	VDD = $3.0V$, WDT disabled, $-40^{\circ}C$ to $+85^{\circ}C$			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

 $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

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15.3	DC Characteristics: PIC16C71 PIC16C71 PIC16LC7 PIC16LC7	-04 (0 -20 (0 1-04 (0	Commerc Commerc Commerc	cial, cial, cial,	Indust Indust Indust	rial) rial) rial)				
		Standa	rd Opera	ting	Conditi	ons (u	nless otherwise stated)			
OOperating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial)										
DC CHA										
operating voltage VDD range as described in DC spec Section 15.1										
and Scoloff 15.2.										
No.	Gharacteristic	Sym		1 1	WIAN	Units	Conditions			
	Input Low Voltage									
	I/O ports	VIL								
D030	with TTL buffer		Vss	-	0.15V	V	For entire VDD range			
D031	with Schmitt Trigger buffer		Vss	-	0.8V	V	$4.5 \leq VDD \leq 5.5V$			
D032	MCLR, OSC1 (in RC mode)		Vss	-	0.2Vdd	V				
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3Vdd	V	Note1			
	Input High Voltage									
	I/O ports (Note 4)	Vін		-						
D040	with TTL buffer		2.0	-	Vdd	V	$4.5 \le VDD \le 5.5V$			
D040A			0.25VDD + 0.8V	-	Vdd		For entire VDD range			
D041	with Schmitt Trigger buffer		0.85Vdd	-	Vdd		For entire VDD range			
D042	MCLR, RB0/INT		0.85Vdd	-	Vdd	V				
D042A	OSC1 (XT, HS and LP)		0.7Vdd	-	Vdd	V	Note1			
D043	OSC1 (in RC mode)		0.9Vdd	-	Vdd	V				
D070	PORTB weak pull-up current	IPURB	50	250	†400	μΑ	VDD = 5V, VPIN = VSS			
	Input Leakage Current (Notes 2, 3)									
D060	I/O ports	lı∟	-	-	±1	μA	Vss \leq VPIN \leq VDD, Pin at hi- impedance			
D061	MCLR, RA4/T0CKI		-	-	±5	μΑ	$Vss \le VPIN \le VDD$			
D063	OSC1		-	-	±5	μA	Vss \leq VPIN \leq VDD, XT, HS and LP osc configuration			
	Output Low Voltage									
D080	I/O ports	Vol	-	-	0.6	V	IOL = 8.5mA, VDD = 4.5V, -40°C to +85°C			
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6mA, VDD = 4.5V, -40°C to +85°C			
	Output High Voltage									
D090	I/O ports (Note 3)	Vон	VDD - 0.7	-	-	V	IOH = -3.0mA, VDD = 4.5V, -40°С to +85°С			
D092	OSC2/CLKOUT (RC osc config)		Vdd - 0.7	-	-	V	IOH = -1.3mA, VDD = 4.5V, -40°С to +85°С			
D130*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin			
·			· · · ·							

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 2: Negative current is defined as current sourced by the pin.

3: Negative current is defined as current sourced by the pin.

4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

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FIGURE 16-22: IOL VS. VOL, VDD = 5V



NOTES:

NOTES: