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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c715t-20i-ss

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#### To Our Valued Customers

We constantly strive to improve the quality of all our products and documentation. We have spent an exceptional amount of time to ensure that these documents are correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please use the reader response form in the back of this data sheet to inform us. We appreciate your assistance in making this a better document.

#### 3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

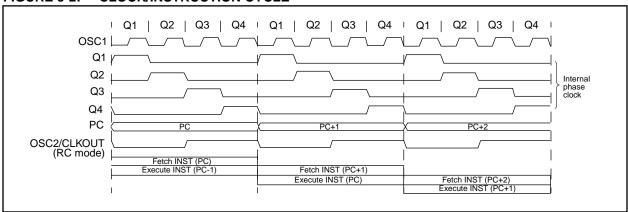
#### 3.2 <u>Instruction Flow/Pipelining</u>

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

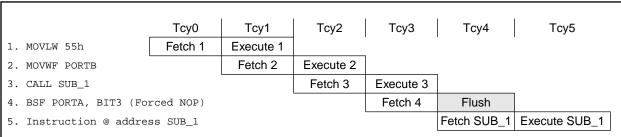
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).





#### **EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

#### 4.2.2.4 PIE1 REGISTER

Applicable Devices710 71 711 715

**Note:** Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

This register contains the individual enable bits for the Peripheral interrupts.

#### FIGURE 4-10: PIE1 REGISTER (ADDRESS 8Ch)

	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	ADIE	_	_	_	_	_	_
b	it7							bit0

R = Readable bit W = Writable bit

U = Unimplemented bit,

read as '0' n = Value at POR reset

bit 7: Unimplemented: Read as '0'

bit 6: ADIE: A/D Converter Interrupt Enable bit

1 = Enables the A/D interrupt 0 = Disables the A/D interrupt bit 5-0: **Unimplemented:** Read as '0'

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#### 7.9 <u>Transfer Function</u>

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is Analog VREF/256 (Figure 7-6).

#### 7.10 References

A very good reference for understanding A/D converters is the "Analog-Digital Conversion Handbook" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).

FIGURE 7-6: A/D TRANSFER FUNCTION

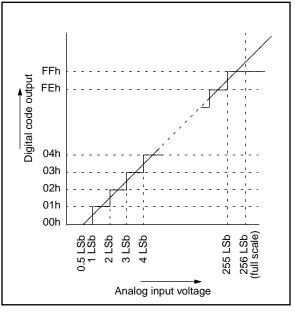


FIGURE 7-7: FLOWCHART OF A/D OPERATION

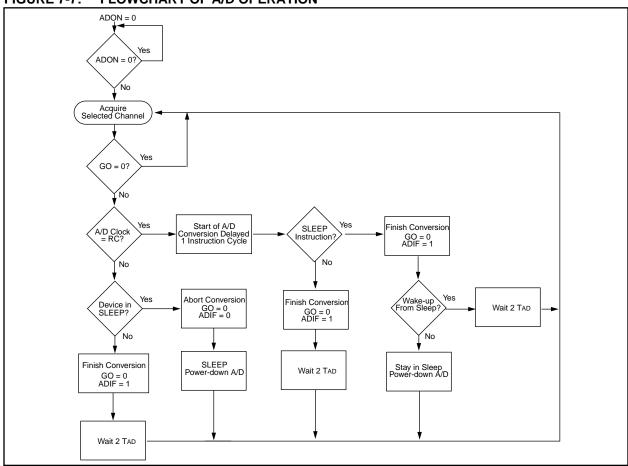
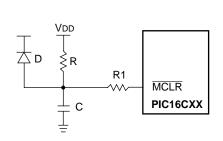
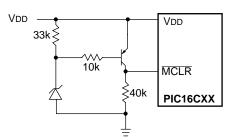


FIGURE 8-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



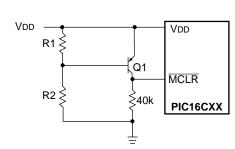
- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
  - 2:  $R < 40 \text{ k}\Omega$  is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
  - 3:  $R1 = 100\Omega$  to 1 k $\Omega$  will limit any current flowing into  $\overline{MCLR}$  from external capacitor C in the event of  $\overline{MCLR}$ /VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

### FIGURE 8-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
  - Resistors should be adjusted for the characteristics of the transistor.

### FIGURE 8-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

**NOTES:** 

CLRF	Clear f							
Syntax:	[label] C	LRF f						
Operands:	$0 \le f \le 12$	27						
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$	)						
Status Affected:	Z							
Encoding:	00	0001	1fff	ffff				
Description:	The conte and the Z	•	ster 'f' are	cleared				
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write register 'f'				
Example	CLRF	FLAC	E_REG					
	Before In	struction FLAG_RE		0x5A				
	After Instruction							

FLAG\_REG = 0x00

CLRW	Clear W			
Syntax:	[ label ]	CLRW		
Operands:	None			
Operation:	$\begin{array}{c} 00h \rightarrow (V \\ 1 \rightarrow Z \end{array}$	V)		
Status Affected:	Z			
Encoding:	00	0001	0xxx	xxxx
Description:	W register set.	is cleare	d. Zero bit	(Z) is
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	NOP	Process data	Write to W
Example	CLRW			
	Before In		-	
	After Inst	W = ruction	0x5A	
		W = Z =	0x00 1	

CLRWDT	Clear Wa	tchdog	Timer				
Syntax:	[ label ]	CLRWD	Т				
Operands:	None						
Operation:	$00h \rightarrow W$ $0 \rightarrow WD$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$		ler,				
Status Affected:	$\overline{TO}$ , $\overline{PD}$						
Encoding:	00	0000	0110	0100			
Description:	CLRWDT in dog Timer of the WD are set.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	NOP	Process data	Clear WDT Counter			
Example	CLRWDT						
	Before In	WDT cou		?			
		WDT cou		0x00			
		WDT pres	scaler= =	0			
		PD	=	1			

XORLW	Exclusive OR Literal with W	XORWF	Exclusive OR W with f
Syntax:	[ <i>label</i> ] XORLW k	Syntax:	[ <i>label</i> ] XORWF f,d
Operands:	0 ≤ k ≤ 255	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(W)$ .XOR. $k \rightarrow (W)$	Operation:	(W) .XOR. (f) $\rightarrow$ (dest)
Status Affected:	Z	Status Affected:	Z
Encoding:	11   1010   kkkk   kkkk	Encoding:	00 0110 dfff ffff
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored heal; in register.
Words:	1		is 1 the result is stored back in register 'f'.
Cycles:	1	Words:	1
Q Cycle Activity:	Q1 Q2 Q3 Q4	Cycles:	1
	Decode Read Process Write to literal 'k' data W	Q Cycle Activity:	Q1 Q2 Q3 Q4
Example:	XORLW 0xAF		Decode Read register data Write to dest
	Before Instruction		
	W = 0xB5	Example	XORWF REG 1
	After Instruction		Before Instruction
	W = 0x1A		$ \begin{array}{rcl} REG & = & 0xAF \\ W & = & 0xB5 \end{array} $
			After Instruction
			REG = 0x1A W = 0xB5

#### 10.0 DEVELOPMENT SUPPORT

#### 10.1 <u>Development Tools</u>

The PICmicro<sup>™</sup> microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART<sup>®</sup> Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy Logic Development System (fuzzyTECH<sup>®</sup>–MP)

# 10.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

#### 10.3 <u>ICEPIC: Low-Cost PIC16CXXX</u> In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT<sup>®</sup> through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

#### 10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In standalone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

#### 10.5 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C75X	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
roducts	PICMASTER®/ PICMASTER-CE In-Circuit Emulator	>	7	7	,	7	7	7	7	7	Available 3Q97		
Fmulator F	ICEPIC Low-Cost In-Circuit Emulator	7		7	7	7	7	7					
'	MPLAB™ Integrated Development Environment	7	7	7	7	7	7	7	7	7	7		
slo	MPLAB™ C Compiler	7	>	>	7	7	7	>	>	>	>		
oT ərswitoč	fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	>	7	7	7	7	7	>	7	>			
3	MP-DriveWay™ Applications Code Generator			7	7	7	7	7		7			
	Total Endurance™ Software Model											7	
	PICSTART® Lite Ultra Low-Cost Dev. Kit			^		7	>	<b>&gt;</b>					
สเมเลยเร	PICSTART <sup>®</sup> Plus Low-Cost Universal Dev. Kit	7	7	>	>	7	>	>	>	7	>		
Progr	PRO MATE <sup>®</sup> II Universal Programmer	>	7	>	7	7	7	7	7	<b>,</b>	>	7	7
	KEELOQ <sup>®</sup> Programmer												7
	SEEVAL <sup>®</sup> Designers Kit											>	
ards	PICDEM-1			7	7			7		7			
0 B 0	PICDEM-2					>	>						
məq	PICDEM-3								7				
	KEELOQ® Evaluation Kit												7

VDD = 3.0V, WDT disabled, -40°C to +125°C

BOR enabled VDD = 5.0V

### 11.2 DC Characteristics: PIC16LC710-04 (Commercial, Industrial, Extended) PIC16LC711-04 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated) Operating temperature  $\leq$  TA  $\leq$  +70°C (commercial) 0°C **DC CHARACTERISTICS** -40°C  $\leq$  TA  $\leq$  +85°C (industrial) -40°C  $\leq$  TA  $\leq$  +125°C (extended) Conditions **Param** Characteristic Sym Min Typ† Max Units No. D001 Supply Voltage Commercial/Industrial VDD 2.5 6.0 ٧ LP, XT, RC osc configuration (DC - 4 MHz) Extended VDD 3.0 6.0 ٧ LP, XT, RC osc configuration (DC - 4 MHz) D002\* RAM Data Retention VDR V 1.5 Voltage (Note 1) D003 VDD start voltage to **VPOR** V Vss See section on Power-on Reset for details ensure internal Poweron Reset signal D004\* VDD rise rate to ensure SVDD 0.05 V/ms See section on Power-on Reset for details internal Power-on Reset signal **Brown-out Reset** D005 **B**VDD 3.7 4.0 4.3 V BODEN configuration bit is enabled Voltage D010 Supply Current IDD 2.0 3.8 mΑ XT, RC osc configuration Fosc = 4 MHz, VDD = 3.0V (Note 4) (Note 2) D010A 22.5 48 LP osc configuration μΑ Fosc = 32 kHz, VDD = 3.0V, WDT disabled D015 **Brown-out Reset** 300\* 500 BOR enabled VDD = 5.0V  $\Delta \text{IBOR}$ μΑ Current (Note 5) D020 Power-down Current 7.5 30 VDD = 3.0V, WDT enabled, -40°C to +85°C **IPD** иΑ D021 0.9 5 VDD = 3.0V. WDT disabled, 0°C to +70°C (Note 3) иΑ D021A μΑ VDD = 3.0V, WDT disabled, -40°C to +85°C 0.9 5

\* These parameters are characterized but not tested.

Brown-out Reset

Current (Note 5)

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

10

500

μΑ

μΑ

0.9

300\*

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

 $\Delta$ IBOR

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.
- 5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

D021B

D023

TABLE 11-6: A/D CONVERTER CHARACTERISTICS:

PIC16C710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16C710/711-10 (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16C710/711-20 (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16LC710/711-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	_	_	8-bits	bit	VREF = VDD, VSS ≤ AIN ≤ VREF
A02	EABS	Absolute error	_	_	< ± 1	LSb	VREF = VDD, VSS ≤ AIN ≤ VREF
A03	EIL	Integral linearity error	_	_	< ± 1	LSb	VREF = VDD, VSS ≤ AIN ≤ VREF
A04	EDL	Differential linearity error	_	_	< ± 1	LSb	VREF = VDD, VSS ≤ AIN ≤ VREF
A05	EFS	Full scale error	_	_	< ± 1	LSb	VREF = VDD, VSS ≤ AIN ≤ VREF
A06	Eoff	Offset error	_	_	< ± 1	LSb	VREF = VDD, VSS ≤ AIN ≤ VREF
A10	_	Monotonicity	_	guaranteed		_	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage	2.5V	_	VDD + 0.3	V	
A25	VAIN	Analog input voltage	Vss - 0.3	_	VREF + 0.3	V	
A30	ZAIN	Recommended impedance of analog voltage source	_	_	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	_	180	_	μА	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	10	_	1000	μА	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1.
			_	_	10	μΑ	During A/D Conversion cycle

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup> Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

<sup>2:</sup> VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

#### FIGURE 13-7: A/D CONVERSION TIMING

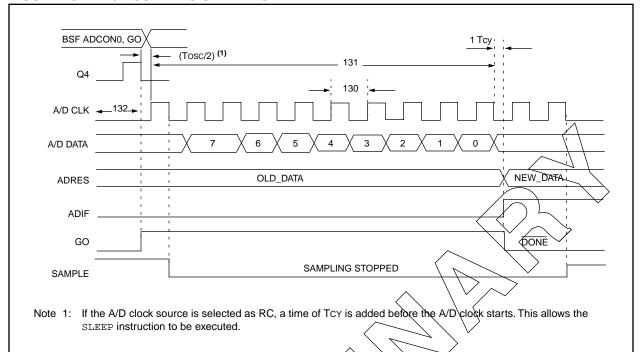


TABLE 13-8: A/D CONVERSION REQUIREMENTS

Parameter	Sym	Characteristic	Min	Турт	Max	Units	Conditions
No.					$\rightarrow$		
130	TAD	A/D clock period	1.6	1/1/4/	<u> </u>	μs	VREF ≥ 3.0V
			2.0		_	μs	VREF full range
130	TAD	A/D Internal RC		$\setminus \setminus \setminus$			ADCS1:ADCS0 = 11
		Oscillator source	\				(RC oscillator source)
			3.0	6.0	9.0	μs	PIC16LC715, VDD = 3.0V
		$\rightarrow$	2.0	4.0	6.0	μs	PIC16C715
131	TCNV	Conversion time		9.5TAD	_	_	
		(not including \$/H					
		time). Note 1	<b>/</b> >				
132	TACQ	Acquisition time	Note 2	20	_	μs	

<sup>\*</sup> These parameters are characterized but not tested.

Note 1: ADRES register may be read on the following Tcy cycle.

<sup>†</sup> Data in type column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

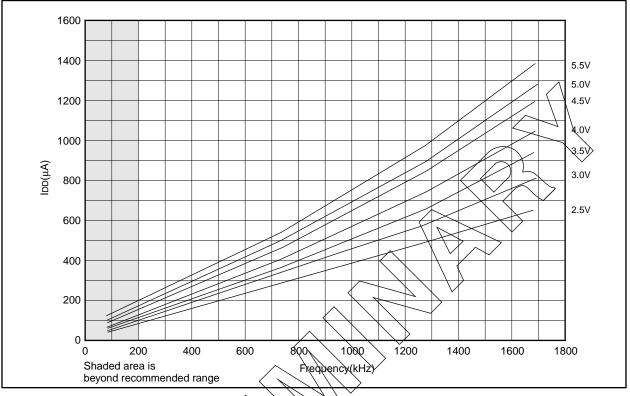


FIGURE 14-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)

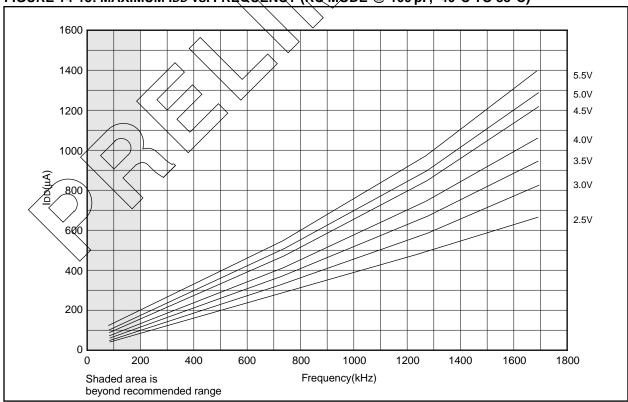


FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

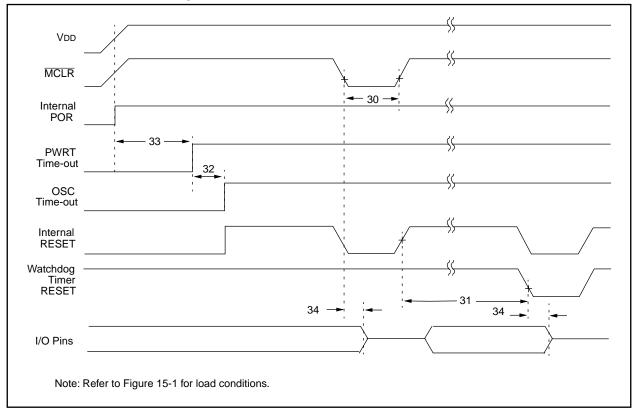


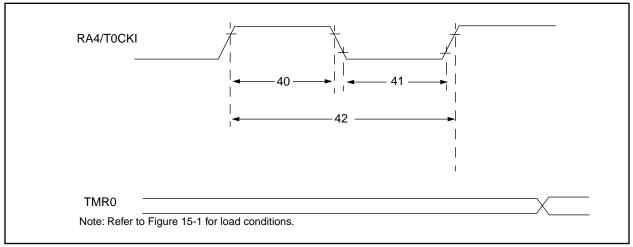
TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	200	_	_	ns	VDD = 5V, -40°C to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	$VDD = 5V$ , $-40^{\circ}C$ to $+85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_	_	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	$VDD = 5V$ , $-40^{\circ}C$ to $+85^{\circ}C$
34	Tıoz	I/O High Impedance from MCLR Low	_	_	100	ns	

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup> Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-5: TIMERO EXTERNAL CLOCK TIMINGS



#### TABLE 15-5: TIMERO EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions	
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	_	_	ns	Must also meet	
			With Prescaler	10		_	ns	parameter 42	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20	_	_	ns	Must also meet parameter 42	
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			With Prescaler	Greater of: 20 ns or Tcy + 40 N				(2, 4,, 256)	

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup> Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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