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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04-p

PIC16C71X

TABLE 1-1: PIC16C71X FAMILY OF DEVICES

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 ⁽¹⁾
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	512	1K	1K	2K	2K	—
Memory	ROM Program Memory (14K words)	—	—	—	—	—	2K
	Data Memory (bytes)	36	36	68	128	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Module(s)	—	—	—	—	1	1
	Serial Port(s) (SPI/I ² C, USART)	—	—	—	—	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	—	—	—	—	—	—
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
Features	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	2.5-6.0	3.0-6.0	2.5-6.0	2.5-5.5	2.5-6.0	3.0-5.5
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
	EPROM Program Memory (x14 words)	4K	4K	8K	8K
Memory	Data Memory (bytes)	192	192	376	376
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Module(s)	2	2	2	2
	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART
	Parallel Slave Port	—	Yes	—	Yes
	A/D Converter (8-bit) Channels	5	8	5	8
	Interrupt Sources	11	12	11	12
Features	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

PIC16C71X

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

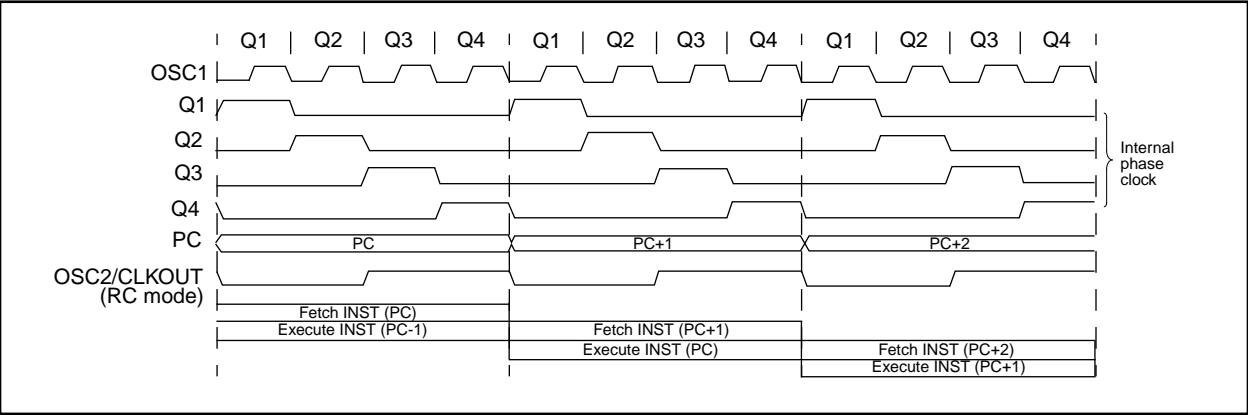
3.2 Instruction Flow/Pipelining

An “Instruction Cycle” consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. *GOTO*) then two cycles are required to complete the instruction (Example 3-1).

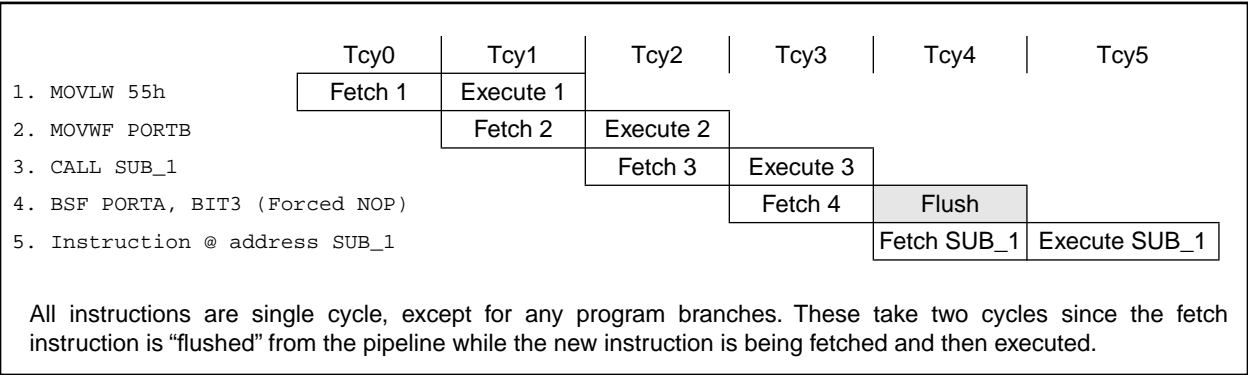
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the “Instruction Register” (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



PIC16C71X

4.2.2.2 OPTION REGISTER

Applicable Devices	710	71	711	715
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The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **RBP_U**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

PIC16C71X

FIGURE 8-2: CONFIGURATION WORD, PIC16C710/711

CP0	CP0	CP0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	PWRT $\overline{\text{E}}$	WDTE	FOSC1	FOSC0	Register: CONFIG Address 2007h
bit13										bit0				
bit 13-7 CP0: Code protection bits ⁽²⁾														
5-4: 1 = Code protection off														
0 = All memory is code protected, but 00h - 3Fh is writable														
bit 6: BODEN: Brown-out Reset Enable bit ⁽¹⁾														
1 = BOR enabled														
0 = BOR disabled														
bit 3: PWRT$\overline{\text{E}}$: Power-up Timer Enable bit ⁽¹⁾														
1 = PWRT disabled														
0 = PWRT enabled														
bit 2: WDTE: Watchdog Timer Enable bit														
1 = WDT enabled														
0 = WDT disabled														
bit 1-0: FOSC1:FOSC0: Oscillator Selection bits														
11 = RC oscillator														
10 = HS oscillator														
01 = XT oscillator														
00 = LP oscillator														
Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRT}}\text{E}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.														
2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.														

FIGURE 8-3: CONFIGURATION WORD, PIC16C715

CP1	CP0	CP1	CP0	CP1	CP0	MPEEN	BODEN	CP1	CP0	PWRT $\overline{\text{E}}$	WDTE	FOSC1	FOSC0	Register: CONFIG Address 2007h
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bit13

bit0

bit 13-8 **CP1:CP0:** Code Protection bits ⁽²⁾

5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **MPEEN:** Memory Parity Error Enable
1 = Memory Parity Checking is enabled
0 = Memory Parity Checking is disabled

bit 6: **BODEN:** Brown-out Reset Enable bit ⁽¹⁾
1 = BOR enabled
0 = BOR disabled

bit 3: **PWRT $\overline{\text{E}}$:** Power-up Timer Enable bit ⁽¹⁾
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRT}}\text{E}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.

2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

TABLE 8-7: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C71

TO	PD	
1	1	Power-on Reset
0	x	Illegal, TO is set on POR
x	0	Illegal, PD is set on POR
0	1	WDT Reset
0	0	WDT Wake-up
u	u	MCLR Reset during normal operation
1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 8-8: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C710/711

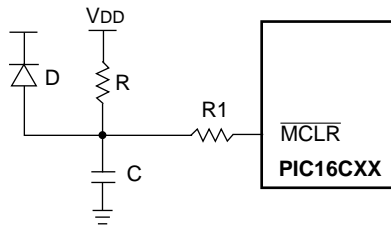
POR	BOR	TO	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	x	x	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 8-9: STATUS BITS AND THEIR SIGNIFICANCE, PIC16C715

PER	POR	BOR	TO	PD	
1	0	x	1	1	Power-on Reset
x	0	x	0	x	Illegal, TO is set on POR
x	0	x	x	0	Illegal, PD is set on POR
1	1	0	x	x	Brown-out Reset
1	1	1	0	1	WDT Reset
1	1	1	0	0	WDT Wake-up
1	1	1	u	u	MCLR Reset during normal operation
1	1	1	1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP
0	1	1	1	1	Parity Error Reset
0	0	x	x	x	Illegal, PER is set on POR
0	x	0	x	x	Illegal, PER is set on BOR

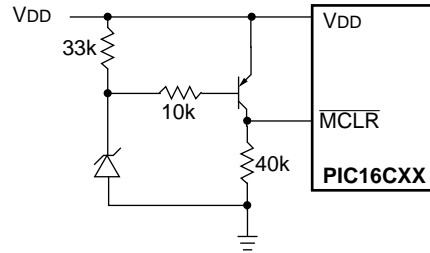
PIC16C71X

FIGURE 8-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



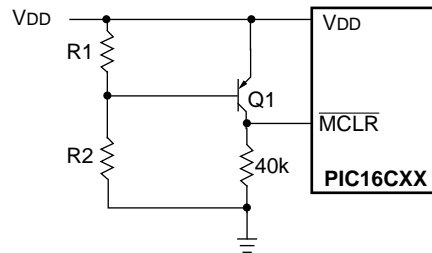
- Note 1: External Power-on Reset circuit is required only if V_{DD} power-up slope is too slow. The diode D helps discharge the capacitor quickly when V_{DD} powers down.
- 2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
- 3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/V_{PP} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 8-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when V_{DD} goes below (V_Z + 0.7V) where V_Z = Zener voltage.
- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 8-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



- Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

10.6 PICDEM-1 Low-Cost PIC16/17 Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

10.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

10.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include

an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

10.9 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from PICMASTER, Microchip's Universal Emulator System.

PIC16C71X

Applicable Devices	710	71	711	715
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- 11.1 DC Characteristics:** **PIC16C710-04 (Commercial, Industrial, Extended)**
PIC16C711-04 (Commercial, Industrial, Extended)
PIC16C710-10 (Commercial, Industrial, Extended)
PIC16C711-10 (Commercial, Industrial, Extended)
PIC16C710-20 (Commercial, Industrial, Extended)
PIC16C711-20 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise stated)							
DC CHARACTERISTICS							
Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)							
Param. No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	- -	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7 3.7	4.0 4.0	4.3 4.4	V V	BODEN configuration bit is enabled Extended Range Only
D010 D013	Supply Current (Note 2)	IDD	- -	2.7 13.5	5 30	mA mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4) HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D015	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V
D020 D021 D021A D021B	Power-down Current (Note 3)	IPD	- - - -	10.5 1.5 1.5 1.5	42 21 24 30	μA μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 5)	ΔIBOR	-	300*	500	μA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = VDD/2R_{ext}$ (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C71X

Applicable Devices	710	71	711	715
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11.4 Timing Parameter Symbolology

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	T	Time

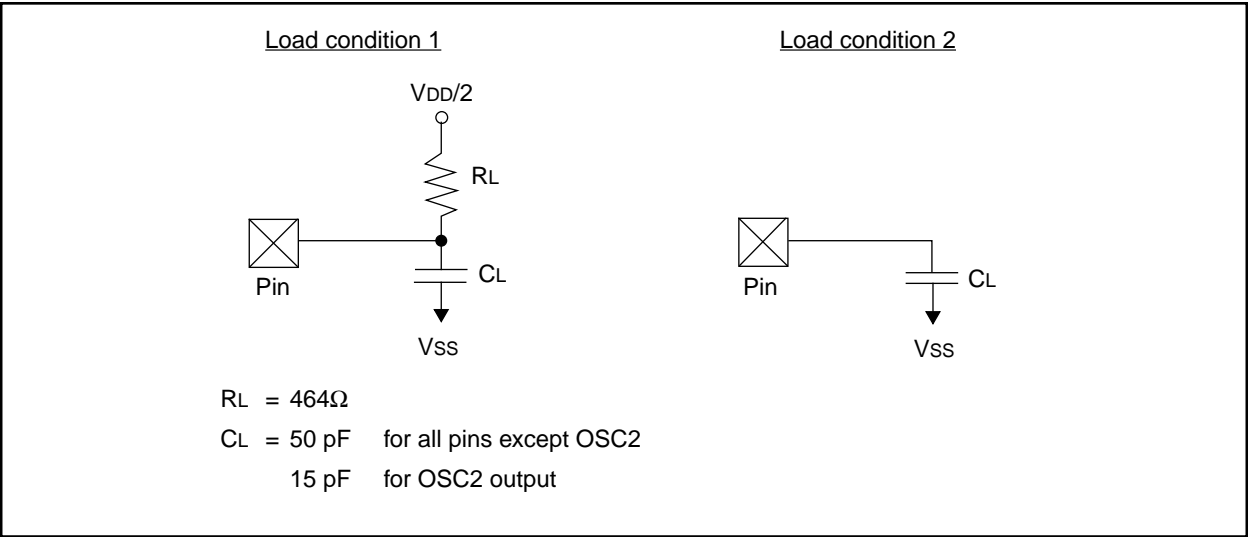
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	ss	SS
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 11-1: LOAD CONDITIONS



PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 11-3: CLKOUT AND I/O TIMING

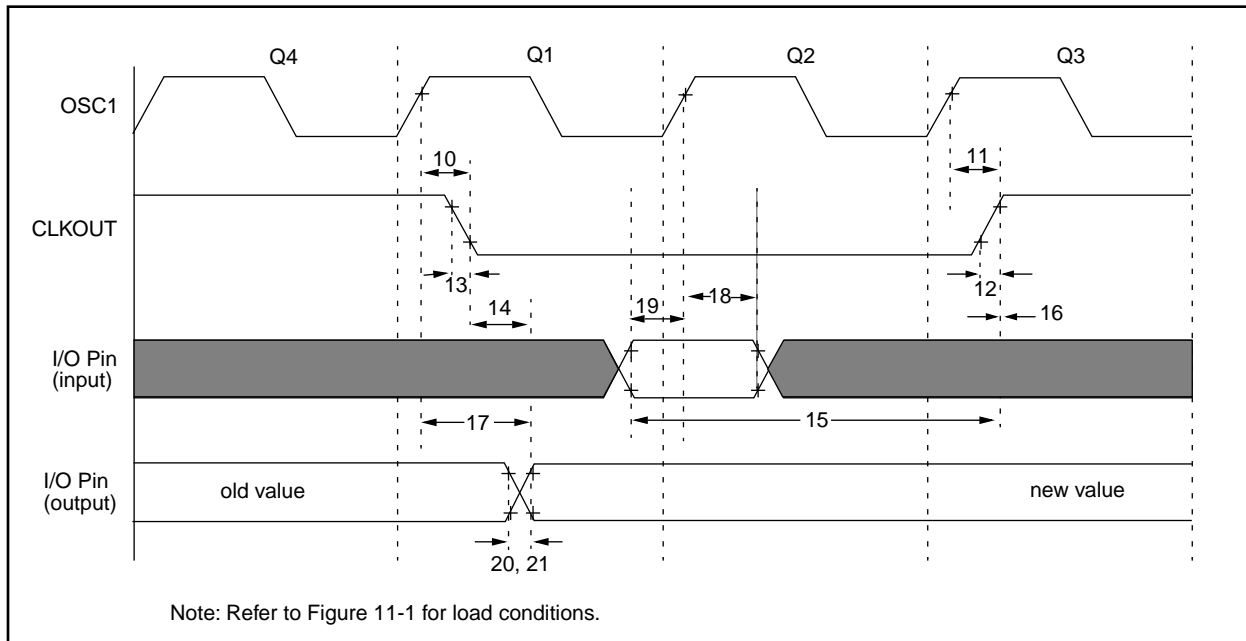


TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5T _{CY} + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	0.25T _{CY} + 25	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16C710/711	—	10	25	ns
			PIC16LC710/711	—	—	60	ns
21*	TioF	Port output fall time	PIC16C710/711	—	10	25	ns
			PIC16LC710/711	—	—	60	ns
22††*	Tinp	INT pin high or low time	20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time	20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x T_{osc}.

PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 11-6: TIMER0 EXTERNAL CLOCK TIMINGS

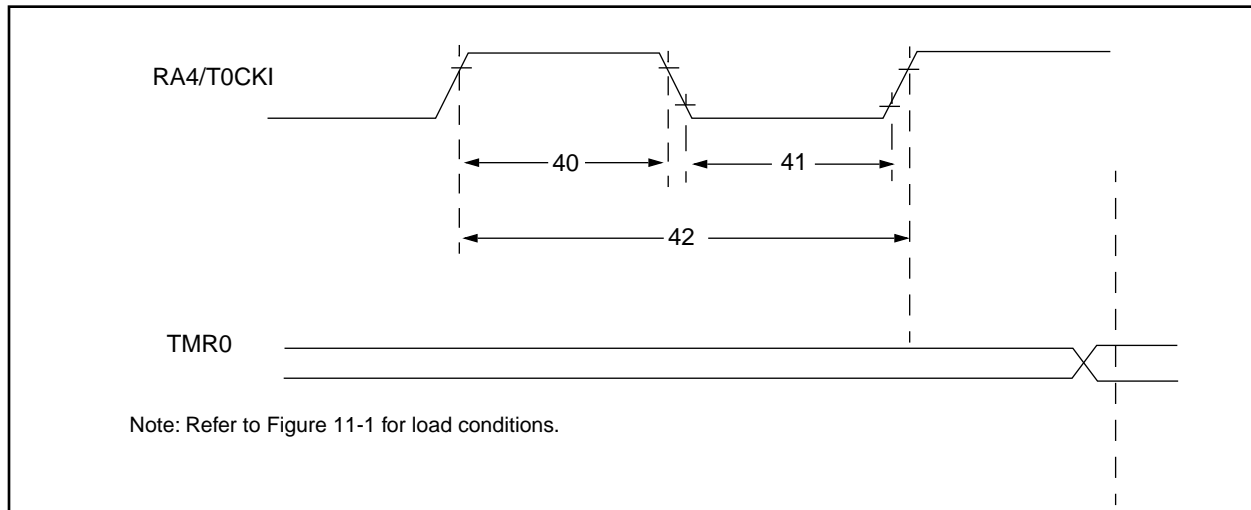


TABLE 11-5: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	Must also meet parameter 42
			With Prescaler	10^*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	Must also meet parameter 42
			With Prescaler	10^*	—	—	ns	
42	Tt0P	T0CKI Period		Greater of: $20 \text{ ns or } \frac{T_{CY} + 40^*}{N}$		—	ns	N = prescale value (2, 4,..., 256)
48	Tcke2tmr1	Delay from external clock edge to timer increment		$2T_{osc}$	—	$7T_{osc}$	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

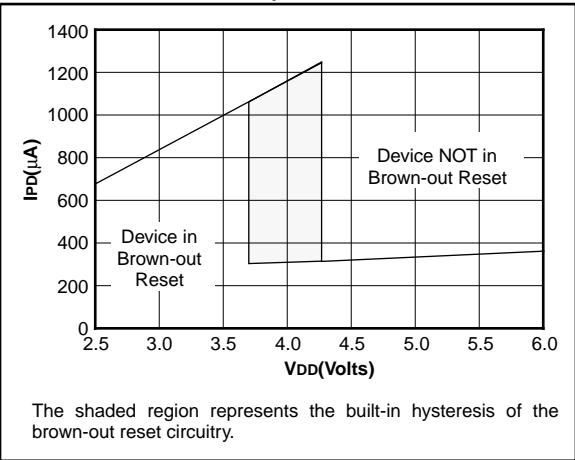


FIGURE 12-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

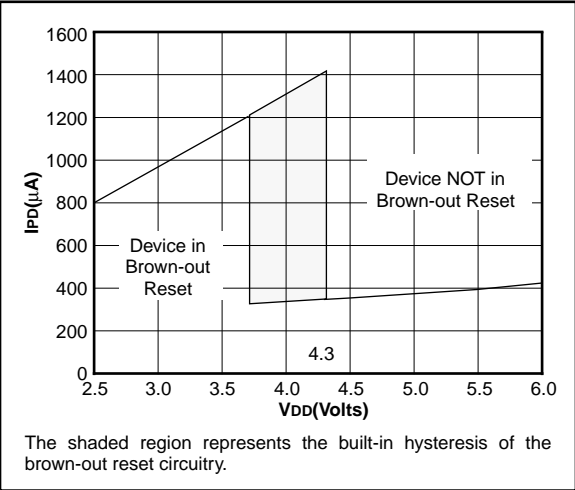


FIGURE 12-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

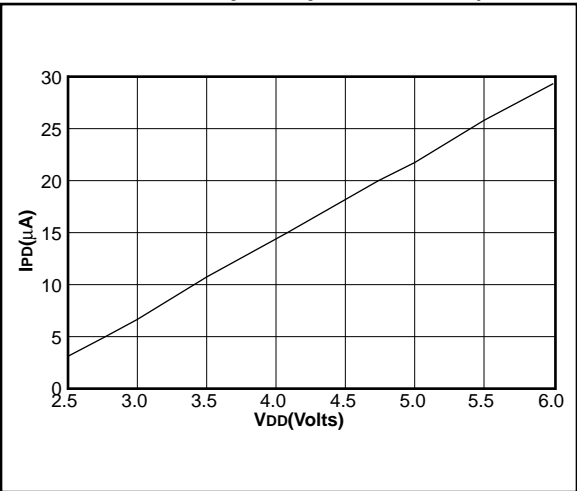


FIGURE 12-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

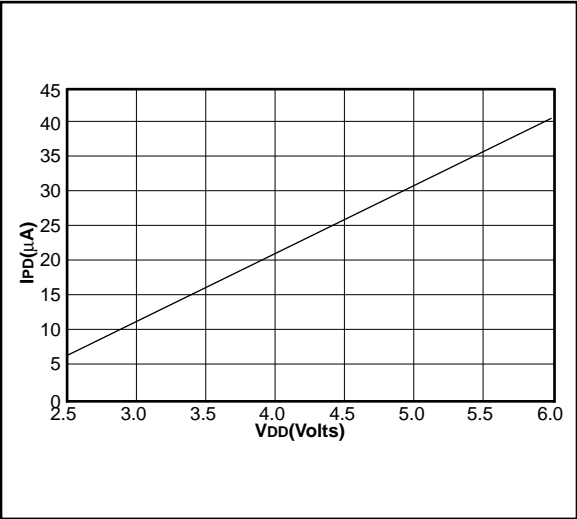


FIGURE 14-18: TYPICAL I_{DD} vs. CAPACITANCE @ 500 kHz (RC MODE)

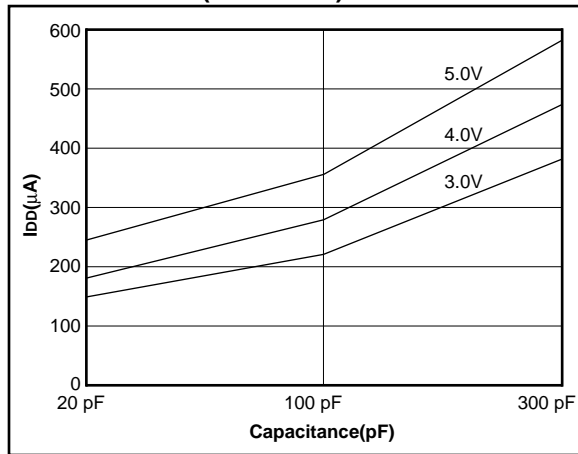


TABLE 14-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average	
		Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5V$.

FIGURE 14-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. V_{DD}

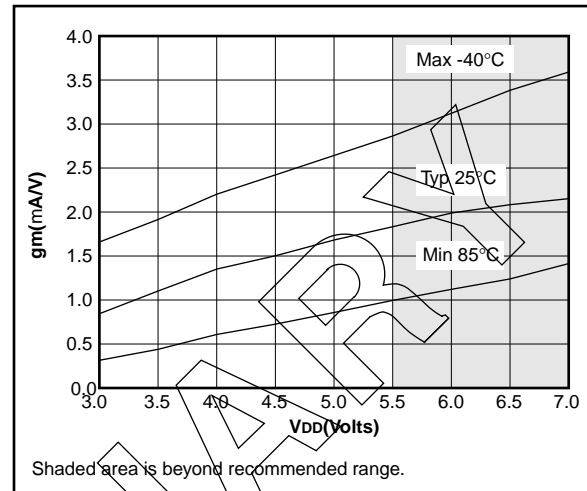


FIGURE 14-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. V_{DD}

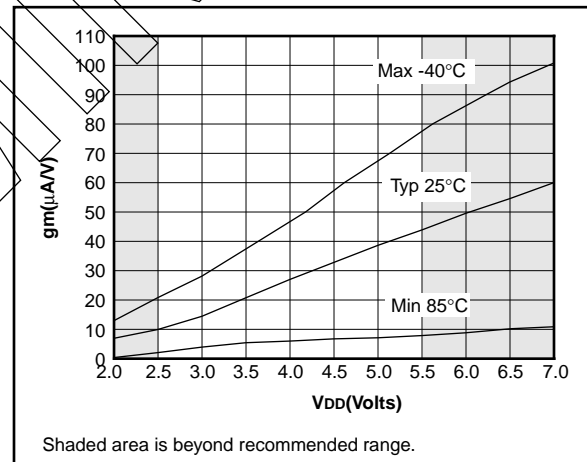
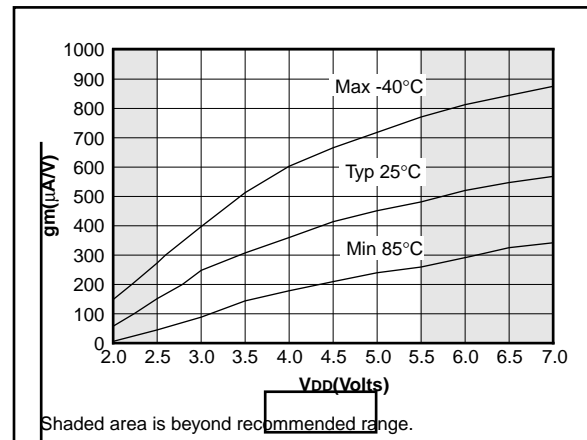


FIGURE 14-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. V_{DD}



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15.3 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial) PIC16LC71-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030 D031 D032 D033	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$, OSC1 (in RC mode) OSC1 (in XT, HS and LP)	V_{IL}	V_{SS}	-	0.15V 0.8V 0.2V _{DD} 0.3V _{DD}	V	For entire V_{DD} range $4.5 \leq V_{DD} \leq 5.5\text{V}$ Note1
D040 D040A D041 D042 D042A D043	Input High Voltage I/O ports (Note 4) with TTL buffer with Schmitt Trigger buffer $\overline{\text{MCLR}}$, RB0/INT OSC1 (XT, HS and LP) OSC1 (in RC mode)	V_{IH}	2.0 0.25V _{DD} + 0.8V 0.85V _{DD} 0.85V _{DD} 0.7V _{DD} 0.9V _{DD}	- - - - - -	V _{DD} V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V	$4.5 \leq V_{DD} \leq 5.5\text{V}$ For entire V_{DD} range For entire V_{DD} range Note1
D070	PORTB weak pull-up current	IPURB	50	250	†400	μA	$V_{DD} = 5\text{V}$, $V_{PIN} = V_{SS}$
D060 D061 D063	Input Leakage Current (Notes 2, 3) I/O ports $\overline{\text{MCLR}}$, RA4/T0CKI OSC1	I_{IL}	- - -	- - -	±1 ±5 ±5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080 D083	Output Low Voltage I/O ports OSC2/CLKOUT (RC osc config)	V_{OL}	- -	- -	0.6 0.6	V	$I_{OL} = 8.5\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $I_{OL} = 1.6\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D090 D092	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (RC osc config)	V_{OH}	$V_{DD} - 0.7$ $V_{DD} - 0.7$	- -	- -	V	$I_{OH} = -3.0\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $I_{OH} = -1.3\text{mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D130*	Open-Drain High Voltage	V_{OD}	-	-	14	V	RA4 pin

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.
- 2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

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FIGURE 15-6: A/D CONVERSION TIMING

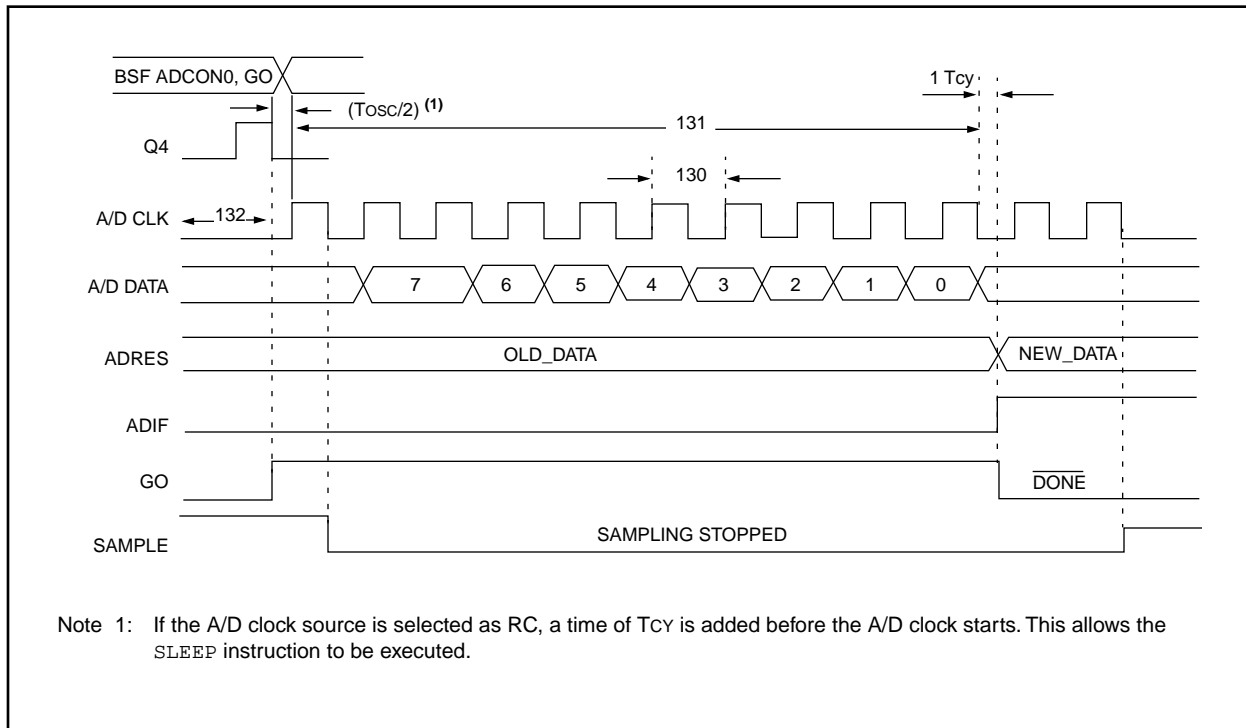


TABLE 15-7: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16C71	2.0	—	—	μs TOSC based, $V_{REF} \geq 3.0\text{V}$
			PIC16LC71	2.0	—	—	μs TOSC based, V_{REF} full range
			PIC16C71	2.0	4.0	6.0	μs A/D RC Mode
			PIC16LC71	3.0	6.0	9.0	μs A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)	—	9.5	—	TAD	
132	TACQ	Acquisition time	Note 2	20	—	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
			5*	—	—	μs	
134	TGO	Q4 to A/D clock start	—	$T_{osc}/2\text{§}$	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the <code>SLEEP</code> instruction to be executed.
135	TSWC	Switching from convert → sample time	1.5§	—	—	TAD	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ These specifications ensured by design.

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Section 7.1 for min conditions.

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FIGURE 16-21: I_{OL} vs. V_{OL} , $V_{DD} = 3V$

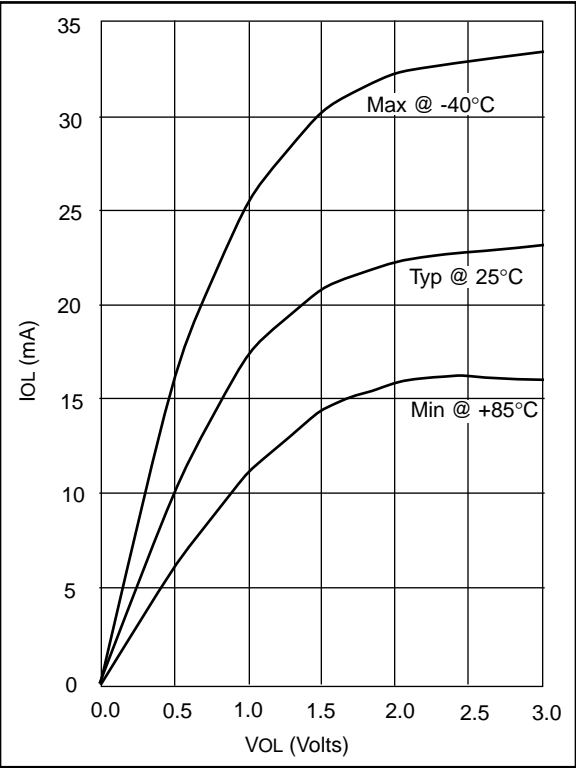
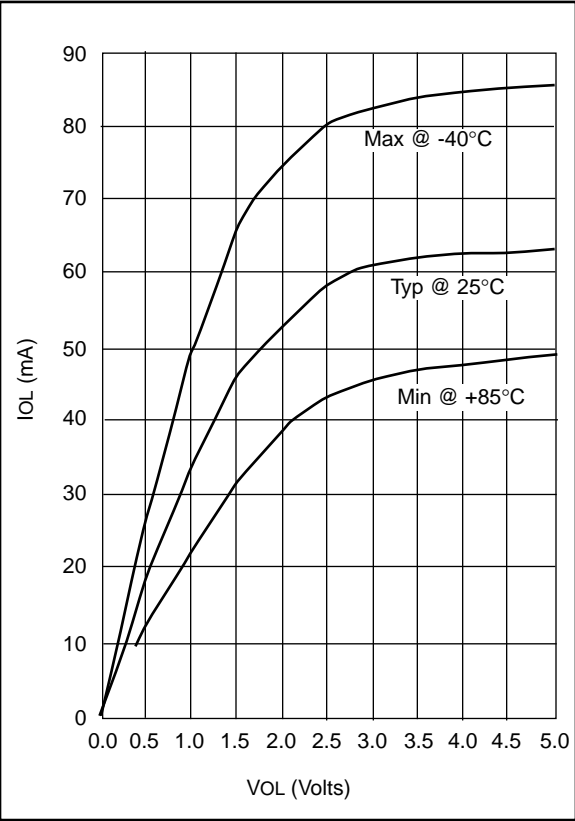
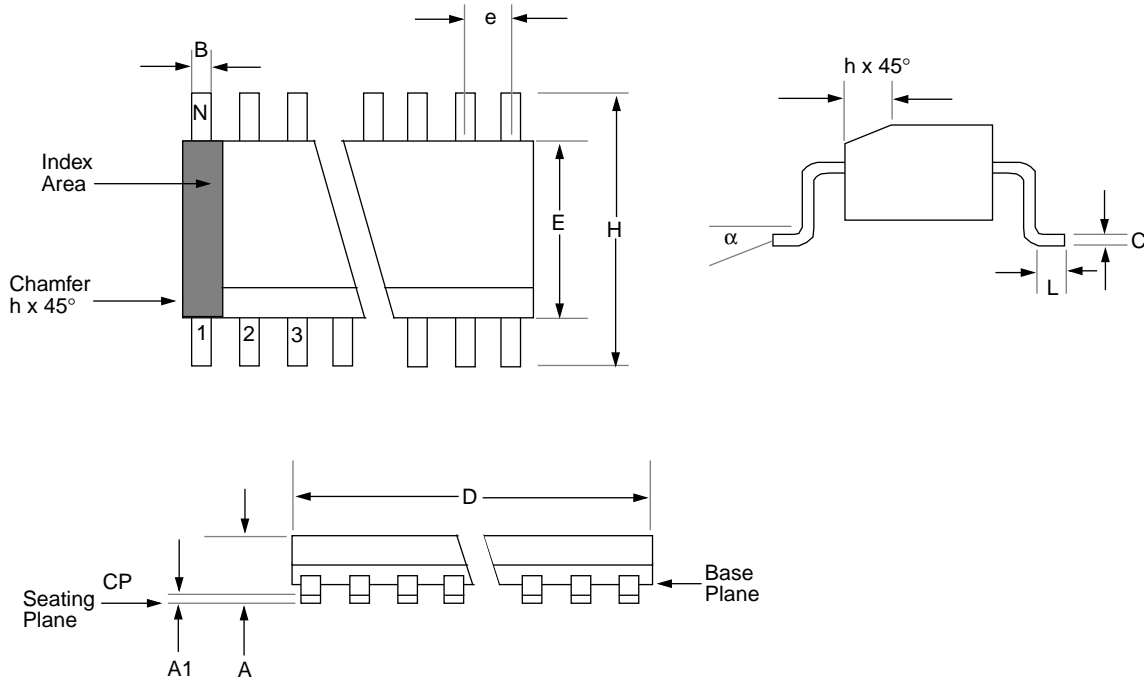


FIGURE 16-22: I_{OL} vs. V_{OL} , $V_{DD} = 5V$



Data based on matrix samples. See first page of this section for details.

17.3 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)(SO)



Package Group: Plastic SOIC (SO)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	18	18		18	18	
CP	—	0.102		—	0.004	

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APPENDIX C: WHAT'S NEW

1. Consolidated all pin compatible 18-pin A/D based devices into one data sheet.

APPENDIX D: WHAT'S CHANGED

1. Minor changes, spelling and grammatical changes.
2. Low voltage operation on the PIC16LC710/711/715 has been reduced from 3.0V to 2.5V.
3. Part numbers of the PIC16C70 and PIC16C71A have changed to PIC16C710 and PIC16C711, respectively.

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