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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04e-p

#### 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C71X device.

Device	Program Memory	Data Memory
PIC16C710	512 x 14	36 x 8
PIC16C71	1K x 14	36 x 8
PIC16C711	1K x 14	68 x 8
PIC16C715	2K x 14	128 x 8

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow bit and a digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input
RA1/AN1	bit1	TTL	Input/output or analog input
RA2/AN2	bit2	TTL	Input/output or analog input
RA3/AN3/VREF	bit3	TTL	Input/output or analog input/VREF
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0
			Output is open drain type

Legend: TTL = TTL input, ST = Schmitt Trigger input

#### TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA	_	_	_	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	_	_	_	PORTA D	Data Direct	tion Registe	1 1111	1 1111		
9Fh	ADCON1	_	_	_	_	_	_	PCFG1	PCFG0	00	00

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

#### 6.3 Prescaler

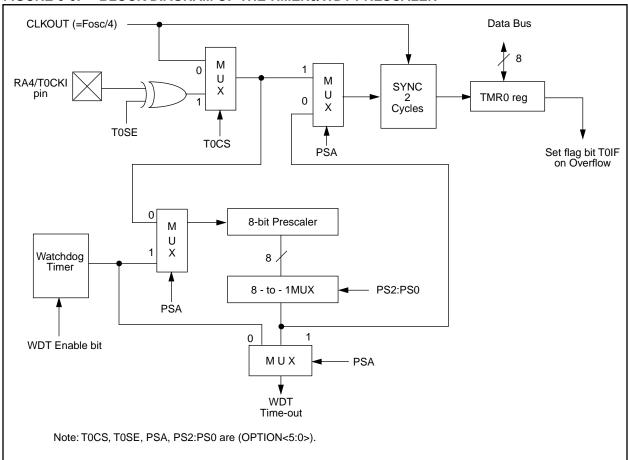
An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1,x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMERO/WDT PRESCALER



Note:

#### 7.9 <u>Transfer Function</u>

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is Analog VREF/256 (Figure 7-6).

#### 7.10 References

A very good reference for understanding A/D converters is the "Analog-Digital Conversion Handbook" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).

FIGURE 7-6: A/D TRANSFER FUNCTION

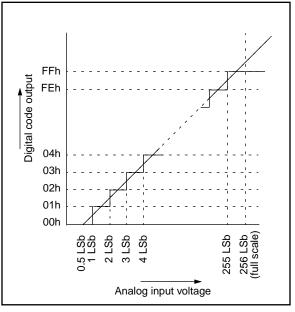


FIGURE 7-7: FLOWCHART OF A/D OPERATION

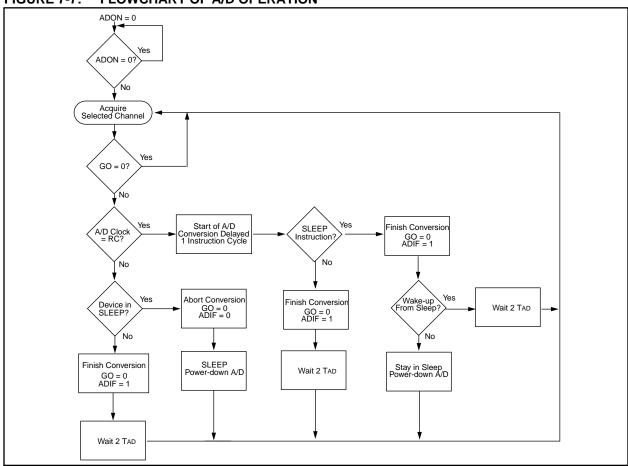
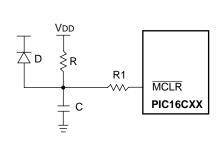
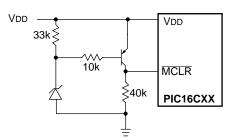


FIGURE 8-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



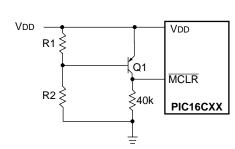
- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
  - 2:  $R < 40 \text{ k}\Omega$  is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
  - 3:  $R1 = 100\Omega$  to 1 k $\Omega$  will limit any current flowing into  $\overline{MCLR}$  from external capacitor C in the event of  $\overline{MCLR}$ /VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

### FIGURE 8-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
  - Resistors should be adjusted for the characteristics of the transistor.

### FIGURE 8-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

IORWF	Inclusive OR W with f								
Syntax:	[ label ]	IORWF	f,d						
Operands:	$0 \le f \le 12$ $d \in [0,1]$	27							
Operation:	(W) .OR.	$(f) \rightarrow (de$	est)						
Status Affected:	Z								
Encoding:	00	0100	dfff	ffff					
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
	Decode	Read register 'f'	Process data	Write to dest					
Example	IORWF		RESULT,	0					
	Before In								
		RESULT W	= 0x13 = 0x91						
	After Inst	• •		3					

MOVLW	Move Lit	eral to V	V				
Syntax:	[ label ]	MOVLW	/ k				
Operands:	$0 \le k \le 2$	55					
Operation:	$k \to (W)$						
Status Affected:	None						
Encoding:	11	00xx	kkkk	kkkk			
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read literal 'k'	Process data	Write to W			
Example	MOVLW After Inst	0x5A ruction W =	0x5A				

MOVF	Move f							
Syntax:	[ label ]	MOVF	f,d					
Operands:	$0 \le f \le 127$ $d \in [0,1]$							
Operation:	$(f) \rightarrow (des$	st)						
Status Affected:	Z							
Encoding:	0.0	1000	dfff	ffff				
Description:	The contents of register f is moved to a destination dependant upon the status of d. If $d = 0$ , destination is W register. If $d = 1$ , the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to dest				
Example	MOVF	FSR,	0					
	After Instruction $W = \text{value in FSR reg}$ $Z = 1$							

Move W	to f		
[ label ]	MOVWI	F f	
$0 \le f \le 12$	27		
$(W) \rightarrow (f)$	)		
None			
00	0000	1fff	ffff
Move data	from W r	egister to	register
1			
1			
Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write register 'f'
MOVWF	OPTIO	ON_REG	
After Inst	OPTION W ruction OPTION	= 0xFi = 0x4F	=
	[label] $0 ≤ f ≤ 12 $ $(W) → (f) $ None $00 $ Move data 'f'. $1 $ $01 $ Decode $MOVWF $ Before In	$0 \le f \le 127$ $(W) \to (f)$ None $00  0000$ Move data from W r r'. $1$ $1$ $Q1  Q2$ $Decode  Read register r'. MOVWF  OPTIO Before \ Instruction OPTION W After \ Instruction$	

XORLW	Exclusive OR Literal with W	XORWF	Exclusive OR W with f
Syntax:	[ <i>label</i> ] XORLW k	Syntax:	[ <i>label</i> ] XORWF f,d
Operands:	0 ≤ k ≤ 255	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(W)$ .XOR. $k \rightarrow (W)$	Operation:	(W) .XOR. (f) $\rightarrow$ (dest)
Status Affected:	Z	Status Affected:	Z
Encoding:	11   1010   kkkk   kkkk	Encoding:	00 0110 dfff ffff
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored heal; in register.
Words:	1		is 1 the result is stored back in register 'f'.
Cycles:	1	Words:	1
Q Cycle Activity:	Q1 Q2 Q3 Q4	Cycles:	1
	Decode Read Process Write to literal 'k' data W	Q Cycle Activity:	Q1 Q2 Q3 Q4
Example:	XORLW 0xAF		Decode Read register data Write to dest
	Before Instruction		
	W = 0xB5	Example	XORWF REG 1
	After Instruction		Before Instruction
	W = 0x1A		$ \begin{array}{rcl} REG & = & 0xAF \\ W & = & 0xB5 \end{array} $
			After Instruction
			REG = 0x1A W = 0xB5

#### 10.0 DEVELOPMENT SUPPORT

#### 10.1 <u>Development Tools</u>

The PICmicro<sup>™</sup> microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART<sup>®</sup> Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy Logic Development System (fuzzyTECH<sup>®</sup>–MP)

# 10.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

#### 10.3 <u>ICEPIC: Low-Cost PIC16CXXX</u> In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT<sup>®</sup> through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

#### 10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In standalone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

#### 10.5 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

FIGURE 12-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

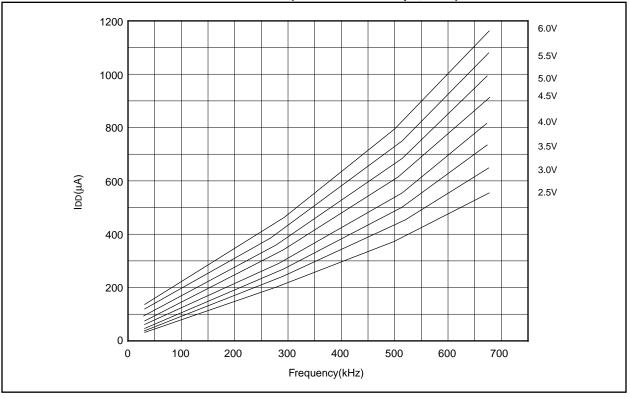
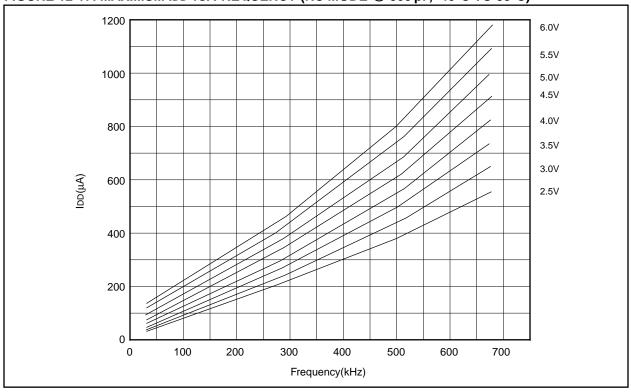


FIGURE 12-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



DC CHARACTERISTICS

#### Applicable Devices 710 71 711 715

#### Standard Operating Conditions (unless otherwise stated)

Operating temperature  $0^{\circ}C \leq TA \leq +70^{\circ}C$  (commercial)

 $-40^{\circ}$ C  $\leq$  TA  $\leq$  +85 $^{\circ}$ C (industrial)

 $-40^{\circ}$ C  $\leq$  TA  $\leq$  +125 $^{\circ}$ C (extended)

Operating voltage VDD range as described in DC spec Section 13.1

and Section 13.2.

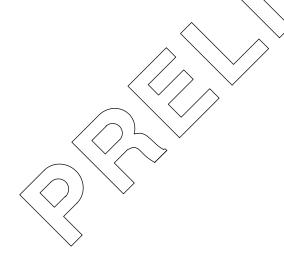
D	Description Own Min Tow May Help On ditions								
Param	Characteristic	Sym	Min	Тур	Max	Units	Conditions		
No.				†					
	Output High Voltage						4		
D090	I/O ports (Note 3)	Vон	VDD - 0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V,		
D090A			VDD - 0.7	-	-	V	-40°C to +85°C IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C		
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V,		
D092A			VDD - 0.7	-	-	V	ION = -1.0 mA, VDD = 4.5V, -40°C to +125°C		
	Capacitive Loading Specs on Output Pins					7			
D100	OSC2 pin	Cosc <sub>2</sub>	-	-	15	p/F /	In XT, HS and LP modes when external clock is used to drive OSC1.		
D101	All I/O pins and OSC2 (in RC mode)	Cıo	-	(-	50	pĘ	0401.		

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC made.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.



Applicable Devices 710 71 711 715

15.3 DC Characteristics: PIC16C71-04 (Commercial, Industrial)

PIC16C71-20 (Commercial, Industrial) PIC16LC71-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)

OOperating temperature  $0^{\circ}C$   $\leq TA \leq +70^{\circ}C$  (commercial)

**DC CHARACTERISTICS**  $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C} \text{ (industrial)}$ 

Operating voltage  $\ensuremath{\text{VDD}}$  range as described in DC spec Section 15.1

and Section 15.2.

	and Section 15.2.									
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions			
	Input Low Voltage									
	I/O ports	VIL								
D030	with TTL buffer		Vss	_	0.15V	V	For entire VDD range			
D031	with Schmitt Trigger buffer		Vss	_	0.8V	V	4.5 ≤ VDD ≤ 5.5V			
D032	MCLR, OSC1 (in RC mode)		Vss	_	0.2VDD	V				
D033	OSC1 (in XT, HS and LP)		Vss	-	0.3VDD	V	Note1			
	Input High Voltage									
	I/O ports (Note 4)	ViH		-						
D040	with TTL buffer		2.0	-	Vdd	V	4.5 ≤ VDD ≤ 5.5V			
D040A			0.25VDD + 0.8V	-	VDD		For entire VDD range			
D041	with Schmitt Trigger buffer		0.85VDD	_	VDD		For entire VDD range			
D041	MCLR, RB0/INT		0.85VDD		VDD	V	or chare vbb range			
D042A	OSC1 (XT, HS and LP)		0.7VDD	_	VDD	V	Note1			
D043	OSC1 (in RC mode)		0.9VDD	_	VDD	V				
D070	PORTB weak pull-up current	IPURB	50	250		μΑ	VDD = 5V, VPIN = VSS			
	Input Leakage Current (Notes 2, 3)				1.00	P				
D060	I/O ports	lıL	-	-	±1	μΑ	Vss ≤ VPIN ≤ VDD, Pin at hi- impedance			
D061	MCLR, RA4/T0CKI		_	_	±5	μA	Vss ≤ VPIN ≤ VDD			
D063	OSC1		-	-	±5	μΑ	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration			
	Output Low Voltage									
D080	I/O ports	Vol	-	-	0.6	V	IOL = 8.5mA, VDD = 4.5V, -40°C to +85°C			
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	IOL = 1.6mA, VDD = 4.5V, -40°C to +85°C			
	Output High Voltage									
D090	I/O ports (Note 3)	Vон	VDD - 0.7	-	-	V	IOH = -3.0mA, VDD = 4.5V, -40°C to +85°C			
D092	OSC2/CLKOUT (RC osc config)		VDD - 0.7	-	-	V	IOH = -1.3mA, VDD = 4.5V, -40°C to +85°C			
D130*	Open-Drain High Voltage	Vod	-	-	14	V	RA4 pin			
	= =		1	1		1	I .			

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

FIGURE 15-3: CLKOUT AND I/O TIMING

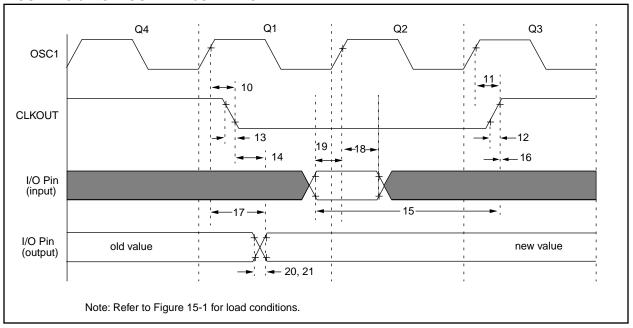


TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		_	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		_	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		_	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		_	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	d	_	_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOL	JT ↑	0.25Tcy + 25	_	_	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT	0	_	_	ns	Note 1	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		_		80 - 100	ns	
18*	TosH2iol	OSC1↑ (Q2 cycle) to	PIC16 <b>C</b> 71	100	_	_	ns	
		Port input invalid (I/O in hold time)	PIC16 <b>LC</b> 71	200		_	ns	
19*	TioV2osH	Port input valid to OSC11	(I/O in setup time)	0	_	_	ns	
20*	TioR	Port output rise time	PIC16 <b>C</b> 71	_	10	25	ns	
			PIC16 <b>LC</b> 71	_	_	60	ns	
21*	TioF	Port output fall time	PIC16 <b>C</b> 71	_	10	25	ns	
			PIC16 <b>LC</b> 71	_		60	ns	
22††*	Tinp	INT pin high or low time		20	_		ns	
23††*	Trbp	RB7:RB4 change INT high	or low time	20	_	_	ns	

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup>Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

<sup>††</sup> These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

FIGURE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

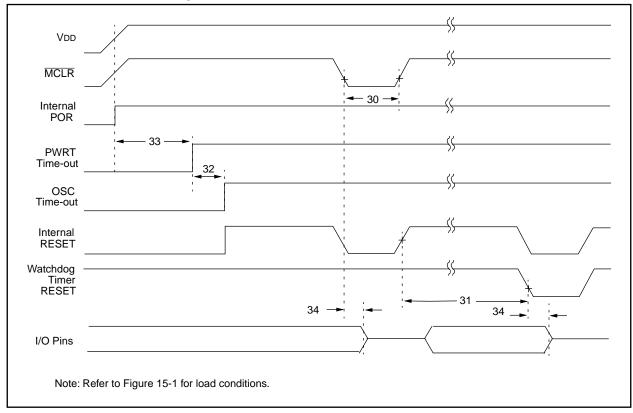


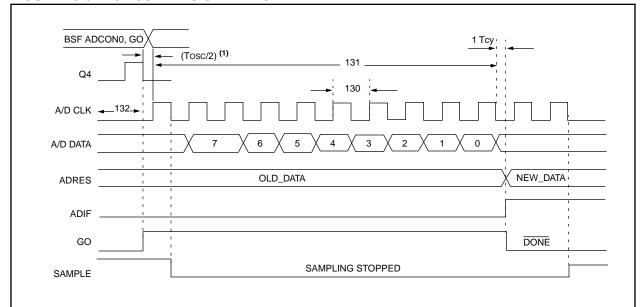
TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	200	_	_	ns	VDD = 5V, -40°C to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	$VDD = 5V$ , $-40^{\circ}C$ to $+85^{\circ}C$
32	Tost	Oscillation Start-up Timer Period	_	1024 Tosc	_	_	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	$VDD = 5V$ , $-40^{\circ}C$ to $+85^{\circ}C$
34	Tıoz	I/O High Impedance from MCLR Low	_	_	100	ns	

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup> Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

#### FIGURE 15-6: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

#### TABLE 15-7: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16 <b>C</b> 71	2.0	_	_	μs	Tosc based, VREF ≥ 3.0V
			PIC16 <b>LC</b> 71	2.0	_	_	μs	Tosc based, VREF full range
			PIC16 <b>C</b> 71	2.0	4.0	6.0	μs	A/D RC Mode
			PIC16 <b>LC</b> 71	3.0	6.0	9.0	μs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time	_	9.5	_	TAD		
132 TACQ	Acquisition time	Note 2	20	_	μs			
				5*	_	_	μѕ	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	Tgo	Q4 to A/D clock start		_	Tosc/2§	_	_	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	Tswc	Switching from conve	$ert \rightarrow sample time$	1.5§	_	_	TAD	

<sup>\*</sup> These parameters are characterized but not tested.

<sup>†</sup> Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

These specifications ensured by design.

Note 1: ADRES register may be read on the following TcY cycle.

<sup>2:</sup> See Section 7.1 for min conditions.

FIGURE 16-14: MAXIMUM IDD VS. FREQ WITH A/D OFF (EXT CLOCK, -55° TO +125°C)

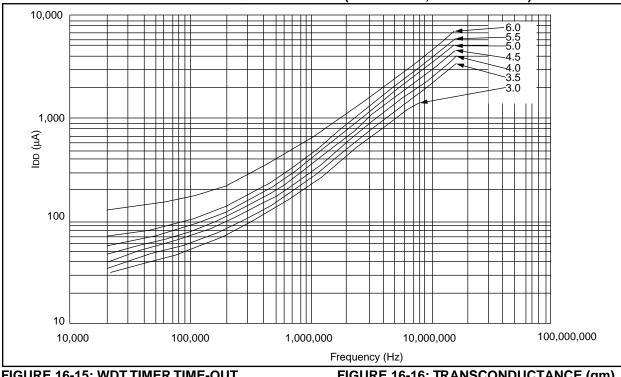


FIGURE 16-15: WDT TIMER TIME-OUT PERIOD vs. VDD

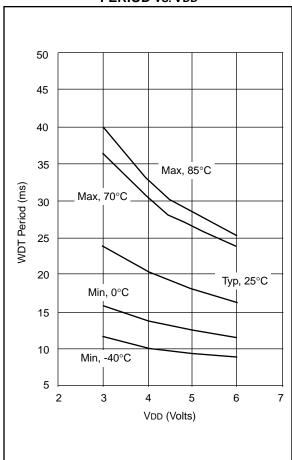
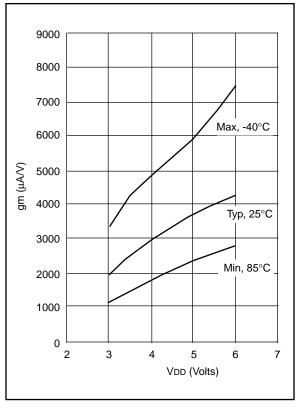
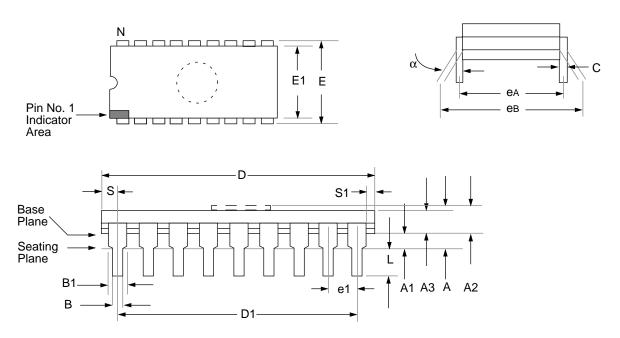


FIGURE 16-16: TRANSCONDUCTANCE (gm)
OF HS OSCILLATOR vs. VDD



#### 17.0 PACKAGING INFORMATION

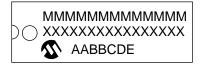
#### 17.1 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)



Package Group: Ceramic CERDIP Dual In-Line (CDP)							
	Millimeters			Inches			
Symbol	Min	Max	Notes	Min	Max	Notes	
α	0°	10°		0°	10°		
Α	_	5.080		_	0.200		
A1	0.381	1.7780		0.015	0.070		
A2	3.810	4.699		0.150	0.185		
А3	3.810	4.445		0.150	0.175		
В	0.355	0.585		0.014	0.023		
B1	1.270	1.651	Typical	0.050	0.065	Typical	
С	0.203	0.381	Typical	0.008	0.015	Typical	
D	22.352	23.622		0.880	0.930		
D1	20.320	20.320	Reference	0.800	0.800	Reference	
E	7.620	8.382		0.300	0.330		
E1	5.588	7.874		0.220	0.310		
e1	2.540	2.540	Reference	0.100	0.100	Reference	
eA	7.366	8.128	Typical	0.290	0.320	Typical	
eB	7.620	10.160		0.300	0.400		
L	3.175	3.810		0.125	0.150		
N	18	18		18	18		
S	0.508	1.397		0.020	0.055		
S1	0.381	1.270		0.015	0.050		

#### 17.5 Package Marking Information

#### 18-Lead PDIP



#### 18-Lead SOIC



#### 18-Lead CERDIP Windowed



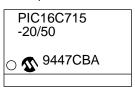
#### 20-Lead SSOP



#### Example



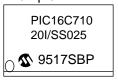
#### Example



#### Example



#### Example



Legend:	MMM	Microchip part number information
	XXX	Customer specific information*
	AA	Year code (last 2 digits of calender year)
	BB	Week code (week of January 1 is week '01')
	С	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A. S = Tempe, Arizona, U.S.A.
	$D_1$	Mask revision number for microcontroller
	E	Assembly code of the plant or country of origin in which part was assembled.
Note:	line, it will	ent the full Microchip part number cannot be marked on one be carried over to the next line thus limiting the number of characters for customer specific information.

<sup>\*</sup> Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask revision number, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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