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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04e-so

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A twostage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C71X device.

Device	Program Memory	Data Memory
PIC16C710	512 x 14	36 x 8
PIC16C71	1K x 14	36 x 8
PIC16C711	1K x 14	68 x 8
PIC16C715	2K x 14	128 x 8

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow bit and a digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

4.2 Data Memory Organization

The data memory is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bit RP0 is the bank select bit.

RP0 (STATUS<5>) = $1 \rightarrow \text{Bank } 1$

RP0 (STATUS<5>) = $0 \rightarrow \text{Bank } 0$

Each Bank extends up to 7Fh (128 bytes). The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. Both Bank 0 and Bank 1 contain special function registers. Some "high use" special function registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

FIGURE 4-4: PIC16C710/71 REGISTER FILE MAP

File	.e		File				
004	IND=(1)	илос(1)					
00n			- 80n				
010		OPTION	- 0111 - 02h				
020		PUL	- 0211 - 02h				
031		STATUS ESD	- 0311 - 046				
0411 05b			- 0411 - 056				
051			0011				
076	PURID		- 0011 - 976				
0711							
001			001				
0911			0911				
	INTCON						
0Ch		General					
	General	Purpose					
	Purpose	Register					
	Register	Mapped					
		In Bank 0.00					
2Fh			AFh				
30h			B0h				
(\						
			\checkmark				
7Fh			FFh				
	Bank 0	Bank 1	_				
	Banko	Bank					
	Unimplemented	data memory locat	tions read				
	as '0'.						
Note 1:	Not a physical re	gister.					
2:	2: The PCON register is not implemented on the						
3:	These locations a	are unimplemented	d in Bank 1.				
5.	Any access to the	ese locations will a	access the				
	corresponding Ba	ank 0 register.					

FIGURE 4-5: PIC16C711 REGISTER FILE MAP



FIGURE 4-6: PIC16C715 REGISTER FILE MAP

File Address	3		File Address				
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h				
01h	TMR0	OPTION					
02h	PCL	PCL					
03h	STATUS	STATUS	83h				
04h	FSR	FSR					
05h	PORTA	TRISA					
06h	PORTB	TRISB					
07h			87h				
08h							
09h			89h				
0Ah	PCLATH	PCLATH	8Ah				
0Bh	INTCON	INTCON	8Bh				
0Ch	PIR1	PIE1	8Ch				
0Dh			8Dh				
0Eh		PCON	8Eh				
0Fh			8Fh				
10h							
11h							
12h							
13h			 93h				
14h							
15h			95h				
16h			96h				
17h			97h				
18h							
19h							
1Ah			9Ah				
1Bh			9Bh				
1Ch			9Ch				
1Dh			9Dh				
1Eh	ADRES		9Eh				
1Fh	ADCON0	ADCON1					
20h	General Purpose	General Purpose	A0h				
	Register	Register	BFh				
			Con				
7Fh	Bank 0	Bank 1	_ FFh				
Unimplemented data memory locations, read as '0'. Note 1: Not a physical register.							

4.2.2.2 OPTION REGISTER

Applicable Devices 710 71 711 715

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)

R/W-1	R/W-1	R/W-1 F	R/W-1 R/W-1	R/W-1	R/W-1	R/W-1					
RBPU bit7	INTEDG	TOCS	TOSE PSA	PS2	PS1	PS0 bit0	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset				
bit 7:	RBPU: PO 1 = PORTE 0 = PORTE	RTB Pull-up 3 pull-ups ai 3 pull-ups ai	o Enable bit re disabled re enabled by inc	lividual port	latch value	es					
bit 6:	bit 6: INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin										
bit 5:	 a TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) 										
bit 4:	TOSE: TMF 1 = Increm 0 = Increm	R0 Source E ent on high- ent on low-t	Edge Select bit to-low transition o-high transition	on RA4/T0 on RA4/T0	CKI pin CKI pin						
bit 3:	PSA: Prese 1 = Presca 0 = Presca	caler Assigr ler is assigr ler is assigr	nment bit ned to the WDT ned to the Timer() module							
bit 2-0:	PS2:PS0:	Prescaler R	ate Select bits								
	Bit Value	TMR0 Rate	WDT Rate								
	000 001 010 011 100 101 110 111	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128								

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

4.2.2.3 INTCON REGISTER

Applicable Devices 710 71 711 715

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

FIGURE 4-9: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	R. – Roodoblo hit			
bit7				KDIE			bit0	W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset			
bit 7:	GIE: ⁽¹⁾ Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts										
bit 6:	 ADIE: A/D Converter Interrupt Enable bit 1 = Enables A/D interrupt 0 = Disables A/D interrupt 										
bit 5:	 TOIE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt 										
bit 4:	INTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt										
bit 3:	RBIE: RB 1 = Enabl 0 = Disab	B Port Cha les the RB les the RB	nge Interr port char 3 port chai	upt Enable ige interru nge interru	e bit pt ıpt						
bit 2:	TOIF: TMI 1 = TMRC 0 = TMRC	R0 Overflo) register ł) register o	ow Interrup has overflo did not ove	ot Flag bit wed (mus erflow	t be cleare	d in softwa	re)				
bit 1:	INTF: RB 1 = The R 0 = The R	0/INT Exte 80/INT ex 80/INT ex	ernal Inter aternal inte aternal inte	rupt Flag b errupt occu errupt did r	oit urred (must not occur	be cleared	d in softwar	e)			
bit 0:	RBIF: RB 1 = At lea 0 = None	Port Cha ist one of t of the RB	nge Interro he RB7:R 7:RB4 pin	upt Flag bi B4 pins ch s have cha	it nanged sta anged state	te (must be	e cleared in	software)			
Note 1:	For the P tionally re for a deta	IC16C71, -enabled I iled descr	if an interr by the RET iption.	rupt occurs	s while the ction in the	GIE bit is t user's Inter	being cleare rrupt Servic	ed, the GIE bit may be uninten- e Routine. Refer to Section 8.5			
Interru global enabli	upt flag bits I enable bit, ing an interr	get set whe GIE (INTC	en an interru ON<7>). Us	pt condition er software	n occurs reg should ens	ardless of th ure the appr	e state of its opriate interr	corresponding enable bit or the rupt flag bits are clear prior to			

FIGURE 8-2: CONFIGURATION WORD, PIC16C710/711

CP0	CF	0 C	P0	CP0	CP0	CP0	CP0	BODEN	CP0	CP0	PWRTE	WDTE	FOSC1	FOSC0	Register:	CONFIG
oit13														bit0	Address	2007h
bit 13- 5- bit 6:	-7 4:	CP0: 1 = C 0 = Al BODE 1 = B 0 = B	Cod ode II me E N: I OR (OR (le prote protec emory i Brown- enable disable	ection b tion off is code out Re d	protec set En	ted, bu able bi	ut 00h - 3 _t (1)	Fh is w	vritable						
bit 3:		PWR 1 = P' 0 = P'	TE: WR1 WR1	Power- Γ disab Γ enab	up Tim led led	er Ena	ble bit	(1)								
bit 2:		WDTI 1 = W 0 = W	E: W /DT /DT	/atchdo enable disable	og Time d ed	er Enab	le bit									
bit 1-C):	FOSC 11 = 10 = 01 = 2 00 =	C1:F RC o HS o XT o LP o	OSCO oscillat oscillat oscillato	: Oscilla or or or or or	ator Se	lection	bits								
Note	1:	Enabl Ensur	ling l re th	Brown∙ e Powe	out Re er-up T	set aut imer is	omatic enable	ally enated anytim	oles Po ne Brov	wer-up vn-out f	Timer (F Reset is	WRT) enabled	regardle d.	ess of the	e value of bit \overline{F}	PWRTE.

2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.

FIGURE 8-3: CONFIGURATION WORD, PIC16C715

CP1	CP0	CP1	CP0	CP1	CP0	MPEEN	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	Register:	CONFIG
bit13													bit0	Address	2007h
bit 13- 5-	 bit 13-8 CP1:CP0: Code Protection bits ⁽²⁾ 5-4: 11 = Code protection off 10 = Upper half of program memory code protected 01 = Upper 3/4th of program memory code protected 00 = All memory is code protected 														
bit 7:	bit 7: MPEEN: Memory Parity Error Enable 1 = Memory Parity Checking is enabled 0 = Memory Parity Checking is disabled														
bit 6:	6: BODEN: Brown-out Reset Enable bit ⁽¹⁾ 1 = BOR enabled 0 = BOR disabled														
bit 3:	P 1 0	WRTE: = PWR = PWR	Powe T disa T enal	r-up Ti bled bled	mer Ei	nable bit	(1)								
bit 2:	W 1 0	DTE: V = WDT = WDT	Vatchd enabl disabl	log Tin ed led	ner En	able bit									
bit 1-(D: F(11 10 01 00	FOSC1:FOSC0: Oscillator Selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator													
Note	1: Er Er 2: Al	nabling nsure th I of the	Browr he Pov CP1:0	n-out R ver-up CP0 pa	teset a Timer airs har	utomatio is enable ve to be	cally enal ed anytin given the	oles Po ne Brov e same	wer-up wn-out value	o Timer (f Reset is to enable	PWRT) enable the co	regardle d. de prote	ess of the	value of bit l eme listed.	PWRTE.

Register	Power-on Reset, Brown-out Reset ⁽⁵⁾	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	XXXX XXXX	uuuu uuuu	นนนน นนนน
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	นนนน นนนน	นนนน นนนน
PCL	0000h	0000h	PC + 1 (2)
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	นนนน นนนน	นนนน นนนน
PORTA	x 0000	u 0000	u uuuu
PORTB	xxxx xxxx	<u>uuuu</u> uuuu	นนนน นนนน
PCLATH	0 0000	0 0000	u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu (1)
ADRES	XXXX XXXX	uuuu uuuu	นนนน นนนน
ADCON0	00-0 0000	00-0 0000	uu-u uuuu
OPTION	1111 1111	1111 1111	นนนน นนนน
TRISA	1 1111	1 1111	u uuuu
TRISB	1111 1111	1111 1111	นนนน นนนน
PCON ⁽⁴⁾	Ou		uu
ADCON1	00	00	uu

TABLE 8-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C710/71/711

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-10 for reset value for specific condition.

4: The PCON register is not implemented on the PIC16C71.

5: Brown-out reset is not implemented on the PIC16C71.

9.1 Instruction Descriptions

ADDLW	Add Lite	ral and \	N				
Syntax:	[<i>label</i>] Al	DDLW	k				
Operands:	$0 \le k \le 25$	55					
Operation:	(W) + k –	→ (W)					
Status Affected:	C, DC, Z						
Encoding:	11	111x	kkkk	kkkk			
Description:	The conter added to the result is pla	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.					
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read literal 'k'	Process data	Write to W			
Example:	ADDLW	0x15					
	Before In	struction					
	After Inst	W =	0x10				
		W =	0x25				
		a al f					
			£ -1				
Syntax:			f,d				
Operands:	$0 \le f \le 12$ $d \in [0,1]$.7					
Operation:	(W) + (f)	ightarrow (dest)					
Status Affected:	C, DC, Z						
Encoding:	00	0111	dfff	ffff			
Description:	Add the co with regist	ontents of er 'f'. If 'd' ne W regi	the W regi is 0 the re ster If 'd' is	ister sult is			

Encoding:	00	0111	dfff	ffff			
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write to Dest			
Example	ADDWF	FSR,	0				
	Before In	struction	1				
		W =	0x17				
		FSR =	0xC2				
	After Inst	ruction					
		VV =	UXD9				
		⊦SR =	0xC2				

ANDLW	AND Lite	eral with	w					
Syntax:	[<i>label</i>] ANDLW k							
Operands:	$0 \le k \le 255$							
Operation:	(W) .AND	D. (k) \rightarrow (W)					
Status Affected:	Z							
Encoding:	11	1001	kkkk	kkkk				
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read literal "k"	Process data	Write to W				
Example	ANDLW	0x5F						
	Before In	struction	0.10					
	After Inst	vv = ruction W =	0x03					

ANDWF	AND W with f						
Syntax:	[<i>label</i>] A	[<i>label</i>] ANDWF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1 \right] \end{array}$						
Operation:	(W) .AND. (f) \rightarrow (dest)						
Status Affected:	Z						
Encoding:	00	0101	dfff	ffff			
Description:	AND the V 'd' is 0 the register. If back in reg	V register result is s 'd' is 1 the gister 'f'.	with regist stored in th e result is s	ter 'f'. If ne W stored			
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write to Dest			
Example	ANDWF	FSR,	1				
	Before Instruction						
	W = 0x17						
	After Inst	ruction	0.02				
		W =	0x17				
		FSR =	0x02				

CLRF	Clear f						
Syntax:	[<i>label</i>] C	LRF f					
Operands:	$0 \le f \le 12$	27					
Operation:	$00h \rightarrow (f)$ 1 $\rightarrow Z$	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$					
Status Affected:	Z						
Encoding:	00	0001	lfff	ffff			
Description:	The contents of register 'f' are cleared and the Z bit is set.						
Words:	1						
Cycles:	1						
Q Cycle Activity:	Q1	Q2	Q3	Q4			
	Decode	Read register 'f'	Process data	Write register 'f'			
Example	CLRF	FLAG	G_REG				
	Before Instruction						
	After least	FLAG_RE	EG =	0x5A			
	AITELINST	FLAG RF	EG =	0x00			
		Ζ	=	1			

CLRW	Clear W			
Syntax:	[label]	CLRW		
Operands:	None			
Operation:	$00h \rightarrow (V)$	V)		
Status Affected	$1 \rightarrow Z$			
Encoding:		0001	0xxx	xxxx
Description:	W register	is cleare	d Zero bit	(7) is
Description.	set.	le cleare		(上) 10
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	NOP	Process data	Write to W
Example	CLRW			
Example	Before In	struction		
	Boloro III	W =	0x5A	
	After Inst	ruction	0.00	
		vv = Z =	0x00 1	
CLRWDT	Clear Wa	tchdog	Timer	
0 1			_	
Syntax:	[label]	CLRWD	I	
Syntax: Operands:	[<i>label</i>] None	CLRWD	I	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None 00h \rightarrow W	CLRWD DT	I	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$	CLRWD DT F presca	l ler,	
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$	CLRWD DT F presca	l ler,	
Syntax: Operands: Operation: Status Affected:	$\begin{bmatrix} label \\ \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD	CLRWD DT Γpresca	l ler,	
Syntax: Operands: Operation: Status Affected: Encoding:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow TO$ $1 \rightarrow PD$ TO, PD 00	CLRWD DT F presca	l er, 0110	0100
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \end{bmatrix}$ None $00h \rightarrow W$ $0 \rightarrow WDT$ $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$ $\overline{TO}, \overline{PD}$ $\boxed{00}$ CLRWDT in	CLRWD DT F presca	l ler, 0110 resets the	0100 Watch-
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ CLRWDT in dog Timer, of the WDT are set. \end{bmatrix}$	CLRWD DT F presca 0000 struction It also re T. Status I	0110 resets the provide TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer, of the WD \\ are set. \\ 1 \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I	0110 resets the poits TO and	0100 Watch- re <u>sca</u> ler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	$\begin{bmatrix} Iabel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \end{bmatrix}$	CLRWD DT F presca output struction It also re T. Status I	I 0110 resets the set <u>s</u> the pi bits TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set. 1\\ 1\\ 2\\ 1\\ Q1\\ \end{bmatrix}$	CLRWD DT presca 0000 Istruction It also re T. Status I	I 0110 resets the set <u>s the</u> pi bits TO and	0100 Watch- rescaler d PD
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline O0\\ \hline CLRWDT indog Timer,of the WDare set. 1\\ 1\\ Q1\\ \hline Decode\\ \end{bmatrix}$	CLRWD DT presca on on struction It also re T. Status I Q2 NOP	I 0110 resets the province of the province of the process Q3 Process	0100 Watch- rescaler d PD Q4 Clear
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WD are set. 11\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca 0000 Istruction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity:	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ CLRWDT indog Timer,of the WDare set. 1\\ 1\\ Q1\\ \hline Decode\\ \hline \end{bmatrix}$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	0110 resets the sets the provide TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline 00\\ \hline CLRWDT indog Timerof the WDare set.11Q1\\ \hline Decode\\ \hline CLRWDT\\ \end{bmatrix}$	CLRWD DT presca oooo struction It also re T. Status I Q2 NOP	0110 resets the sets the pi bits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Ooh \rightarrow W\\ O \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline OO\\ CLRWDT indog Timer,of the WDare set.11Q1DecodeCLRWDTBefore In$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP	I OIIO resets the sets the ploits TO and Q3 Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} abel \\ None \\ 00h \rightarrow W \\ 0 \rightarrow WD1 \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in \\ dog Timer \\ of the WD \\ are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou	I ler, 0110 resets the provide the providet the provide the providet the p	0100 Watch- rescaler d PD Q4 Clear WDT Counter
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W \\ 0 \rightarrow WDT \\ 1 \rightarrow TO \\ 1 \rightarrow PD \\ \hline TO, PD \\ \hline 00 \\ CLRWDT in dog Timer. of the WD are set. \\ 1 \\ 1 \\ Q1 \\ \hline Q1 \\ \hline CLRWDT \\ Before In \\ After Inst$	CLRWD DT presca 0000 struction It also re T. Status I Q2 NOP struction WDT cou ruction WDT cou	I OIIO resets the sets the province of the process data Process data	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Q Cycle Activity: Example	$\begin{bmatrix} Iabel \\ Oh \rightarrow W\\ 0 \rightarrow WDT\\ 1 \rightarrow TO\\ 1 \rightarrow PD\\ \hline TO, PD\\ \hline O0\\ CLRWDT indog Timer,of the WDare set.11Q1CLRWDTBefore InAfter Inst$	CLRWD DT presca r presca struction It also re T. Status I Q2 NOP struction WDT cou WDT cou WDT cou WDT cou	I ler, 0110 resets the provide the providet the	0100 Watch- rescaler d PD Q4 Clear WDT Counter ? 0x00 0

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FIGURE 11-3: CLKOUT AND I/O TIMING



TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
	T 110 11							
10*	TosH2ckL	OSC1 ^T to CLKOUT↓			15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time			5	15	ns	Note 1
14*	TckL2ioV	CLKOUT \downarrow to Port out valid	b		_	0.5Tcy + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOL	JT ↑	0.25Tcy + 25	—	—	ns	Note 1
16*	TckH2iol	Port in hold after CLKOUT ↑		0	_	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to		—	—	80 - 100	ns	
		Port out valid						
18*	TosH2iol	OSC1 [↑] (Q2 cycle) to		TBD	—	—	ns	
		Port input invalid (I/O in ho	ld time)					
19*	TioV2osH	Port input valid to OSC11	(I/O in setup time)	TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16 C 710/711		10	25	ns	
			PIC16LC710/711	—	—	60	ns	
21*	TioF	Port output fall time	PIC16 C 710/711	—	10	25	ns	
			PIC16LC710/711	—	—	60	ns	
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high	or low time	20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

tt These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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13.5 <u>Timing Diagrams and Specifications</u>

FIGURE 13-2: EXTERNAL CLOCK TIMING



TABLE 13-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fos	External CI KIN Frequency	DC		4	MHZ	XTosc mode
	100	(Note 1)		_	4		HS osc mode (PIC16C715-04)
			DC	_	20	MHZ	HS osc mode (PIC16C715-20)
			DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
		(Note 1)	0.1		<u> </u>	MHz	XT osc mode
			4	$ \langle \rangle$	4	MHz	HS osc mode (PIC16C715-04)
			4	$\wedge - \land$	10	MHz	HS osc mode (PIC16C715-10)
			<u>4</u>	\mathbb{A}	20	MHz	HS osc mode (PIC16C715-20)
		<	B	<u>II</u>	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	$\left \right\rangle \rightarrow \left $	—	ns	XT osc mode
		(Note 1)	250	\searrow	-	ns	HS osc mode (PIC16C715-04)
			100		-	ns	HS osc mode (PIC16C715-10)
			\$0	-	-	ns	HS osc mode (PIC16C715-20)
			> 5	—		μs	LP osc mode
		Oscillator Períod	250	_	_	ns	RC osc mode
			250	-	10,000	ns	XT osc mode
			250	-	250	ns	HS osc mode (PIC16C715-04)
			100	_	250	ns	HS osc mode (PIC16C715-10)
		$r > - \sqrt{r}$	50	_	250	ns	HS osc mode (PIC16C715-20)
		\land	5	_	_	μs	LP osc mode
2 /	Ter	Instruction Cycle Time (Note 1)	200	—	DC	ns	TCY = 4/FOSC
3	TosĻ,	External Clock in (OSC1) High	50	_	—	ns	XT oscillator
$ \setminus \setminus$	TosH	or Low Time	2.5	—	—	μs	LP oscillator
	\leq		10	—		ns	HS oscillator
4	TosR,	External Clock in (OSC1) Rise	_	_	25	ns	XT oscillator
	TósF	or Fall Time	-	-	50	ns	LP oscillator
			—	_	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C715.

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15.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial)

DC CH	ARACTERISTICS		Standa Operat	ard Op ing terr	eratin perati	g Cond ure 0° -4	litions (unless otherwise stated) $^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $^{\circ}O^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)
Param No.	Characteristic	Sym	Min	Тур†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5		6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	Vdr	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	Vss	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	1.8	3.3	mA	XT, RC osc configuration Fosc = 4 MHz, VDD = 5.5V (Note 4)
D013			-	13.5	30	mA	HS osc configuration Fosc = 20 MHz, VDD = 5.5V
D020 D021 D021A	Power-down Current (Note 3)	IPD	- - -	7 1.0 1.0	28 14 16	μΑ μΑ μΑ	$VDD = 4.0V, WDT enabled, -40^{\circ}C to +85^{\circ}C$ $VDD = 4.0V, WDT disabled, -0^{\circ}C to +70^{\circ}C$ $VDD = 4.0V, WDT disabled, -40^{\circ}C to +85^{\circ}C$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD $\overline{MCLR} = VDD$; WDT enabled/disabled as specified.

The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm. Applicable Devices 710 71 711 715

FIGURE 15-6: A/D CONVERSION TIMING



TABLE 15-7: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions
130	TAD	A/D clock period	PIC16 C 71	2.0	_	_	μs	Tosc based, VREF ≥ 3.0V
			PIC16 LC 71	2.0	_		μs	TOSC based, VREF full range
			PIC16 C 71	2.0	4.0	6.0	μs	A/D RC Mode
			PIC16 LC 71	3.0	6.0	9.0	μs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time)	(Note 1)	_	9.5	_	TAD	
132	TACQ	Acquisition time		Note 2	20		μs	
				5*	_	_	μs	The minimum time is the ampli- fier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start		_	Tosc/2§	_	_	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	Tswc	Switching from convert -	\rightarrow sample time	1.5§	—		TAD	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ These specifications ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 7.1 for min conditions.

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FIGURE 16-22: IOL VS. VOL, VDD = 5V



APPENDIX A:

The following are the list of modifications over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (1K now as opposed to 512 before) and register file (68 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. Bits PA2, PA1, PA0 are removed from STATUS register.
- 3. Data memory paging is redefined slightly. STATUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out although they are kept for compati-bility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. Reset vector is changed to 0000h.
- Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt on change feature.
- 13. T0CKI pin is also a port pin (RA4) now.
- 14. FSR is made a full eight bit register.
- "In-circuit serial programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, Vss, MCLR/VPP, RB6 (clock) and RB7 (data in/out).
- PCON status register is added with a Power-on Reset status bit (POR).
- 17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
- Brown-out protection circuitry has been added. Controlled by configuration word bit BODEN. Brown-out reset ensures the device is placed in a reset condition if VDD dips below a fixed setpoint.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- 1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change reset vector to 0000h.

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