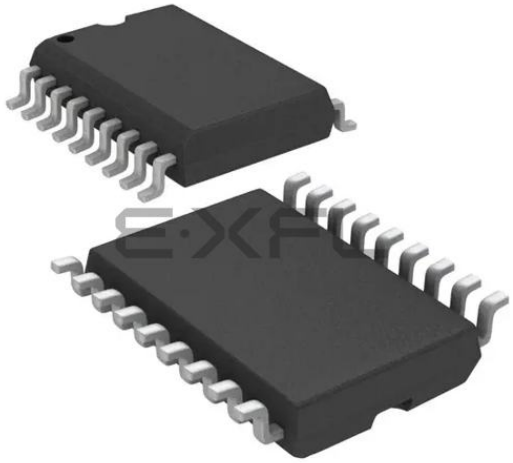

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, PWM, WDT |
| Number of I/O | 13 |
| Program Memory Size | 896B (512 x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 36 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 6V |
| Data Converters | A/D 4x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 18-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 18-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04e-so |

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture, in which, program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The table below lists program memory (EPROM) and data memory (RAM) for each PIC16C71X device.

| Device | Program Memory | Data Memory |
|---|---|---|
| PIC16C710 | 512 x 14 | 36 x 8 |
| PIC16C71 | 1K x 14 | 36 x 8 |
| PIC16C711 | 1K x 14 | 68 x 8 |
| PIC16C715 | 2K x 14 | 128 x 8 |

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC16CXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ bit and a $\overline{\text{digit}}$ $\overline{\text{borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

## 4.2 Data Memory Organization

The data memory is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bit RP0 is the bank select bit.

RP0 (STATUS<5>) = 1 → Bank 1

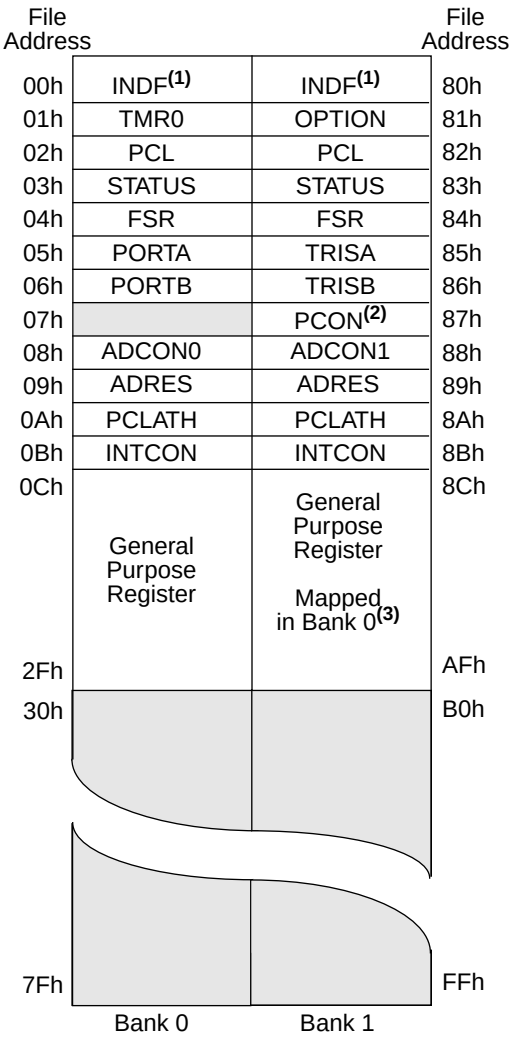
RP0 (STATUS<5>) = 0 → Bank 0

Each Bank extends up to 7Fh (128 bytes). The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. Both Bank 0 and Bank 1 contain special function registers. Some "high use" special function registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

### 4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

**FIGURE 4-4: PIC16C710/71 REGISTER FILE MAP**




Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: The PCON register is not implemented on the PIC16C71.

3: These locations are unimplemented in Bank 1. Any access to these locations will access the corresponding Bank 0 register.

**FIGURE 4-5: PIC16C711 REGISTER FILE MAP**

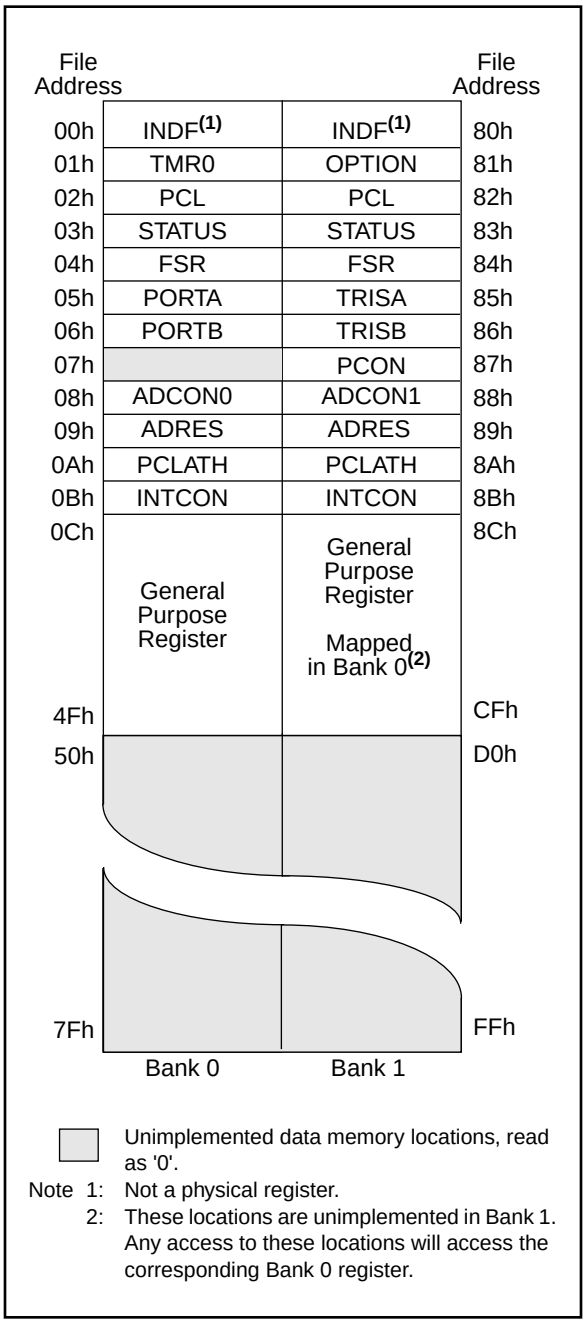
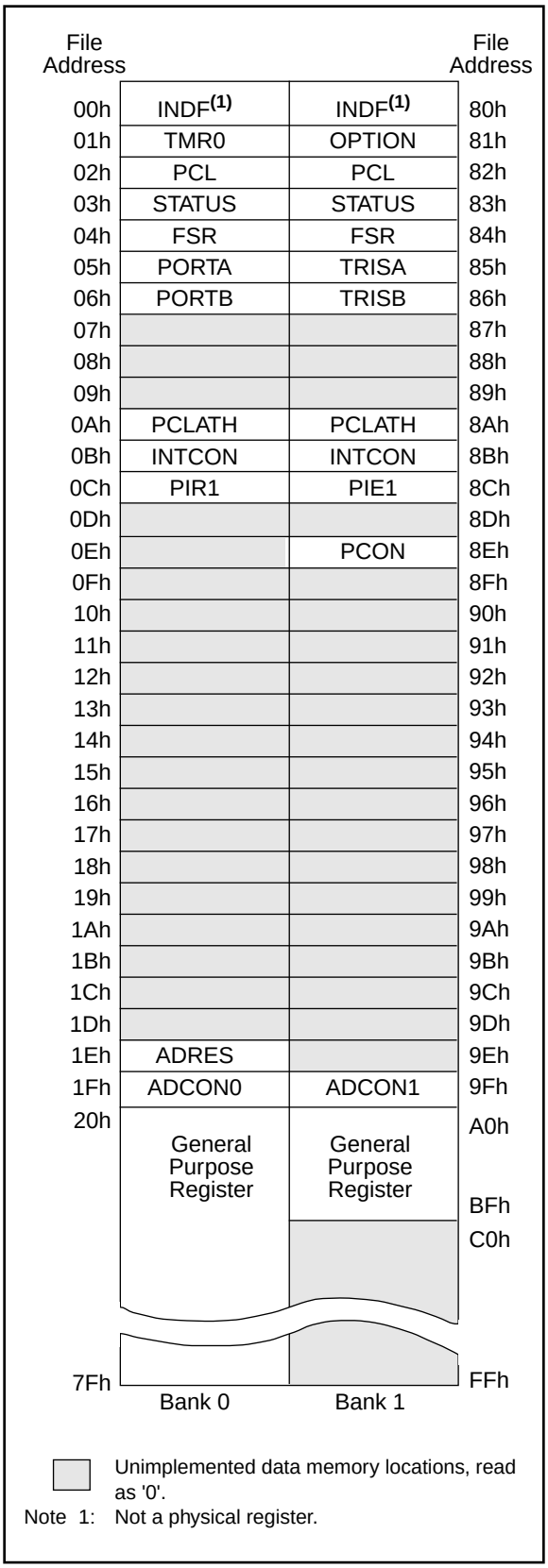



**FIGURE 4-6: PIC16C715 REGISTER FILE MAP**



4.2.2.2 OPTION REGISTER

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

**Note:** To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

**FIGURE 4-8: OPTION REGISTER (ADDRESS 81h, 181h)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6: **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0: **PS2:PS0:** Prescaler Rate Select bits

| Bit Value | TMR0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

4.2.2.3 INTCON REGISTER

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

**Note:** Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

**FIGURE 4-9: INTCON REGISTER (ADDRESS 0Bh, 8Bh)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-x |
|---|---|---|---|---|---|---|---|
| GIE | ADIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:**(1) Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

bit 6: **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables A/D interrupt
0 = Disables A/D interrupt

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1: **INTF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note 1: For the PIC16C71, if an interrupt occurs while the GIE bit is being cleared, the GIE bit may be unintentionally re-enabled by the RETFIE instruction in the user's Interrupt Service Routine. Refer to Section 8.5 for a detailed description.

Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**FIGURE 8-2: CONFIGURATION WORD, PIC16C710/711**

| CP0 | CP0 | CP0 | CP0 | CP0 | CP0 | CP0 | BODEN | CP0 | CP0 | $\overline{\text{PWRTE}}$ | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| bit13 | | | | | | | | | | | | | bit0 |

Register: CONFIG
Address 2007h

bit 13-7 **CP0:** Code protection bits (2)
5-4: 1 = Code protection off
0 = All memory is code protected, but 00h - 3Fh is writable

bit 6: **BODEN:** Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3: **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit (1)
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP0 bits have to be given the same value to enable the code protection scheme listed.

**FIGURE 8-3: CONFIGURATION WORD, PIC16C715**

| CP1 | CP0 | CP1 | CP0 | CP1 | CP0 | MPEEN | BODEN | CP1 | CP0 | $\overline{\text{PWRTE}}$ | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| bit13 | | | | | | | | | | | | | bit0 |

Register: CONFIG
Address 2007h

bit 13-8 **CP1:CP0:** Code Protection bits (2)
5-4: 11 = Code protection off
10 = Upper half of program memory code protected
01 = Upper 3/4th of program memory code protected
00 = All memory is code protected

bit 7: **MPEEN:** Memory Parity Error Enable
1 = Memory Parity Checking is enabled
0 = Memory Parity Checking is disabled

bit 6: **BODEN:** Brown-out Reset Enable bit (1)
1 = BOR enabled
0 = BOR disabled

bit 3: **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit (1)
1 = PWRT disabled
0 = PWRT enabled

bit 2: **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.
2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

**TABLE 8-12: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C710/71/711**

| Register | Power-on Reset, Brown-out Reset(5) | $\overline{\text{MCLR}}$ Resets WDT Reset | Wake-up via WDT or Interrupt |
|---|---|---|---|
| W | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | N/A | N/A | N/A |
| TMR0 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 0000h | 0000h | PC + 1(2) |
| STATUS | 0001 1xxx | 000q quuu(3) | uuuq quuu(3) |
| FSR | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA | ---x 0000 | ---u 0000 | ---u uuuu |
| PORTB | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCLATH | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0000 000x | 0000 000u | uuuu uuuu(1) |
| ADRES | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON0 | 00-0 0000 | 00-0 0000 | uu-u uuuu |
| OPTION | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISA | ---1 1111 | ---1 1111 | ---u uuuu |
| TRISB | 1111 1111 | 1111 1111 | uuuu uuuu |
| PCON(4) | ---- --0u | ---- --uu | ---- --uu |
| ADCON1 | ---- --00 | ---- --00 | ---- --uu |

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-10 for reset value for specific condition.

4: The PCON register is not implemented on the PIC16C71.

5: Brown-out reset is not implemented on the PIC16C71.

## 9.1 Instruction Descriptions

**ADDLW** **Add Literal and W**

Syntax: [*label*] ADDLW k

Operands: $0 \le k \le 255$

Operation: (W) + k → (W)

Status Affected: C, DC, Z

Encoding:

| | | | |
|---|---|---|---|
| 11 | 111x | kkkk | kkkk |

Description: The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal 'k' | Process data | Write to W |

Example:
```
ADDLW   0x15
```
Before Instruction
W = 0x10
After Instruction
W = 0x25

**ANDLW** **AND Literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W) .AND. (k) → (W)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 11 | 1001 | kkkk | kkkk |

Description: The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read literal "k" | Process data | Write to W |

Example
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

**ADDWF** **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 0111 | dfff | ffff |

Description: Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to Dest |

Example
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

**ANDWF** **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

| | | | |
|---|---|---|---|
| 00 | 0101 | dfff | ffff |

Description: AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write to Dest |

Example
```
ANDWF   FSR, 1
```
Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

**CLRF** **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \le f \le 127$

Operation: 00h → (f)
1 → Z

Status Affected: Z

Encoding:

| 00 | 0001 | 1fff | ffff |
|---|---|---|---|

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process data | Write register 'f' |

Example
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

**CLRW** **Clear W**

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

| 00 | 0001 | 0xxx | xxxx |
|---|---|---|---|

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | Process data | Write to W |

Example
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

**CLRWDT** **Clear Watchdog Timer**

Syntax: [ *label* ] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 00 | 0000 | 0110 | 0100 |
|---|---|---|---|

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

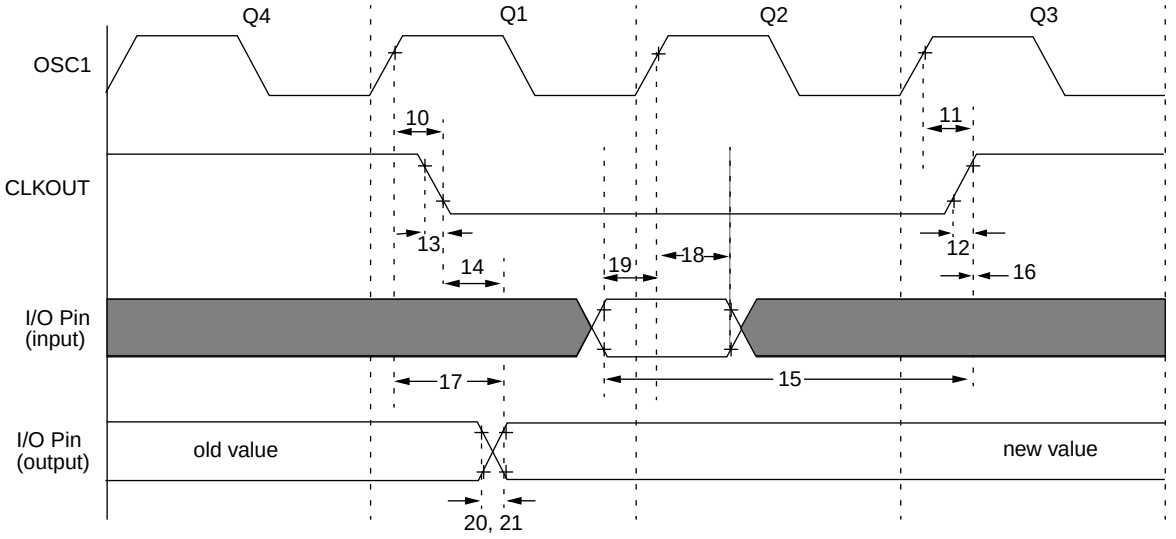
Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | NOP | Process data | Clear WDT Counter |

Example
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 11-3: CLKOUT AND I/O TIMING**




Note: Refer to Figure 11-1 for load conditions.

**TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS**

| Parameter No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | | — | 15 | 30 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | | — | 15 | 30 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | | — | 5 | 15 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | | — | 5 | 15 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | | 0.25TCY + 25 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | | — | — | 80 - 100 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | | TBD | — | — | ns | |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | | TBD | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16**C**710/711 | — | 10 | 25 | ns | |
| | | | PIC16**LC**710/711 | — | — | 60 | ns | |
| 21* | TioF | Port output fall time | PIC16**C**710/711 | — | 10 | 25 | ns | |
| | | | PIC16**LC**710/711 | — | — | 60 | ns | |
| 22††* | Tinp | INT pin high or low time | | 20 | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change INT high or low time | | 20 | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

## 13.5 Timing Diagrams and Specifications

**FIGURE 13-2: EXTERNAL CLOCK TIMING**

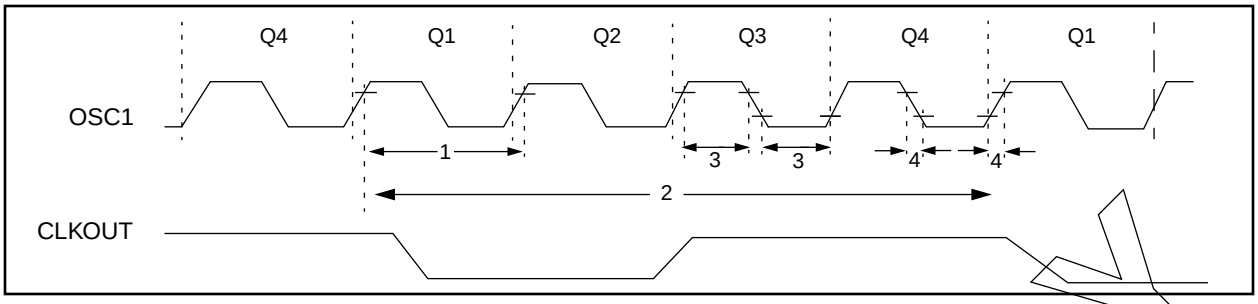



**TABLE 13-2: CLOCK TIMING REQUIREMENTS**

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Fos | **External CLKIN Frequency (Note 1)** | DC | — | 4 | MHz | XT osc mode |
| | | | DC | — | 4 | MHz | HS osc mode (PIC16C715-04) |
| | | | DC | — | 20 | MHz | HS osc mode (PIC16C715-20) |
| | | | DC | — | 200 | kHz | LP osc mode |
| | | **Oscillator Frequency (Note 1)** | DC | — | 4 | MHz | RC osc mode |
| | | | 0.1 | — | 4 | MHz | XT osc mode |
| | | | 4 | — | 4 | MHz | HS osc mode (PIC16C715-04) |
| | | | 4 | — | 10 | MHz | HS osc mode (PIC16C715-10) |
| | | | 4 | — | 20 | MHz | HS osc mode (PIC16C715-20) |
| | | | 5 | — | 200 | kHz | LP osc mode |
| 1 | Tosc | **External CLKIN Period (Note 1)** | 250 | — | — | ns | XT osc mode |
| | | | 250 | — | — | ns | HS osc mode (PIC16C715-04) |
| | | | 100 | — | — | ns | HS osc mode (PIC16C715-10) |
| | | | 50 | — | — | ns | HS osc mode (PIC16C715-20) |
| | | | 5 | — | — | µs | LP osc mode |
| | | **Oscillator Period (Note 1)** | 250 | — | — | ns | RC osc mode |
| | | | 250 | — | 10,000 | ns | XT osc mode |
| | | | 250 | — | 250 | ns | HS osc mode (PIC16C715-04) |
| | | | 100 | — | 250 | ns | HS osc mode (PIC16C715-10) |
| | | | 50 | — | 250 | ns | HS osc mode (PIC16C715-20) |
| | | | 5 | — | — | µs | LP osc mode |
| 2 | TCY | **Instruction Cycle Time (Note 1)** | 200 | — | DC | ns | TCY = 4/FOSC |
| 3 | TosL, TosH | **External Clock in (OSC1) High or Low Time** | 50 | — | — | ns | XT oscillator |
| | | | 2.5 | — | — | µs | LP oscillator |
| | | | 10 | — | — | ns | HS oscillator |
| 4 | TosR, TosF | **External Clock in (OSC1) Rise or Fall Time** | — | — | 25 | ns | XT oscillator |
| | | | — | — | 50 | ns | LP oscillator |
| | | | — | — | 15 | ns | HS oscillator |

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC16C715.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 14-29: TYPICAL IDD vs. FREQUENCY (HS MODE, 25°C)**

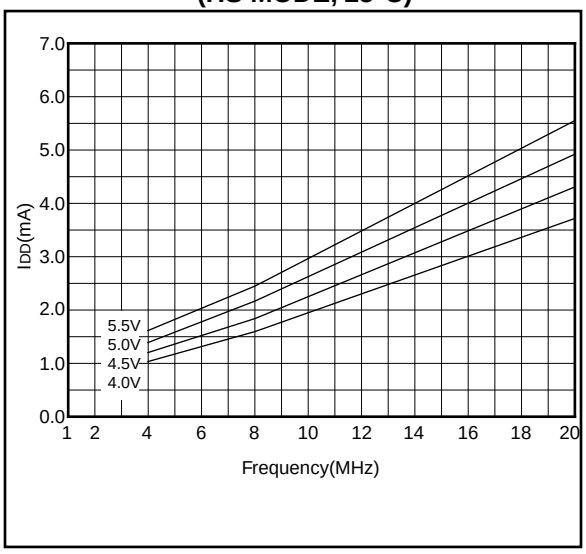
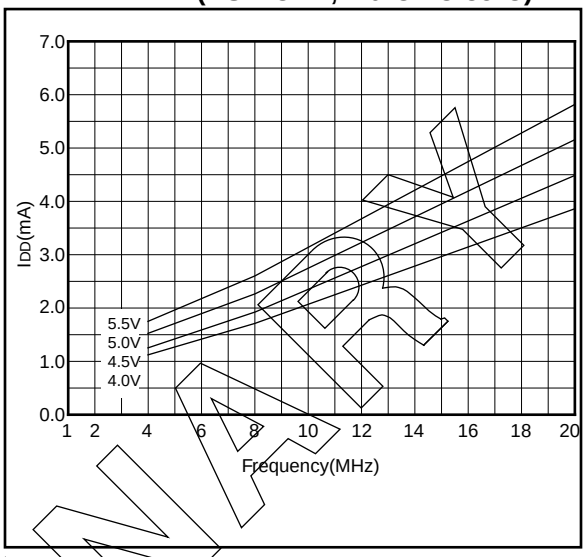



**FIGURE 14-30: MAXIMUM IDD vs. FREQUENCY (HS MODE, -40°C TO 85°C)**



| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

### 15.1 DC Characteristics: PIC16C71-04 (Commercial, Industrial) PIC16C71-20 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C (commercial)<br>-40°C ≤ TA ≤ +85°C (industrial) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Sym** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001<br>D001A | Supply Voltage | VDD | 4.0<br>4.5 | -<br>- | 6.0<br>5.5 | V<br>V | XT, RC and LP osc configuration<br>HS osc configuration |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D010<br><br><br>D013 | Supply Current (Note 2) | IDD | -<br><br><br>- | 1.8<br><br><br>13.5 | 3.3<br><br><br>30 | mA<br><br><br>mA | XT, RC osc configuration<br>FOSC = 4 MHz, VDD = 5.5V (Note 4)<br><br>HS osc configuration<br>FOSC = 20 MHz, VDD = 5.5V |
| D020<br>D021<br>D021A | Power-down Current (Note 3) | IPD | -<br>-<br>- | 7<br>1.0<br>1.0 | 28<br>14<br>16 | µA<br>µA<br>µA | VDD = 4.0V, WDT enabled, -40°C to +85°C<br>VDD = 4.0V, WDT disabled, -0°C to +70°C<br>VDD = 4.0V, WDT disabled, -40°C to +85°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

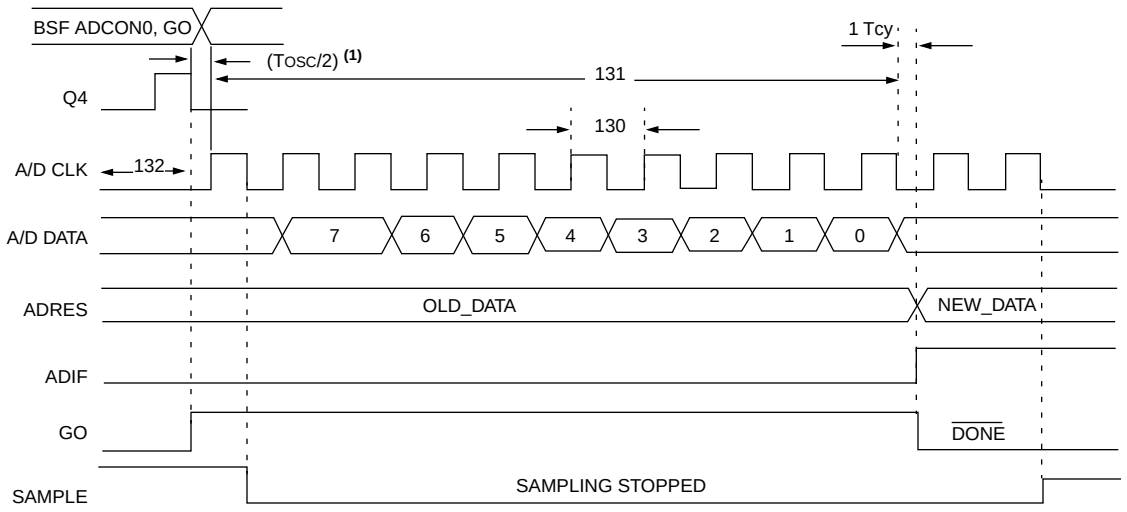
2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 15-6: A/D CONVERSION TIMING**




Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

**TABLE 15-7: A/D CONVERSION REQUIREMENTS**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 130 | TAD | A/D clock period | PIC16**C**71 | 2.0 | — | — | µs | TOSC based, VREF ≥ 3.0V |
| | | | PIC16**LC**71 | 2.0 | — | — | µs | TOSC based, VREF full range |
| | | | PIC16**C**71 | 2.0 | 4.0 | 6.0 | µs | A/D RC Mode |
| | | | PIC16**LC**71 | 3.0 | 6.0 | 9.0 | µs | A/D RC Mode |
| 131 | TCNV | Conversion time (not including S/H time) (Note 1) | | — | 9.5 | — | TAD | |
| 132 | TACQ | Acquisition time | | Note 2 | 20 | — | µs | |
| | | | | 5* | — | — | µs | The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD). |
| 134 | TGO | Q4 to A/D clock start | | — | Tosc/2§ | — | — | If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed. |
| 135 | TSWC | Switching from convert → sample time | | 1.5§ | — | — | TAD | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ These specifications ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 7.1 for min conditions.

| Applicable Devices | 710 | 71 | 711 | 715 |
|---|---|---|---|---|

**FIGURE 16-21: IOL VS. VOL, VDD = 3V**

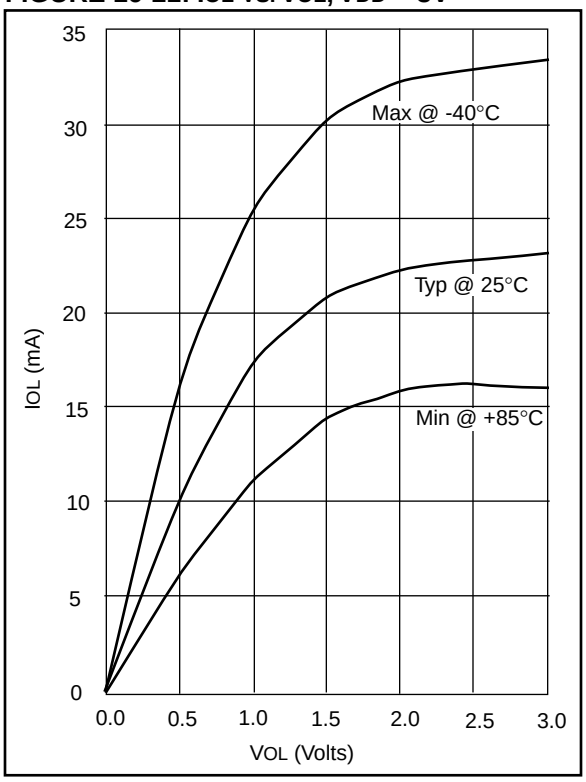
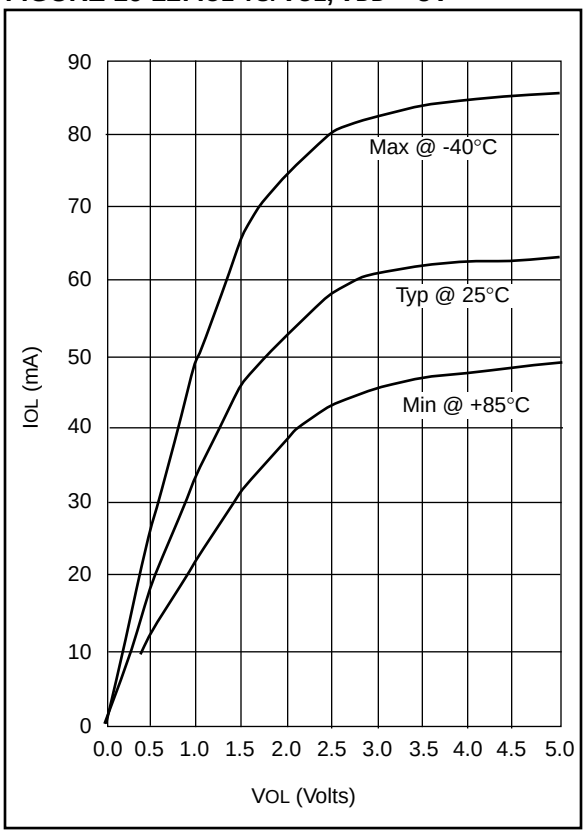



**FIGURE 16-22: IOL VS. VOL, VDD = 5V**




Data based on matrix samples. See first page of this section for details.

## APPENDIX A:

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14-bits. This allows larger page sizes both in program memory (1K now as opposed to 512 before) and register file (68 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. Bits PA2, PA1, PA0 are removed from STATUS register.
3. Data memory paging is redefined slightly. STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change feature.
13. T0CKI pin is also a port pin (RA4) now.
14. FSR is made a full eight bit register.
15. "In-circuit serial programming" is made possible. The user can program PIC16CXX devices using only five pins: $V_{DD}$, $V_{SS}$, $\overline{MCLR}/V_{PP}$, RB6 (clock) and RB7 (data in/out).
16. PCON status register is added with a Power-on Reset status bit ($\overline{POR}$).
17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
18. Brown-out protection circuitry has been added. Controlled by configuration word bit BODEN. Brown-out reset ensures the device is placed in a reset condition if $V_{DD}$ dips below a fixed setpoint.

## APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

## LIST OF TABLES

**NOTES:**