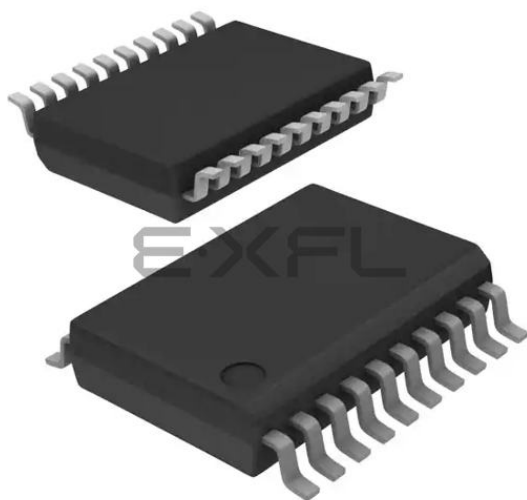




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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04e-ss

PIC16C71X

TABLE 1-1: PIC16C71X FAMILY OF DEVICES

		PIC16C710	PIC16C71	PIC16C711	PIC16C715	PIC16C72	PIC16CR72 ⁽¹⁾
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20
	EPROM Program Memory (x14 words)	512	1K	1K	2K	2K	—
Memory	ROM Program Memory (14K words)	—	—	—	—	—	2K
	Data Memory (bytes)	36	36	68	128	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
	Capture/Compare/PWM Module(s)	—	—	—	—	1	1
	Serial Port(s) (SPI/I ² C, USART)	—	—	—	—	SPI/I ² C	SPI/I ² C
	Parallel Slave Port	—	—	—	—	—	—
	A/D Converter (8-bit) Channels	4	4	4	4	5	5
Features	Interrupt Sources	4	4	4	4	8	8
	I/O Pins	13	13	13	13	22	22
	Voltage Range (Volts)	2.5-6.0	3.0-6.0	2.5-6.0	2.5-5.5	2.5-6.0	3.0-5.5
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	—	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC, 20-pin SSOP	18-pin DIP, SOIC, 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC, SSOP

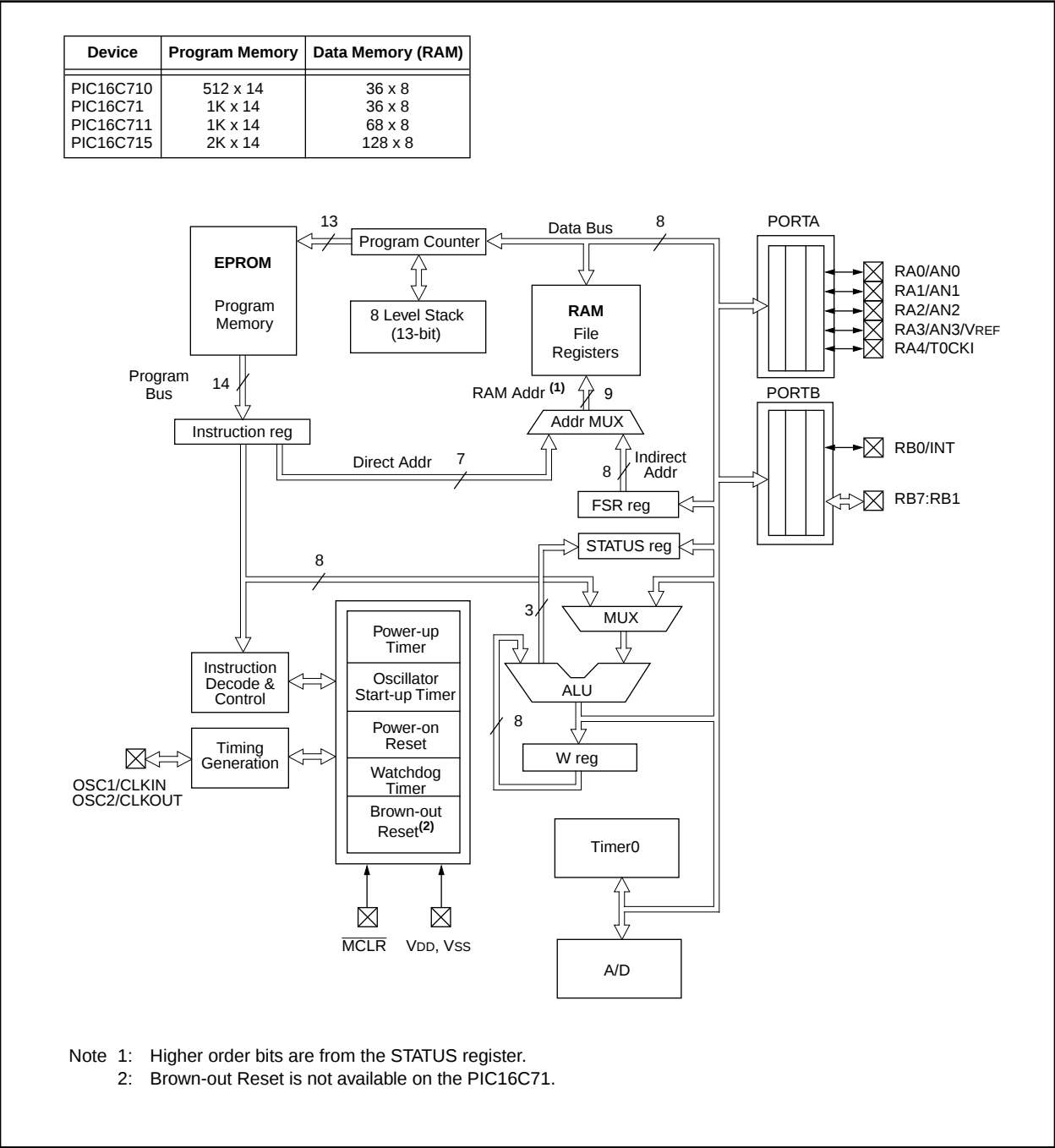
		PIC16C73A	PIC16C74A	PIC16C76	PIC16C77
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
	EPROM Program Memory (x14 words)	4K	4K	8K	8K
Memory	Data Memory (bytes)	192	192	376	376
	Timer Module(s)	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2	TMR0, TMR1, TMR2
Peripherals	Capture/Compare/PWM Module(s)	2	2	2	2
	Serial Port(s) (SPI/I ² C, USART)	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART	SPI/I ² C, USART
	Parallel Slave Port	—	Yes	—	Yes
	A/D Converter (8-bit) Channels	5	8	5	8
	Interrupt Sources	11	12	11	12
Features	I/O Pins	22	33	22	33
	Voltage Range (Volts)	2.5-6.0	2.5-6.0	2.5-6.0	2.5-6.0
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	Yes	Yes	Yes
	Packages	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP	28-pin SDIP, SOIC	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C7XX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip sales office for availability of these devices.

PIC16C71X

FIGURE 3-1: PIC16C71X BLOCK DIAGRAM



4.0 MEMORY ORGANIZATION

4.1 Program Memory Organization

The PIC16C71X family has a 13-bit program counter capable of addressing an 8K x 14 program memory space. The amount of program memory available to each device is listed below:

Device	Program Memory	Address Range
PIC16C710	512 x 14	0000h-01FFh
PIC16C71	1K x 14	0000h-03FFh
PIC16C711	1K x 14	0000h-03FFh
PIC16C715	2K x 14	0000h-07FFh

For those devices with less than 8K program memory, accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC16C710 PROGRAM MEMORY MAP AND STACK

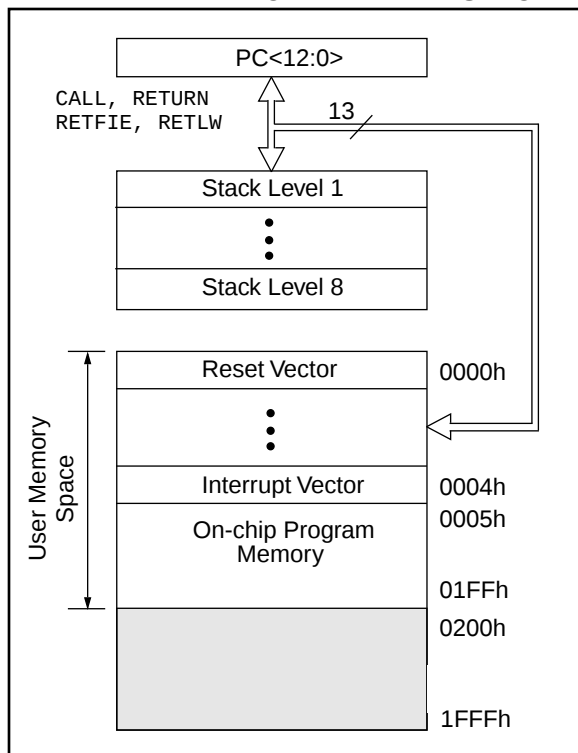


FIGURE 4-2: PIC16C71/711 PROGRAM MEMORY MAP AND STACK

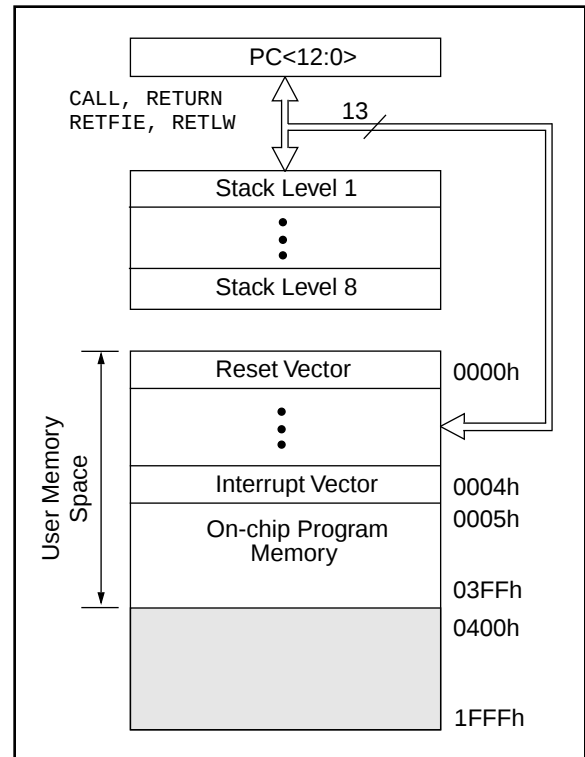
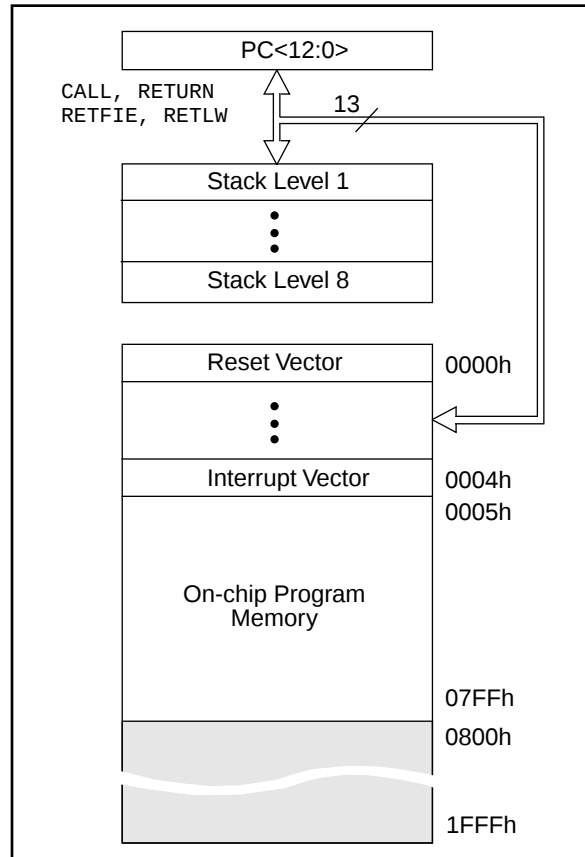


FIGURE 4-3: PIC16C715 PROGRAM MEMORY MAP AND STACK



PIC16C71X

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). Those registers associated with the “core” functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: PIC16C710/71/711 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (1)
Bank 0											
00h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h ⁽³⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h ⁽³⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h ⁽³⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	PORTA Data Latch when written: PORTA pins when read					- - - x 0000	- - - u 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	—	Unimplemented								—	—
08h	ADCON0	ADCS1	ADCS0	(6)	CHS1	CHS0	GO/DONE	ADIF	ADON	00-0 0000	00-0 0000
09h ⁽³⁾	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
0Ah ^(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					- - - 0 0000	- - - 0 0000
0Bh ⁽³⁾	INTCON	GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h ⁽³⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽³⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h ⁽³⁾	STATUS	IRP ⁽⁵⁾	RP1 ⁽⁵⁾	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h ⁽³⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA Data Direction Register					- - - 1 1111	- - - 1 1111
86h	TRISB	PORTB Data Direction Control Register								1111 1111	1111 1111
87h ⁽⁴⁾	PCON	—	—	—	—	—	—	POR	$\overline{BOR}$	- - - - - qq	- - - - - uu
88h	ADCON1	—	—	—	—	—	—	PCFG1	PCFG0	- - - - - 00	- - - - - 00
89h ⁽³⁾	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
8Ah ^(2,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					- - - 0 0000	- - - 0 0000
8Bh ⁽³⁾	INTCON	GIE	ADIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: Other (non power-up) resets include external reset through $\overline{MCLR}$ and Watchdog Timer Reset.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: These registers can be addressed from either bank.

4: The PCON register is not physically implemented in the PIC16C71, read as '0'.

5: The IRP and RP1 bits are reserved on the PIC16C710/71/711, always maintain these bits clear.

6: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

Applicable Devices 710 71 711 715

The analog-to-digital (A/D) converter module has four analog inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 7-1 and Figure 7-2, controls the operation of the A/D module. The ADCON1 register, shown in Figure 7-3 configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

FIGURE 7-1: ADCON0 REGISTER (ADDRESS 08h), PIC16C710/71/711

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	— (1)	CHS1	CHS0	GO/DONE	ADIF	ADON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from an RC oscillation)

bit 5: **Unimplemented:** Read as '0'.

bit 4-3: **CHS1:CHS0:** Analog Channel Select bits
00 = channel 0, (RA0/AN0)
01 = channel 1, (RA1/AN1)
10 = channel 2, (RA2/AN2)
11 = channel 3, (RA3/AN3)

bit 2: **GO/DONE:** A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **ADIF:** A/D Conversion Complete Interrupt Flag bit
1 = conversion is complete (must be cleared in software)
0 = conversion is not complete

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Note 1: Bit5 of ADCON0 is a General Purpose R/W bit for the PIC16C710/711 only. For the PIC16C71, this bit is unimplemented, read as '0'.

PIC16C71X

TABLE 8-13: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C715

Register	Power-on Reset, Brown-out Reset Parity Error Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	---x 0000	---u 0000	---u uuuu
PORTB	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
PIR1	-0-- ----	-0-- ----	-u-- ---- ⁽¹⁾
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION	1111 1111	1111 1111	uuuu uuuu
TRISA	---1 1111	---1 1111	---u uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-0-- ----	-0-- ----	-u-- ----
PCON	---- -qqq	---- -1uu	---- -1uu
ADCON1	---- --00	---- --00	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

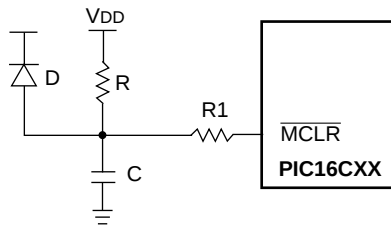
Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-11 for reset value for specific condition.

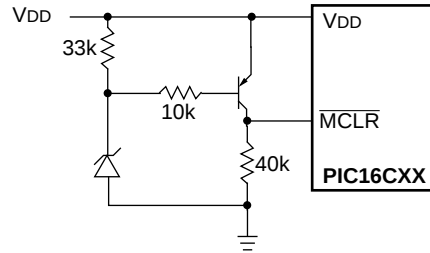
PIC16C71X

FIGURE 8-14: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



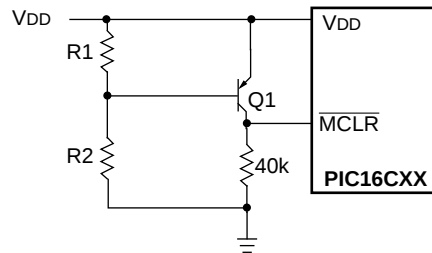
- Note 1: External Power-on Reset circuit is required only if V_{DD} power-up slope is too slow. The diode D helps discharge the capacitor quickly when V_{DD} powers down.
- 2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
- 3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR/V_{PP} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 8-15: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate reset when V_{DD} goes below (V_Z + 0.7V) where V_Z = Zener voltage.
- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 8-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



- Note 1: This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

- 2: Internal brown-out detection on the PIC16C710/711/715 should be disabled when using this circuit.
- 3: Resistors should be adjusted for the characteristics of the transistor.

COMF		Complement f						
Syntax:	[<i>label</i>] COMF f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	$(\bar{f}) \rightarrow (\text{dest})$							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>00</td><td>1001</td><td>dfff</td><td>ffff</td></tr></table>				00	1001	dfff	ffff
00	1001	dfff	ffff					
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to dest				

Example COMF REG1, 0

Before Instruction
 REG1 = 0x13

After Instruction
 REG1 = 0x13
 W = 0xEC

DECf		Decrement f						
Syntax:	[label] DECf f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	(f) - 1 $\rightarrow$ (dest)							
Status Affected:	Z							
Encoding:	<table><tr><td>00</td><td>0011</td><td>dfff</td><td>ffff</td></tr></table>				00	0011	dfff	ffff
00	0011	dfff	ffff					
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process data	Write to dest				

Example DECf CNT, 1

Before Instruction
 CNT = 0x01
 Z = 0

After Instruction
 CNT = 0x00
 Z = 1

DECFSZ		Decrement f, Skip if 0										
Syntax:	[<i>label</i>] DECFSZ f,d											
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$											
Operation:	$(f) - 1 \rightarrow (\text{dest}); \quad \text{skip if result} = 0$											
Status Affected:	None											
Encoding:	<table><tr><td>00</td><td>1011</td><td>dfff</td><td>ffff</td></tr></table>				00	1011	dfff	ffff				
00	1011	dfff	ffff									
Description:	The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 1, the next instruction, is executed. If the result is 0, then a NOP is executed instead making it a 2Tcy instruction.											
Words:	1											
Cycles:	1(2)											
Q Cycle Activity:	<table><tr><th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process data</td><td>Write to dest</td></tr></table>				Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process data	Write to dest
Q1	Q2	Q3	Q4									
Decode	Read register 'f'	Process data	Write to dest									
If Skip:	(2nd Cycle)											
	<table><tr><th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr><tr><td>NOP</td><td>NOP</td><td>NOP</td><td>NOP</td></tr></table>				Q1	Q2	Q3	Q4	NOP	NOP	NOP	NOP
Q1	Q2	Q3	Q4									
NOP	NOP	NOP	NOP									

Example HERE DECFSZ CNT, 1
 GOTO LOOP

CONTINUE •
 •
 •

Before Instruction
 PC = address HERE

After Instruction
 CNT = CNT - 1
 if CNT = 0,
 PC = address CONTINUE
 if CNT $\neq$ 0,
 PC = address HERE+1

Applicable Devices	710	71	711	715
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FIGURE 12-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

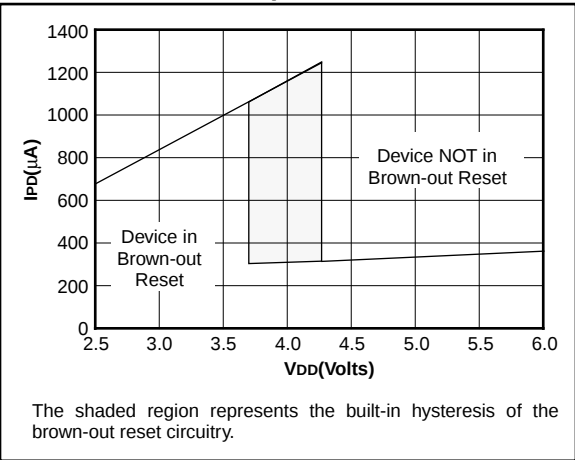


FIGURE 12-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

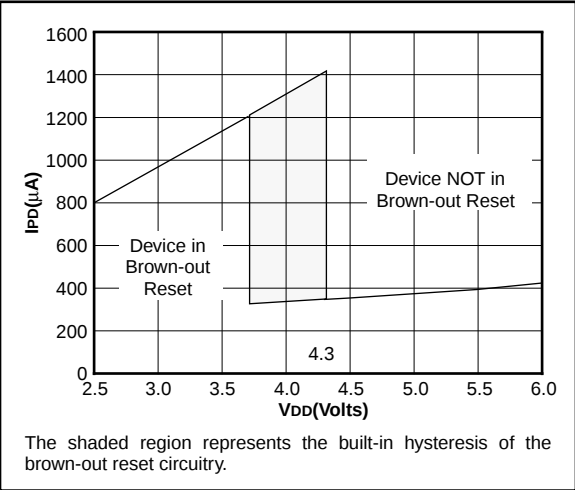


FIGURE 12-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

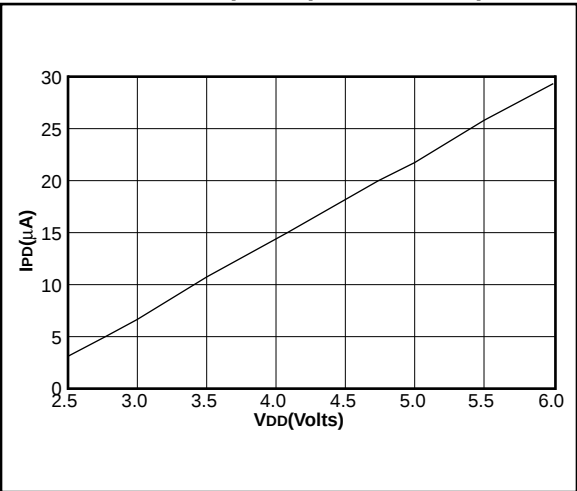


FIGURE 12-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

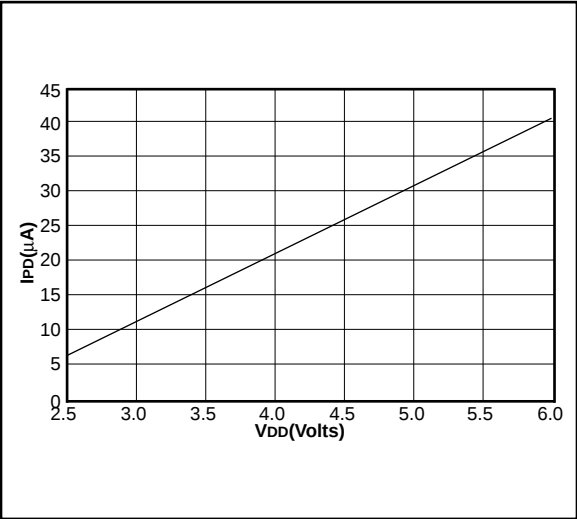


FIGURE 14-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

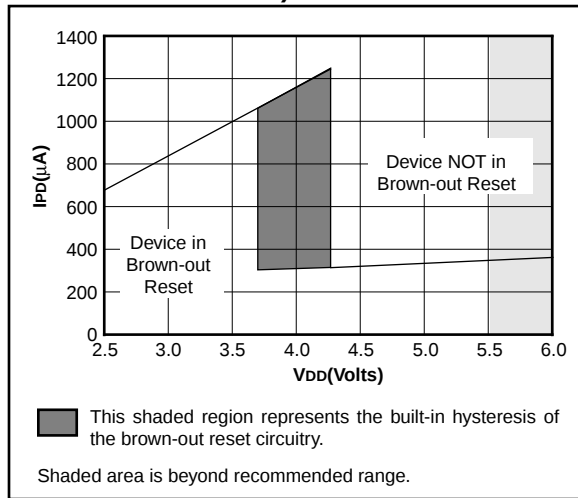


FIGURE 14-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

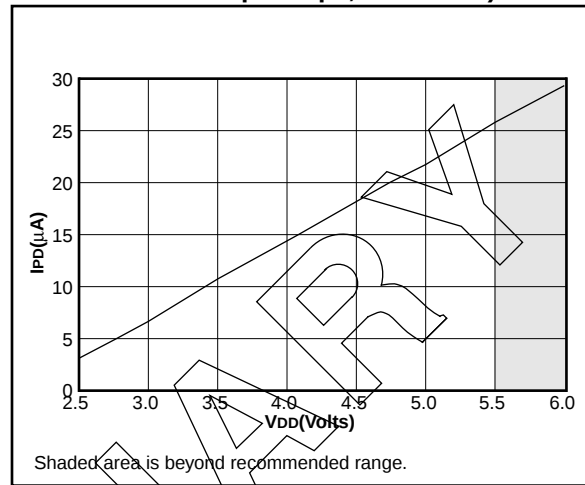


FIGURE 14-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

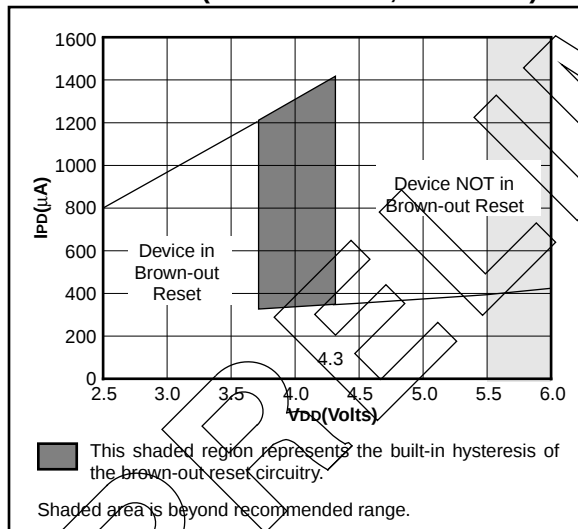


FIGURE 14-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)

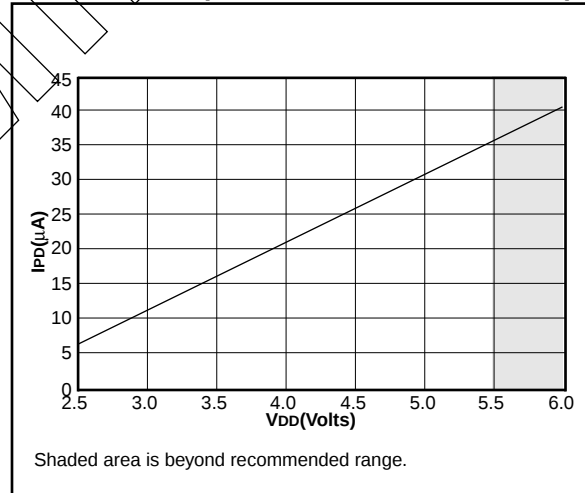


FIGURE 14-18: TYPICAL I_{DD} vs. CAPACITANCE @ 500 kHz (RC MODE)

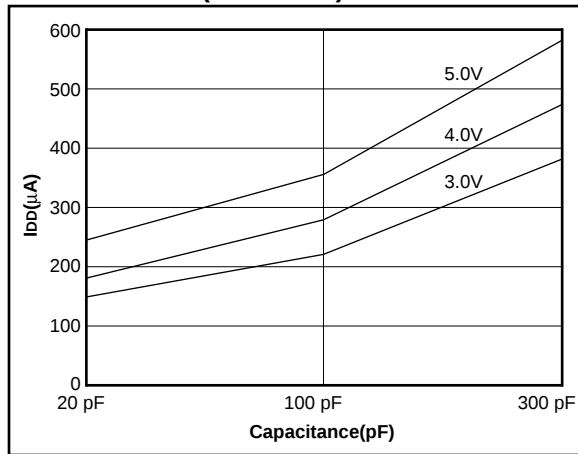


TABLE 14-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average	
		Fosc @ 5V, 25°C	
22 pF	5k	4.12 MHz	± 1.4%
	10k	2.35 MHz	± 1.4%
	100k	268 kHz	± 1.1%
100 pF	3.3k	1.80 MHz	± 1.0%
	5k	1.27 MHz	± 1.0%
	10k	688 kHz	± 1.2%
	100k	77.2 kHz	± 1.0%
300 pF	3.3k	707 kHz	± 1.4%
	5k	501 kHz	± 1.2%
	10k	269 kHz	± 1.6%
	100k	28.3 kHz	± 1.1%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for $V_{DD} = 5V$.

FIGURE 14-19: TRANSCONDUCTANCE(gm) OF HS OSCILLATOR vs. V_{DD}

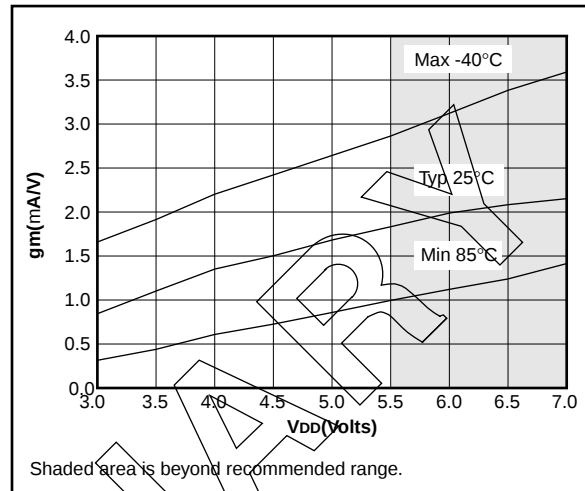


FIGURE 14-20: TRANSCONDUCTANCE(gm) OF LP OSCILLATOR vs. V_{DD}

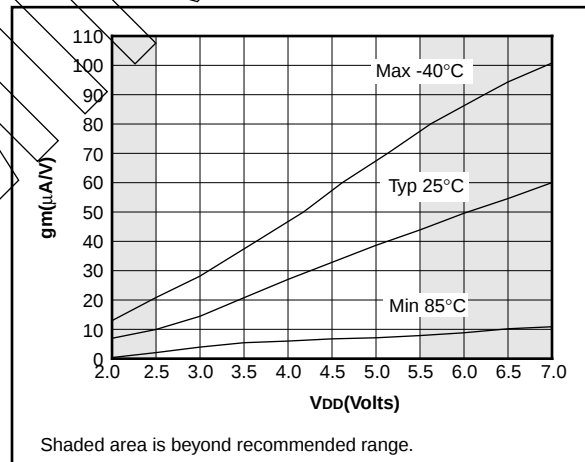
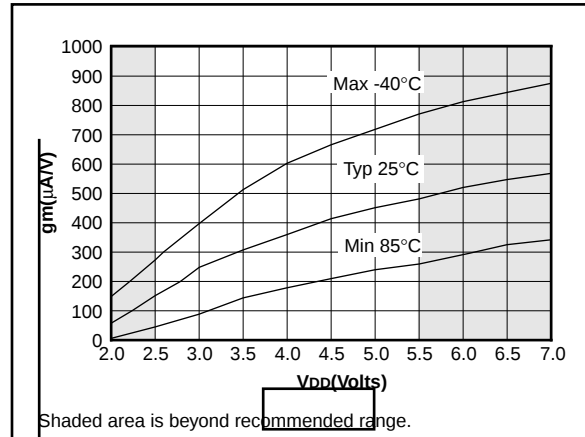


FIGURE 14-21: TRANSCONDUCTANCE(gm) OF XT OSCILLATOR vs. V_{DD}



PIC16C71X

Applicable Devices	710	71	711	715
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DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
		Operating voltage V_{DD} range as described in DC spec Section 15.1 and Section 15.2.					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D100	Capacitive Loading Specs on Output Pins						
	OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2 (in RC mode)	CIO			50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

- The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- Negative current is defined as current sourced by the pin.
- PIC16C71 Rev. "Ax" INT pin has a TTL input buffer. PIC16C71 Rev. "Bx" INT pin has a Schmitt Trigger input buffer.

PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 15-3: CLKOUT AND I/O TIMING

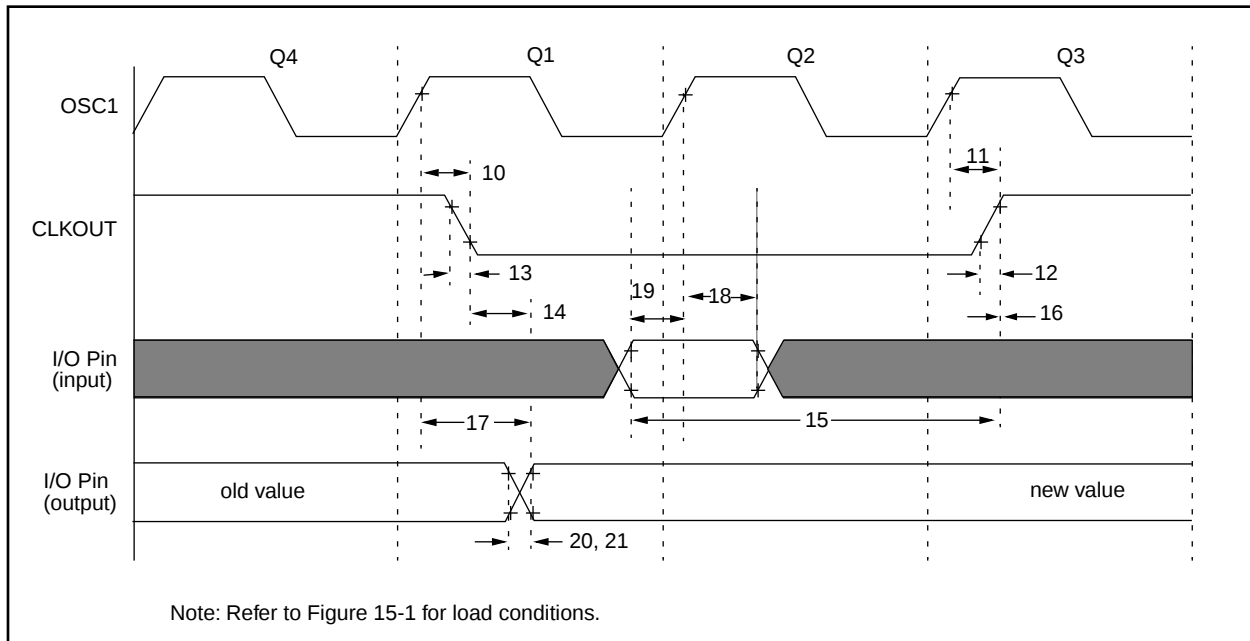


TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5T _{cy} + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	0.25T _{cy} + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16C71	100	—	ns	
			PIC16LC71	200	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	PIC16C71	—	10	ns	
			PIC16LC71	—	—	60	ns
21*	TioF	Port output fall time	PIC16C71	—	10	ns	
			PIC16LC71	—	—	60	ns
22††*	Tinp	INT pin high or low time	20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time	20	—	—	ns	

* These parameters are characterized but not tested.

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x T_{osc}.

TABLE 15-6: A/D CONVERTER CHARACTERISTICS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	8 bits	bits	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
A02	EABS	Absolute error	PIC16C71	—	$< \pm 1$	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
			PIC16LC71	—	$< \pm 2$	LSb	$V_{REF} = V_{DD} = 3.0V$ (Note 3)
A03	EIL	Integral linearity error	PIC16C71	—	$< \pm 1$	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
			PIC16LC71	—	$< \pm 2$	LSb	$V_{REF} = V_{DD} = 3.0V$ (Note 3)
A04	EDL	Differential linearity error	PIC16C71	—	$< \pm 1$	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
			PIC16LC71	—	$< \pm 2$	LSb	$V_{REF} = V_{DD} = 3.0V$ (Note 3)
A05	EFS	Full scale error	PIC16C71	—	$< \pm 1$	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
			PIC16LC71	—	$< \pm 2$	LSb	$V_{REF} = V_{DD} = 3.0V$ (Note 3)
A06	EOFF	Offset error	PIC16C71	—	$< \pm 1$	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq V_{AIN} \leq V_{REF}$
			PIC16LC71	—	$< \pm 2$	LSb	$V_{REF} = V_{DD} = 3.0V$ (Note 3)
A10	—	Monotonicity	—	guaranteed	—	—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	VREF	Reference voltage	3.0V	—	$V_{DD} + 0.3$	V	
A25	VAIN	Analog input voltage	$V_{SS} - 0.3$	—	VREF	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	k Ω	
A40	IAD	A/D conversion current (V_{DD})	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)	PIC16C71	10	—	1000	μA During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1.
				—	—	40	μA During A/D Conversion cycle
			PIC16LC71	—	—	1	mA During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD see Section 7.1.
				—	—	10	μA During A/D Conversion cycle

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

3: These specifications apply if $V_{REF} = 3.0V$ and if $V_{DD} \geq 3.0V$. V_{AIN} must be between V_{SS} and V_{REF} .

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES FOR PIC16C71

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

Note: The data presented in this section is a statistical summary of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

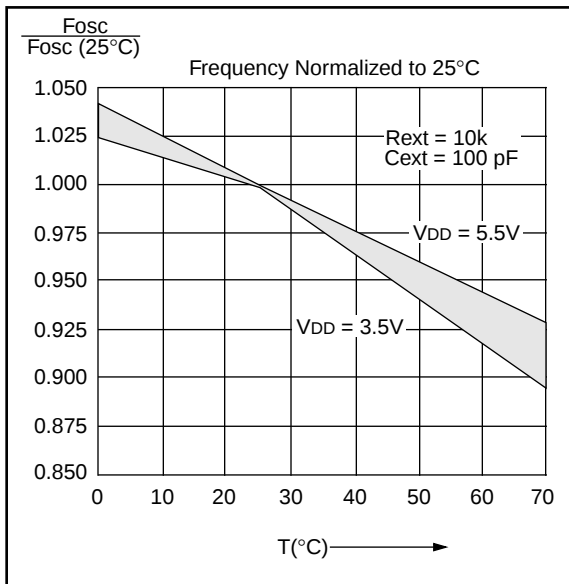


FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}

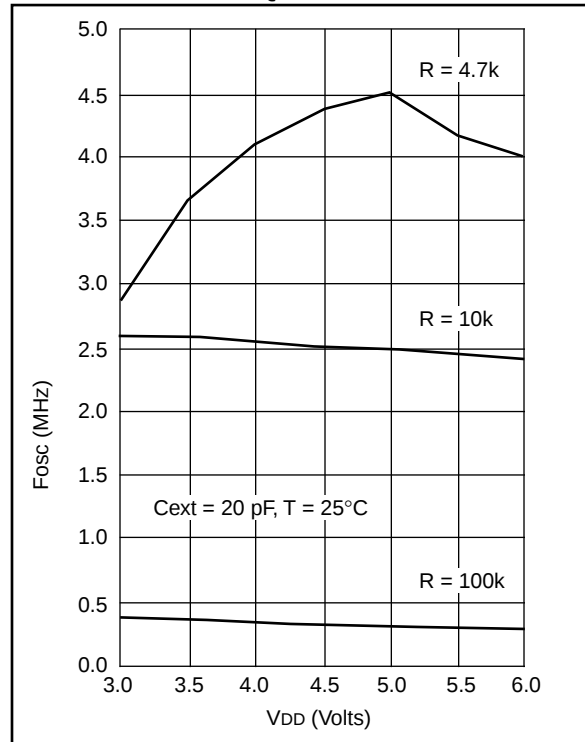
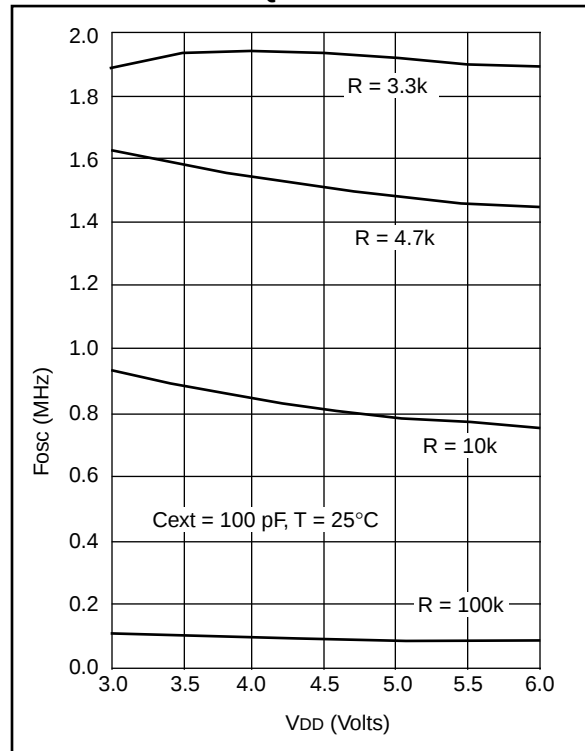


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}



PIC16C71X

Applicable Devices 710 71 711 715

FIGURE 16-4: TYPICAL RC OSCILLATOR
FREQUENCY vs. VDD

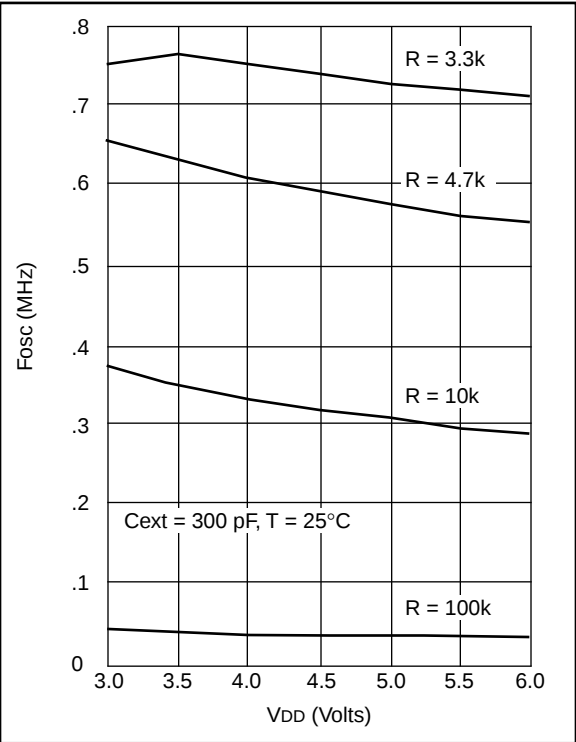


FIGURE 16-5: TYPICAL IPD vs. VDD
WATCHDOG TIMER
DISABLED 25°C

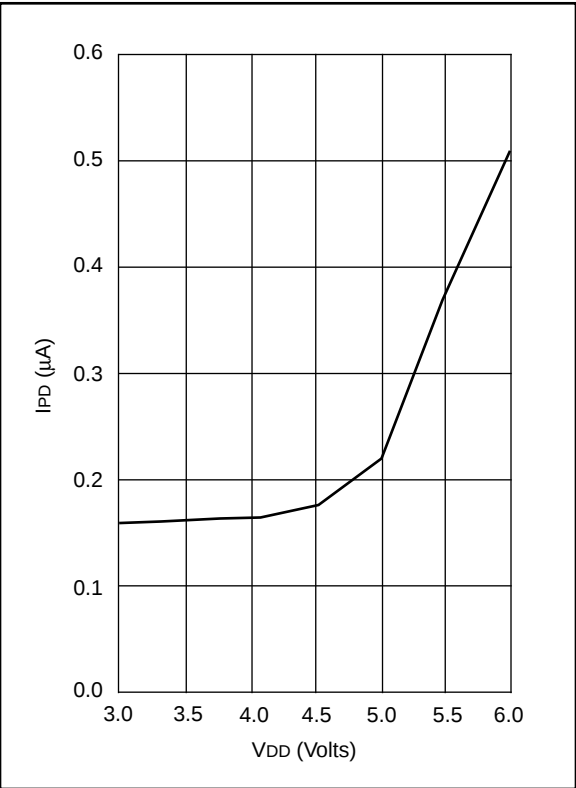
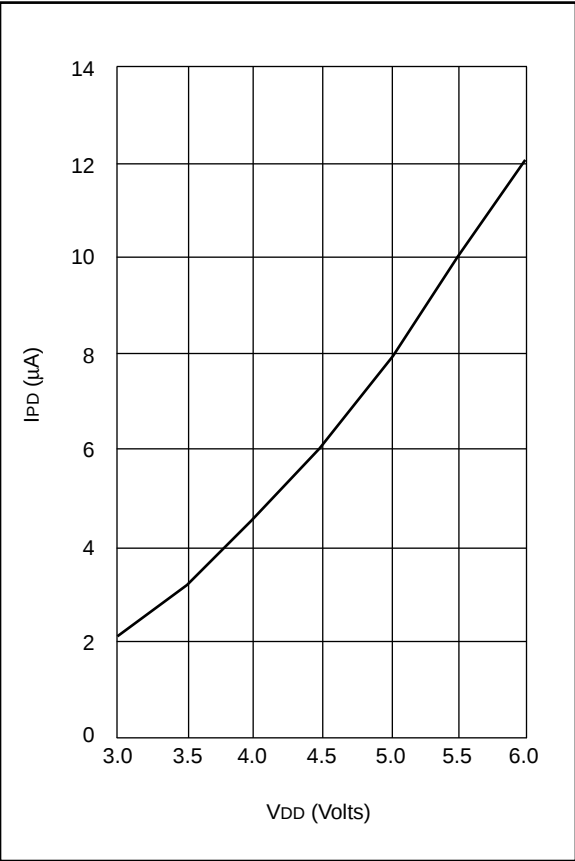


TABLE 16-1: RC OSCILLATOR
FREQUENCIES

Cext	Rext	Average	
		Fosc @ 5V, 25°C	
20 pF	4.7k	4.52 MHz	±17.35%
	10k	2.47 MHz	±10.10%
	100k	290.86 kHz	±11.90%
100 pF	3.3k	1.92 MHz	±9.43%
	4.7k	1.49 MHz	±9.83%
	10k	788.77 kHz	±10.92%
	100k	88.11 kHz	±16.03%
300 pF	3.3k	726.89 kHz	±10.97%
	4.7k	573.95 kHz	±10.14%
	10k	307.31 kHz	±10.43%
	100k	33.82 kHz	±11.24%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

FIGURE 16-6: TYPICAL IPD vs. VDD
WATCHDOG TIMER ENABLED
25°C



Data based on matrix samples. See first page of this section for details.

PIC16C71X

NOTES:

PIC16C71X

$\overline{TO}$ bit	17
TOSE bit	18
TRISA Register	14, 16, 25
TRISB Register	14, 16, 27
Two's Complement	7

U

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W

W Register	
ALU	7
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Z

Z bit	17
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