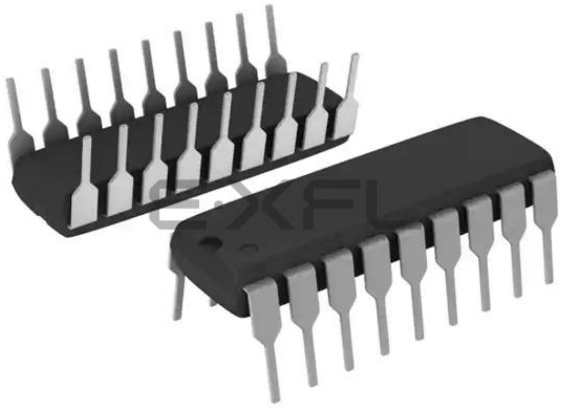


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc710-04i-p

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 PIC16C71X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C71X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For the PIC16C71X family, there are two device “types” as indicated in the device number:

1. **C**, as in PIC16**C**71. These devices have EPROM type memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**71. These devices have EPROM type memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the oscillator modes.

Microchip's PICSTART® Plus and PRO MATE® II programmers both support programming of the PIC16C71X.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround Production (SQTP℠) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

7.4 A/D Conversions

Example 7-2 shows how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (V_{REF}) is the device V_{DD}. The A/D interrupt is enabled, and the A/D conversion clock is F_{RC}. The conversion is performed on the RA0 pin (channel 0).

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a $2T_{AD}$ wait is required before the next acquisition is started. After this $2T_{AD}$ wait, an acquisition is automatically started on the selected channel.

EXAMPLE 7-2: A/D CONVERSION

```
     BSF      STATUS, RP0         ; Select Bank 1
     CLRF     ADCON1              ; Configure A/D inputs
     BCF      STATUS, RP0         ; Select Bank 0
     MOVLW    0xC1                ; RC Clock, A/D is on, Channel 0 is selected
     MOVWF    ADCON0              ;
     BSF      INTCON, ADIE        ; Enable A/D Interrupt
     BSF      INTCON, GIE         ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input channel has elapsed.
;  Then the conversion may be started.
;
     BSF      ADCON0, GO          ; Start A/D Conversion
       :                          ; The ADIF bit will be set and the GO/DONE bit
       :                          ;  is cleared upon completion of the A/D Conversion.
```

7.4.1 FASTER CONVERSION - LOWER RESOLUTION TRADE-OFF

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the T_{AD} time violates the minimum specified time (see the applicable electrical specification). Once the T_{AD} time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$
Where: N = number of bits of resolution required.

Since the T_{AD} is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 7-3 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 20 MHz and 16 MHz (The A/D clock is programmed for $32T_{OSC}$), and assumes that immediately after $6T_{AD}$, the A/D clock is programmed for $2T_{OSC}$.

The $2T_{OSC}$ violates the minimum T_{AD} time since the last 4-bits will not be converted to correct values.

EXAMPLE 7-3: 4-BIT vs. 8-BIT CONVERSION TIMES

	Freq. (MHz)(1)	Resolution	
		4-bit	8-bit
T_{AD}	20	1.6 µs	1.6 µs
	16	2.0 µs	2.0 µs
T_{OSC}	20	50 ns	50 ns
	16	62.5 ns	62.5 ns
$2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$	20	10 µs	16 µs
	16	12.5 µs	20 µs

Note 1: The PIC16C71 has a minimum T_{AD} time of 2.0 µs.
All other PIC16C71X devices have a minimum T_{AD} time of 1.6 µs.

8.4.5 TIME-OUT SEQUENCE

Applicable Devices	710	71	711	715

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 8-11, Figure 8-12, and Figure 8-13 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 8-12). This is useful for testing purposes or to synchronize more than one PIC16CXX device operating in parallel.

Table 8-10 and Table 8-11 show the reset conditions for some special function registers, while Table 8-12 and Table 8-13 show the reset conditions for all the registers.

8.4.6 POWER CONTROL/STATUS REGISTER (PCON)

Applicable Devices	710	71	711	715

The Power Control/Status Register, PCON has up to two bits, depending upon the device.

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred. The $\overline{\text{BOR}}$ bit is a "Don’t Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

For the PIC16C715, bit2 is $\overline{\text{PER}}$ (Parity Error Reset). It is cleared on a Parity Error Reset and must be set by user software. It will also be set on a Power-on Reset.

For the PIC16C715, bit7 is MPEEN (Memory Parity Error Enable). This bit reflects the status of the MPEEN bit in configuration word. It is unaffected by any reset of interrupt.

8.4.7 PARITY ERROR RESET (PER)

Applicable Devices	710	71	711	715

The PIC16C715 has on-chip parity bits that can be used to verify the contents of program memory. Parity bits may be useful in applications in order to increase overall reliability of a system.

There are two parity bits for each word of Program Memory. The parity bits are computed on alternating bits of the program word. One computation is performed using even parity, the other using odd parity. As a program executes, the parity is verified. The even parity bit is XOR’d with the even bits in the program memory word. The odd parity bit is negated and XOR’d with the odd bits in the program memory word. When an error is detected, a reset is generated and the $\overline{\text{PER}}$ flag bit 2 in the PCON register is cleared (logic ‘0’). This indication can allow software to act on a failure. However, there is no indication of the program memory location of the failure in Program Memory. This flag can only be set (logic ‘1’) by software.

The parity array is user selectable during programming. Bit 7 of the configuration word located at address 2007h can be programmed (read as ‘0’) to disable parity. If left unprogrammed (read as ‘1’), parity is enabled.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS, PIC16C71

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024 TOSC
RC	72 ms	—	—

TABLE 8-6: TIME-OUT IN VARIOUS SITUATIONS, PIC16C710/711/715

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	—	72 ms	—

TABLE 8-13: INITIALIZATION CONDITIONS FOR ALL REGISTERS, PIC16C715

Register	Power-on Reset, Brown-out Reset Parity Error Reset	$\overline{\text{MCLR}}$ Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1(2)
STATUS	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	---x 0000	---u 0000	---u uuuu
PORTB	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	-0-- ----	-0-- ----	-u-- ----(1)
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION	1111 1111	1111 1111	uuuu uuuu
TRISA	---1 1111	---1 1111	---u uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-0-- ----	-0-- ----	-u-- ----
PCON	---- -qqq	---- -1uu	---- -1uu
ADCON1	---- --00	---- --00	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 8-11 for reset value for specific condition.

9.1 Instruction Descriptions

ADDLW — Add Literal and W

Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k $\rightarrow$ (W)
Status Affected:	C, DC, Z
Encoding:	`11` `111x` `kkkk` `kkkk`
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process data	Write to W

Example: `ADDLW 0x15`

Before Instruction
W = 0x10
After Instruction
W = 0x25

ADDWF — Add W and f

Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) $\rightarrow$ (dest)
Status Affected:	C, DC, Z
Encoding:	`00` `0111` `dfff` `ffff`
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to Dest

Example `ADDWF FSR, 0`

Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0xD9
FSR = 0xC2

ANDLW — AND Literal with W

Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) $\rightarrow$ (W)
Status Affected:	Z
Encoding:	`11` `1001` `kkkk` `kkkk`
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal "k"	Process data	Write to W

Example `ANDLW 0x5F`

Before Instruction
W = 0xA3
After Instruction
W = 0x03

ANDWF — AND W with f

Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) $\rightarrow$ (dest)
Status Affected:	Z
Encoding:	`00` `0101` `dfff` `ffff`
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process data	Write to Dest

Example `ANDWF FSR, 1`

Before Instruction
W = 0x17
FSR = 0xC2
After Instruction
W = 0x17
FSR = 0x02

NOP	No Operation			
Syntax:	[*label*] NOP			
Operands:	None			
Operation:	No operation			
Status Affected:	None			
Encoding:	00	0000	0xx0	0000
Description:	No operation.			
Words:	1			
Cycles:	1			
Q Cycle Activity:	Q1	Q2	Q3	Q4
	Decode	NOP	NOP	NOP
Example	`NOP`			

OPTION	Load Option Register			
Syntax:	[*label*] OPTION			
Operands:	None			
Operation:	(W) → OPTION			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.			
Words:	1			
Cycles:	1			
Example	**To maintain upward compatibility with future PIC16CXX products, do not use this instruction.**			

RETFIE	Return from Interrupt			
Syntax:	[*label*] RETFIE			
Operands:	None			
Operation:	TOS → PC, 1 → GIE			
Status Affected:	None			
Encoding:	00	0000	0000	1001
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.			
Words:	1			
Cycles:	2			
Q Cycle Activity:	Q1	Q2	Q3	Q4
1st Cycle	Decode	NOP	Set the GIE bit	Pop from the Stack
2nd Cycle	NOP	NOP	NOP	NOP
Example	`RETFIE`			

After Interrupt
PC = TOS
GIE = 1

10.0 DEVELOPMENT SUPPORT

10.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH®–MP)

10.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

10.3 ICEPIC: Low-Cost PIC16CXXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

10.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

Applicable Devices	710	71	711	715

11.2 DC Characteristics: PIC16LC710-04 (Commercial, Industrial, Extended) PIC16LC711-04 (Commercial, Industrial, Extended)

DC CHARACTERISTICS							**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0˚C ≤ TA ≤ +70˚C (commercial) -40˚C ≤ TA ≤ +85˚C (industrial) -40˚C ≤ TA ≤ +125˚C (extended)
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage Commercial/Industrial Extended	 VDD VDD	 2.5 3.0	 - -	 6.0 6.0	 V V	 LP, XT, RC osc configuration (DC - 4 MHz) LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	-	-	V/ms	See section on Power-on Reset for details
D005	Brown-out Reset Voltage	BVDD	3.7	4.0	4.3	V	BODEN configuration bit is enabled
D010	Supply Current (Note 2)	IDD	-	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			-	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D015	Brown-out Reset Current (Note 5)	∆IBOR	-	300*	500	µA	BOR enabled VDD = 5.0V
D020	Power-down Current (Note 3)	IPD	-	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021			-	0.9	5	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A			-	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D021B			-	0.9	10	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C
D023	Brown-out Reset Current (Note 5)	∆IBOR	-	300*	500	µA	BOR enabled VDD = 5.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

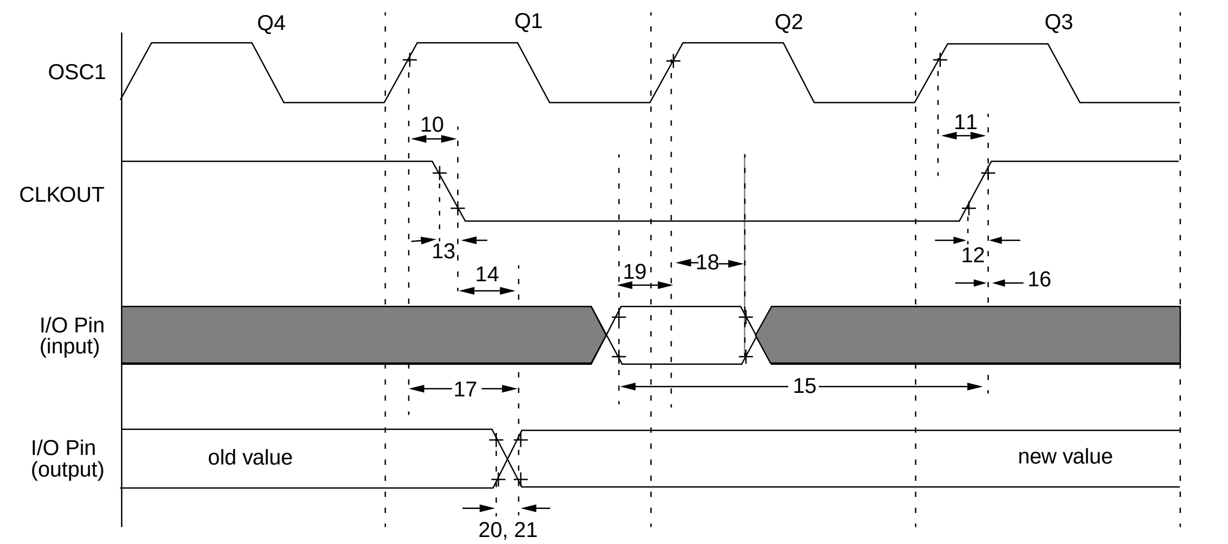
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

Applicable Devices	710	71	711	715

FIGURE 11-3: CLKOUT AND I/O TIMING



Note: Refer to Figure 11-1 for load conditions.

TABLE 11-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓		—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑		—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time		—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time		—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑		0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid		—	—	80 - 100	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)		TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)		TBD	—	—	ns	
20*	TioR	Port output rise time	PIC16**C**710/711	—	10	25	ns	
			PIC16**LC**710/711	—	—	60	ns	
21*	TioF	Port output fall time	PIC16**C**710/711	—	10	25	ns	
			PIC16**LC**710/711	—	—	60	ns	
22††*	Tinp	INT pin high or low time		20	—	—	ns	
23††*	Trbp	RB7:RB4 change INT high or low time		20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

Applicable Devices	710	71	711	715

FIGURE 12-14: TYPICAL IDD vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

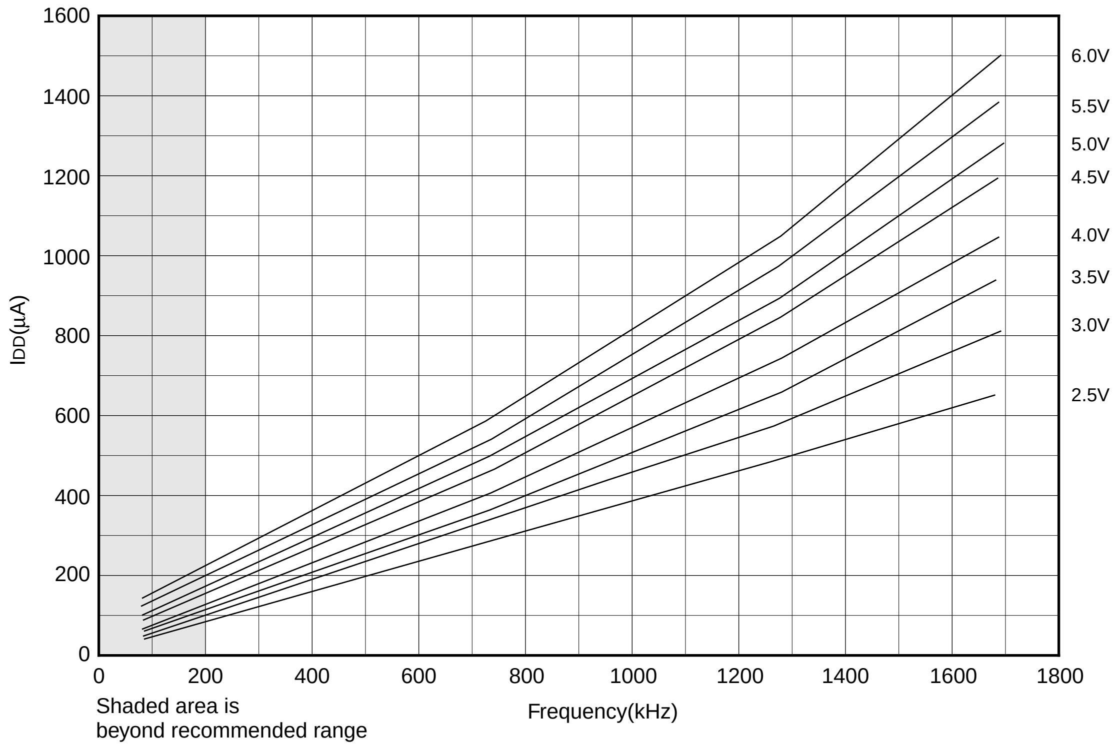
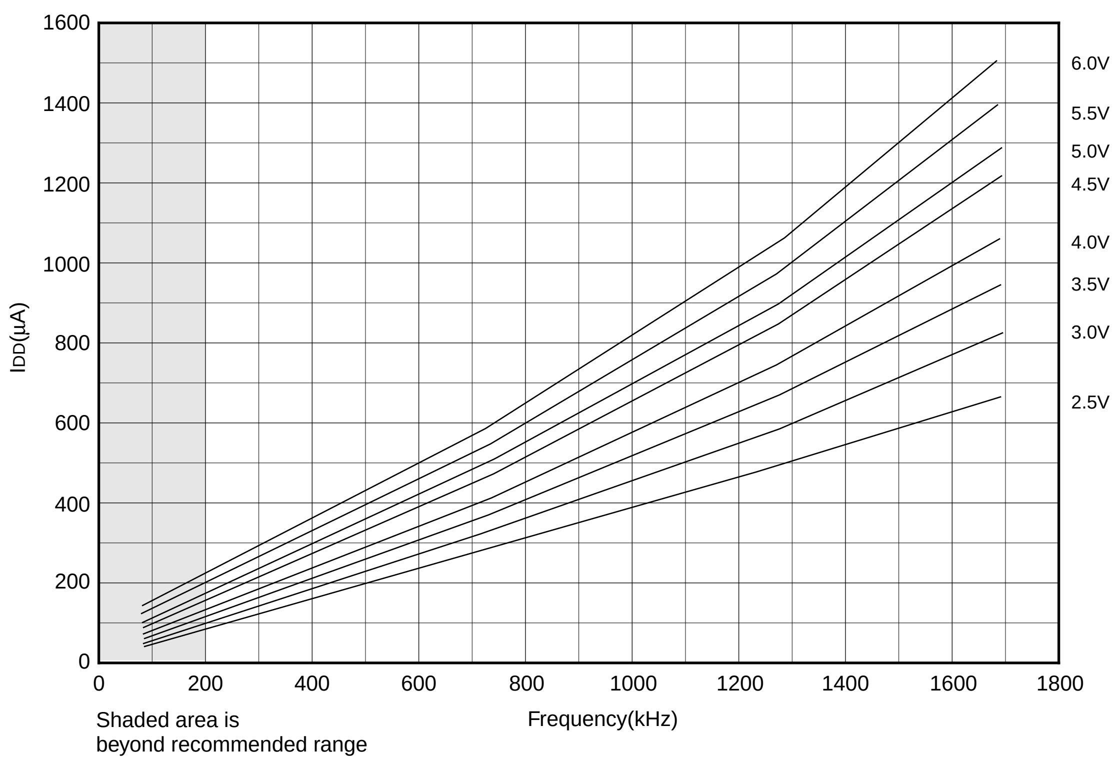


FIGURE 12-15: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)



Applicable Devices	710	71	711	715

FIGURE 12-16: TYPICAL IDD vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

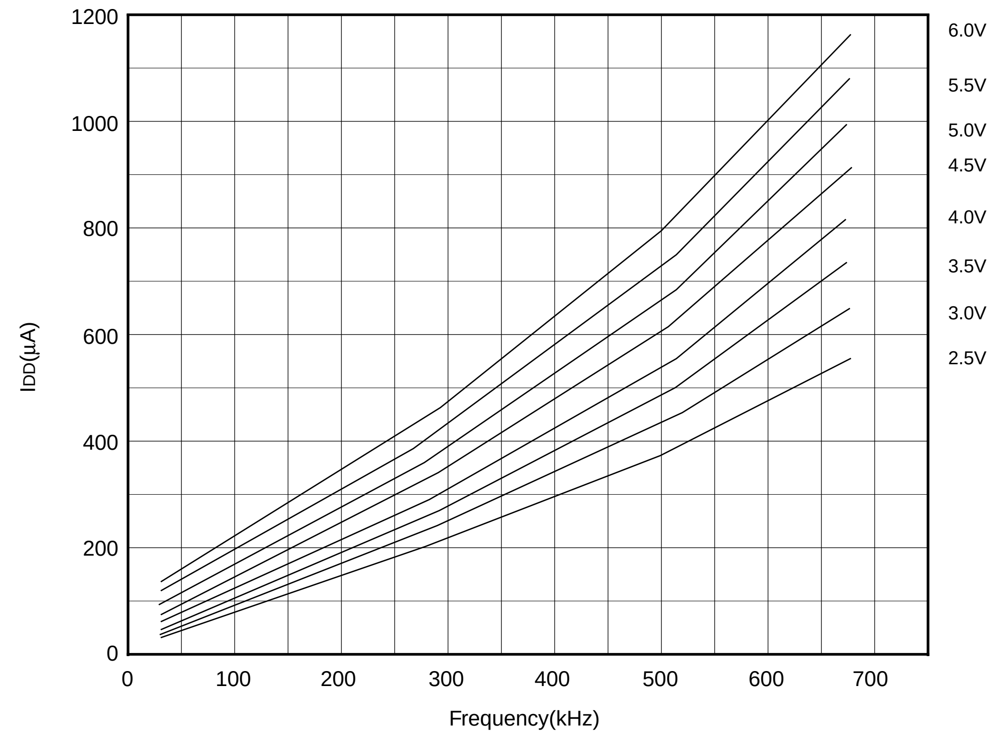
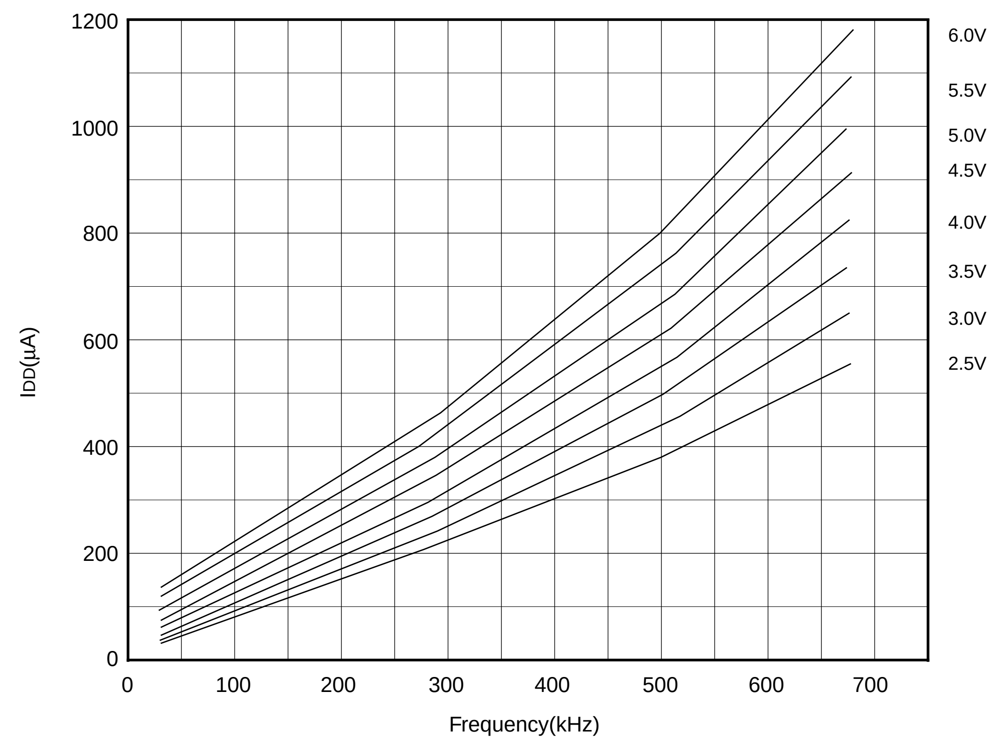


FIGURE 12-17: MAXIMUM IDD vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Applicable Devices	710	71	711	715

13.3 DC Characteristics: PIC16C715-04 (Commercial, Industrial, Extended) PIC16C715-10 (Commercial, Industrial, Extended) PIC16C715-20 (Commercial, Industrial, Extended) PIC16LC715-04 (Commercial, Industrial))

DC CHARACTERISTICS		**Standard Operating Conditions (unless otherwise stated)** Operating temperature 0˚C ≤ TA ≤ +70˚C (commercial) -40˚C ≤ TA ≤ +85˚C (industrial) -40˚C ≤ TA ≤ +125˚C (extended) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.					
Param No.	**Characteristic**	**Sym**	**Min**	**Typ †**	**Max**	**Units**	**Conditions**
	Input Low Voltage						
	I/O ports	V_{IL}					
D030	with TTL buffer		V_{SS}	-	0.5V	V	
D031	with Schmitt Trigger buffer		V_{SS}	-	$0.2V_{DD}$	V	
D032	$\overline{MCLR}$, RA4/T0CKI,OSC1 (in RC mode)		V_{SS}	-	$0.2V_{DD}$	V	
D033	OSC1 (in XT, HS and LP)		V_{SS}	-	$0.3V_{DD}$	V	Note1
	Input High Voltage						
	I/O ports	V_{IH}		-			
D040	with TTL buffer		2.0	-	V_{DD}	V	$4.5 \le V_{DD} \le 5.5V$
D040A			$0.8V_{DD}$	-	V_{DD}	V	For $V_{DD} > 5.5V$ or $V_{DD} < 4.5V$
D041	with Schmitt Trigger buffer		$0.8V_{DD}$	-	V_{DD}	V	For entire V_{DD} range
D042	$\overline{MCLR}$, RA4/T0CKI RB0/INT		$0.8V_{DD}$	-	V_{DD}	V	
D042A	OSC1 (XT, HS and LP)		$0.7V_{DD}$	-	V_{DD}	V	Note1
D043	OSC1 (in RC mode)		$0.9V_{DD}$	-	V_{DD}	V	
D070	PORTB weak pull-up current	I_{PURB}	50	250	400	µA	V_{DD} = 5V, V_{PIN} = V_{SS}
	Input Leakage Current (Notes 2, 3)						
D060	I/O ports	I_{IL}	-	-	±1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
D061	$\overline{MCLR}$, RA4/T0CKI		-	-	±5	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
D063	OSC1		-	-	±5	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT, HS and LP osc configuration
	Output Low Voltage						
D080	I/O ports	V_{OL}	-	-	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	I_{OL} = 7.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D083	OSC2/CLKOUT (RC osc config)		-	-	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	I_{OL} = 1.2 mA, V_{DD} = 4.5V, -40°C to +125°C

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

Applicable Devices	710	71	711	715

FIGURE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

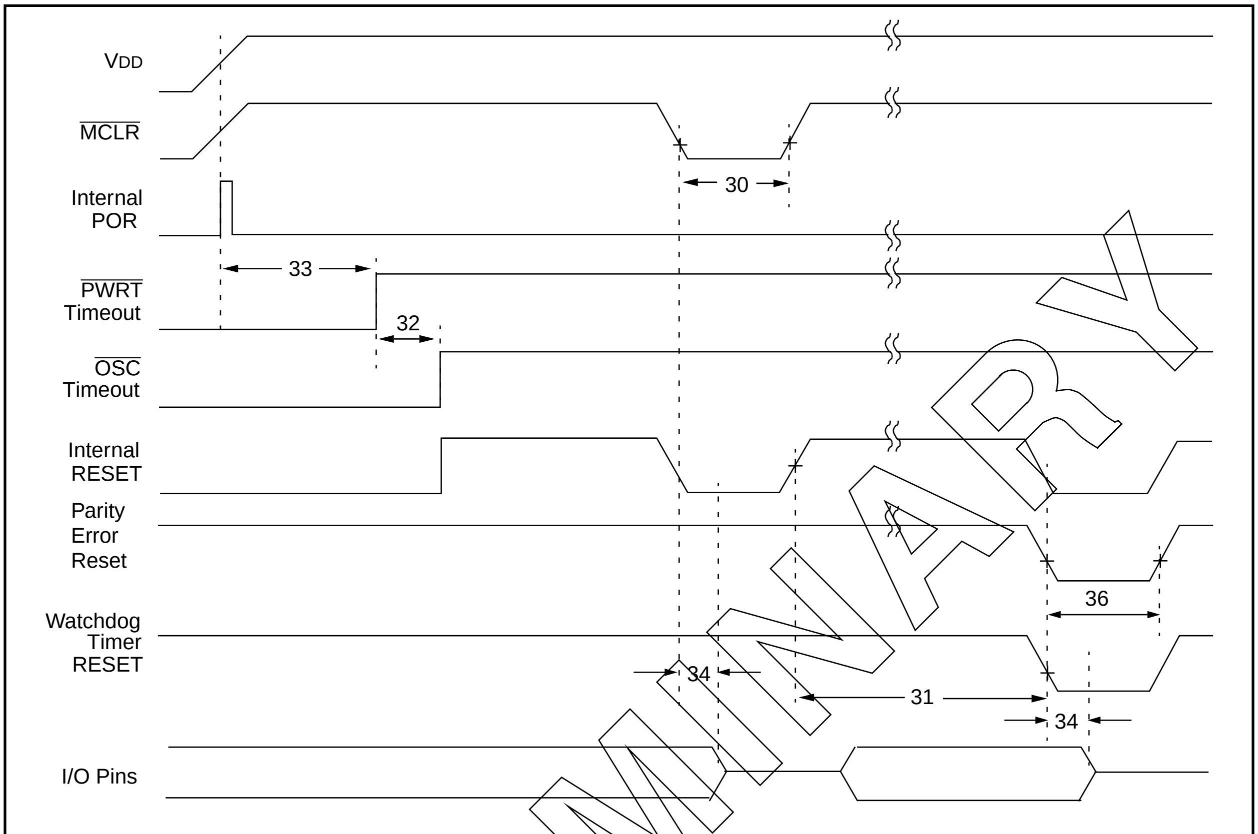


FIGURE 13-5: BROWN-OUT RESET TIMING

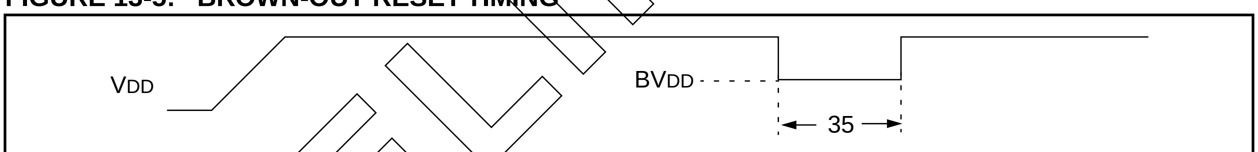


TABLE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

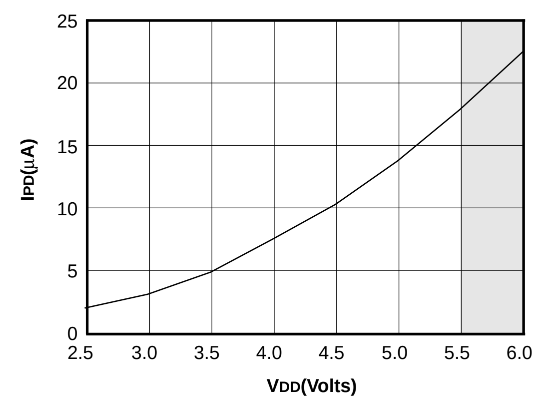
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	VDD = 5V, -40˚C to +125˚C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40˚C to +125˚C
32	Tost	Oscillation Start-up Timer Period	—	1024TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40˚C to +125˚C
34	TIOZ	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.1	µs	
35	TBOR	Brown-out Reset pulse width	100	—	—	µs	VDD ≤ BVDD (D005)
36	TPER	Parity Error Reset	—	TBD	—	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

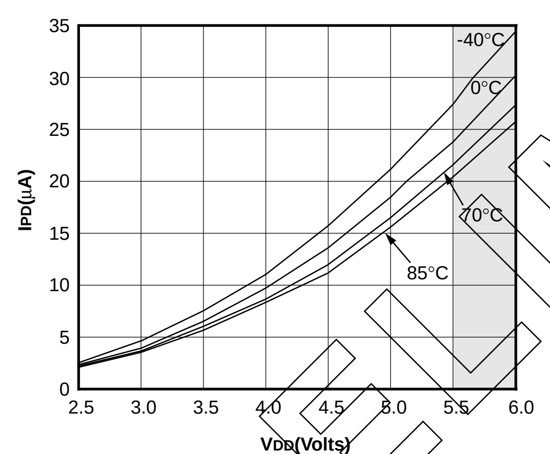
Applicable Devices	710	71	711	715

FIGURE 14-3: TYPICAL IPD vs. VDD @ 25°C (WDT ENABLED, RC MODE)



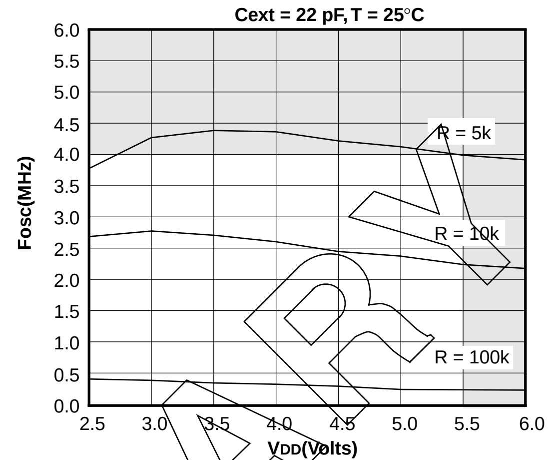
Shaded area is beyond recommended range.

FIGURE 14-4: MAXIMUM IPD vs. VDD (WDT ENABLED, RC MODE)



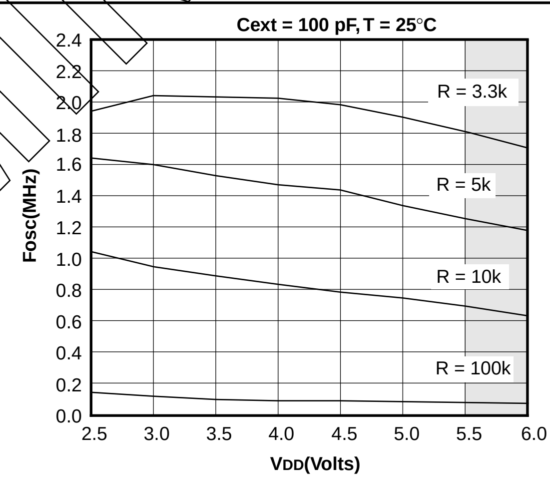
Shaded area is beyond recommended range.

FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



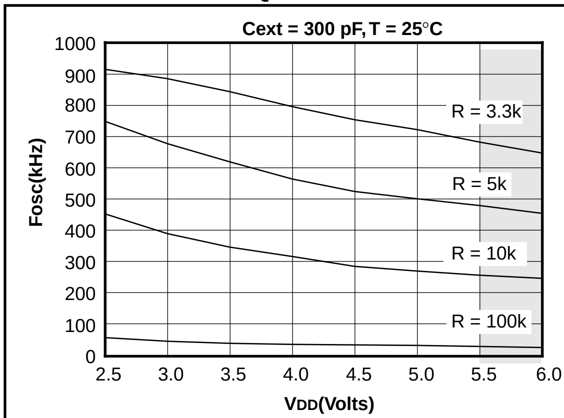
Shaded area is beyond recommended range.

FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Shaded area is beyond recommended range.

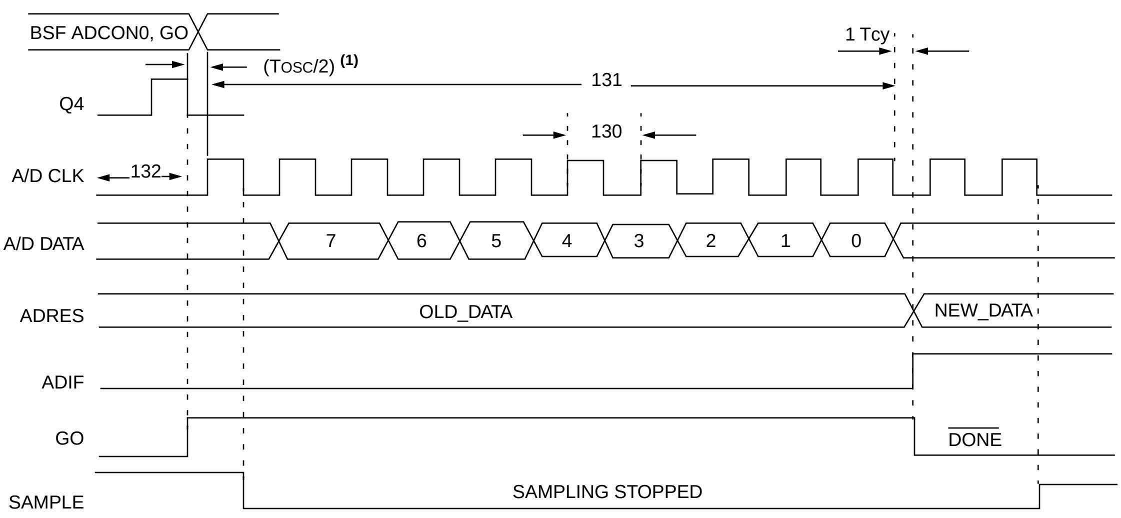
FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD



Shaded area is beyond recommended range.

Applicable Devices	710	71	711	715

FIGURE 15-6: A/D CONVERSION TIMING



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 15-7: A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC16**C**71	2.0	—	—	µs	TOSC based, VREF ≥ 3.0V
			PIC16**LC**71	2.0	—	—	µs	TOSC based, VREF full range
			PIC16**C**71	2.0	4.0	6.0	µs	A/D RC Mode
			PIC16**LC**71	3.0	6.0	9.0	µs	A/D RC Mode
131	TCNV	Conversion time (not including S/H time) (Note 1)		—	9.5	—	TAD	
132	TACQ	Acquisition time		Note 2	20	—	µs	
				5*	—	—	µs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 19.5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
134	TGO	Q4 to A/D clock start		—	Tosc/2§	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
135	TSWC	Switching from convert → sample time		1.5§	—	—	TAD	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

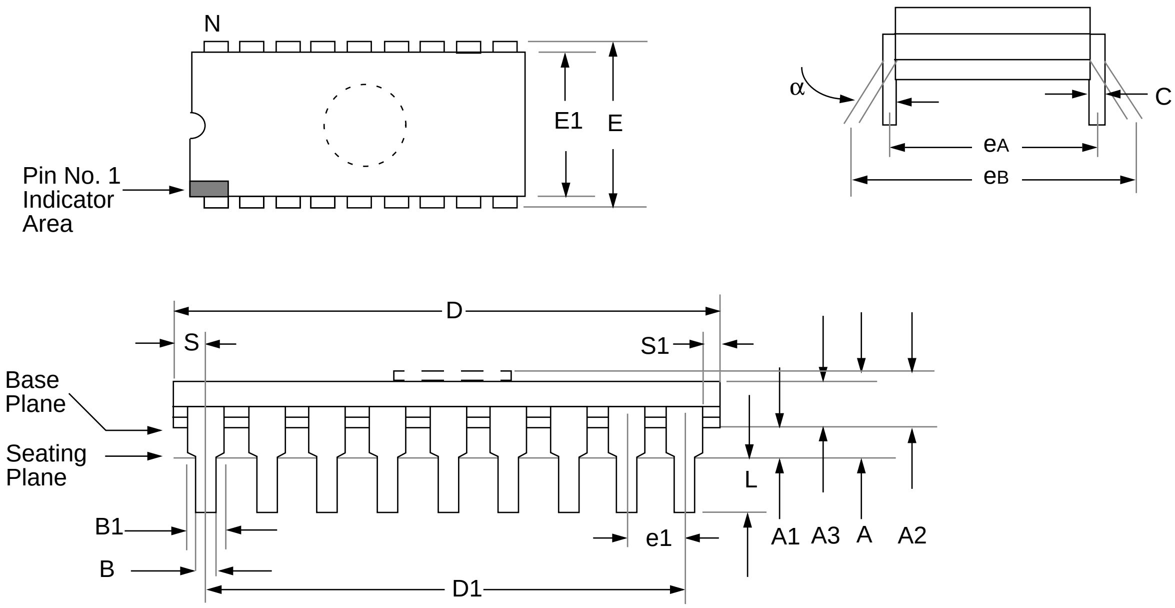
§ These specifications ensured by design.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Section 7.1 for min conditions.

17.0 PACKAGING INFORMATION

17.1 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil) (JW)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.7780		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	**Reference**	0.800	0.800	**Reference**
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Reference**	0.100	0.100	**Reference**
eA	7.366	8.128	**Typical**	0.290	0.320	**Typical**
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

APPENDIX C: WHAT'S NEW

1. Consolidated all pin compatible 18-pin A/D based devices into one data sheet.

APPENDIX D: WHAT'S CHANGED

1. Minor changes, spelling and grammatical changes.
2. Low voltage operation on the PIC16LC710/711/715 has been reduced from 3.0V to 2.5V.
3. Part numbers of the PIC16C70 and PIC16C71A have changed to PIC16C710 and PIC16C711, respectively.

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

01/18/02