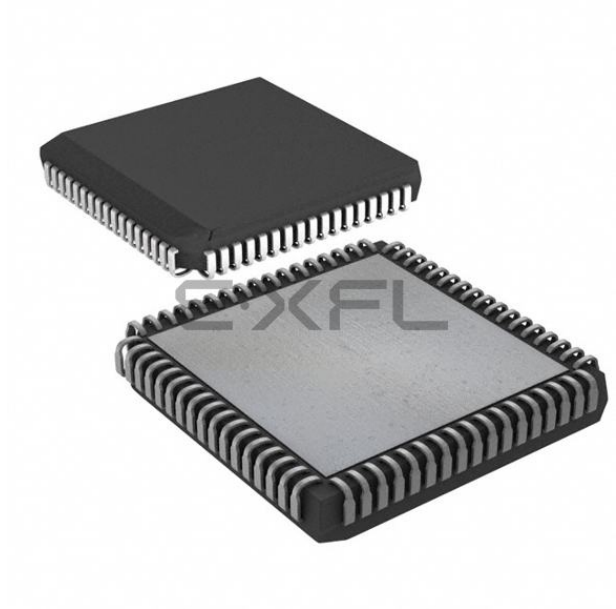
Analog Devices Inc./Maxim Integrated - DS87C550-QCL+ Datasheet



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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, PWM, WDT
Number of I/O	55
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c550-qcl

PIN DESCRIPTION Table 1

PLCC/ CLCC	QFP	SIGNAL NAME	DESCRIPTION
2	72	V_{CC}	**V_{CC} -** Digital +5V power input.
36 37	34 35	GND	**GND –** Digital ground.
15	9	RST	**RST - I/O.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external Reset sources. An RC is not required for power-up, as the DS87C550 provides this function internally. This pin also acts as an output when the source of the reset is internal to the device (i.e., watchdog timer, power-fail, or crystal-fail detect). In this case, the RST pin will be held high while the processor is in a Reset state, and will return to low as the processor exits this state. When this output capability is used, the RST pin should not be connected to an RC network or a logic output driver.
35 34	32 31	XTAL1 XTAL2	**Input -** The crystal oscillator pins XTAL1 and XTAL2 provide support for fundamental mode, parallel resonant, AT cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier. Note that this output cannot be used to drive any additional load when a crystal is attached as this can disturb the oscillator circuit.
47	48	$\overline{\text{PSEN}}$	**$\overline{\text{PSEN}}$ - Output.** The Program Store Enable output. This signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ will provide an active low pulse during a program byte access, and is driven high when not accessing external program memory.
48	49	ALE	**ALE - Output.** The Address Latch Enable output functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE is driven high when the DS87C550 is in a Reset condition. ALE can also be disabled and forced high using the EMI reduction mode ALEOFF.
49	50	$\overline{\text{EA}}$	**$\overline{\text{EA}}$ - Input.** An active low input pin that when connected to ground will force the DS87C550 to use an external program memory. The internal RAM is still accessible as determined by register settings. $\overline{\text{EA}}$ should be connected to V_{CC} to use internal program memory. The input level on this pin is latched at reset.
16-23	10-17	P1.0-P1.7	**Port 1 - I/O.** Port 1 functions as both an 8-bit, bi-directional I/O port and an alternate functional interface for several internal resources. The reset condition of Port 1 is all bits at logic 1. In this state, a weak pullup holds the port high. This condition allows the pins to serve as both input and output. Input is possible since any external circuit whose output drives the port will overcome the weak pullup. When software writes a 0 to any Port 1 pin, the DS87C550 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again returns to a weakly held high output (and input) state. The alternate functions of Port 1 pins are detailed below. Note that when the Capture/Compare functions of timer 2 are used, the interrupt input pins become capture trigger inputs. **Port Alternate Function** P1.0 INT2/CT0 External Interrupt 2/Capture Trigger 0 P1.1 INT3/CT1 External Interrupt 3/Capture Trigger 1 P1.2 INT4/CT2 External Interrupt 4/Capture Trigger 2 P1.3 INT5/CT3 External Interrupt 5/Capture Trigger 3 P1.4 T2 External I/O for Timer/Counter 2 P1.5 T2EX Timer/Counter 2 Capture/Reload Trigger P1.6 RXD1 Serial Port 1 Input P1.7 TXD1 Serial Port 1 Output
16 17 18 19 20 21 22 23	10 11 12 13 14 15 16 17		

COMPATIBILITY

The DS87C550 is a fully static, CMOS 8051-compatible microcontroller designed for high performance. While remaining familiar to 8051 family users, it has many new features. With very few exceptions, software written for existing 8051-based systems works without modification on the DS87C550. The exception is critical timing since the High Speed Micro performs its instructions much faster than the original for any given crystal selection. The DS87C550 runs the standard 8051 family instruction set and is pin-compatible with existing devices with similar features in PLCC or QFP packages.

The DS87C550 provides three 16-bit timer/counters, two full-duplex serial ports, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers default to a 12 clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 4 clocks per cycle if desired.

The DS87C550 provides several new hardware features implemented by new Special Function Registers. A summary of all SFRs is provided in Table 2.

PERFORMANCE OVERVIEW

The DS87C550 features a high-speed, 8051-compatible core. Higher speed comes not just from increasing the clock frequency, but also from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C550, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C550 will see the full 3 to 1 speed improvement. However, some instructions will achieve between 1.5 and 2.4 to 1 improvement. Regardless of specific performance improvements, all instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual mix of instructions used. Speed sensitive applications would make the most use of instructions that are 3 times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any arbitrary combination of instructions. These architecture improvements and the sub-micron CMOS design produce a peak instruction cycle in 121 ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS87C550 perform exactly the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the High Speed Micro User's Guide. However, counter/timers default to run at the old 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct"

instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C550, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles, but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C550 usually uses one instruction cycle for each instruction byte. Examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High Speed Micro User's Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C550. This allows the DS87C550 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C550 duplicates the SFRs contained in the standard 80C52. Table 2 shows the register addresses and bit locations. Many are standard 80C52 registers. The High Speed Micro User's Guide describes all SFRs in full detail.

SPECIAL FUNCTION REGISTER LOCATION: Table 2

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
PORT0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	ID1	ID0	TSL	-	-	-	-	SEL	86h
PCON	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
RCON	-	-	-	-	CKRDY	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PMR	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEOFF	DEM1	DME0	9Fh
PORT2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
SADDR0									A1h
SADDR1									A2h
IE	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	A8h
CMPL0									A9h
CMPL1									AAh
CMPL2									ABh
CPTL0									ACh
CPTL1									ADh
CPTL2									AEh
CPTL3									AFh
PORT3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
ADCON1	STRT/BSY	EOC	CONT/SS	ADEX	WCQ	WCM	ADON	WCIO	B2h

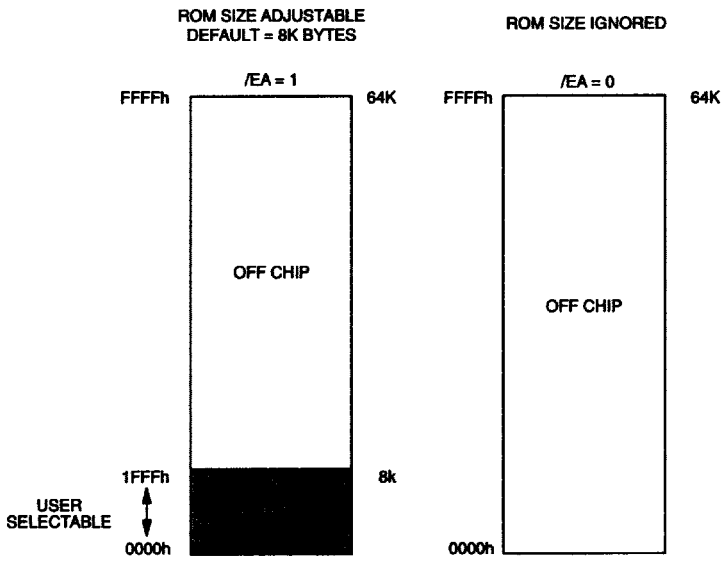
SPECIAL FUNCTION REGISTER LOCATION: Table 2 continued

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
ADCON2	OUTCF	MUX2	MUX1	MUX0	APS3	APS2	APS1	APS0	B3h
ADMSB									B4h
ADLSB									B5h
WINHI									B6h
WINLO									B7h
IP	-	PAD	PS1	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	$\overline{RL2}$	BEh
T2MOD	-	-	-	-	-	-	T2OE	DCEN	BFh
PORT4	CMT1	CMT0	CMSR5	CMSR4	CMSR3	CMSR2	CMSR1	CMSR0	C0h
ROMSIZE	-	-	-	-	-	RMS2	RMS1	RMS0	C2h
PORT5	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	C4h
STATUS	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA									C7h
T2IR	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF1	IE2/CF0	C8h
CMPH0									C9h
CMPH1									CAh
CMPH2									CBh
CPTH0									CCh
CPTH1									CDh
CPTH2									CEh
CPTH3									CFh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
PW0FG									D2h
PW1FG									D3h
PW2FG									D4h
PW3FG									D5h
PWMADR	ADRS	-	-	-	-	-	PWE1	PWE0	D6h
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	D8h
SBUF1									D9h
PWM0									DCh
PWM1									DDh
PWM2									DEh
PWM3									DFh
ACC									E0h
PW01CS	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN	E1h
PW23CS	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN	E2h
PW01CON	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C	E3h
PW23CON	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C	E4h
RLOADL									E6h
RLOADH									E7h
EIE	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EX1	EX2/EC0	E8h
T2SEL	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0	EAh
CTCON	$\overline{CT3}$	CT3	$\overline{CT2}$	CT2	$\overline{CT1}$	CT1	$\overline{CT0}$	CT0	EBh
TL2									ECh
TH2									EDh
SETR	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0	EEh
RSTR	CMTE1	CMTE0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	EFh
B									F0h
PORT6	STADC	-	PWMC1	PWMC0	PWMO3	PWMO2	PWMO1	PWMO0	F1h
EIP	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0	F8h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	FFh

ROM address of 5k. This would cause the current address to switch from internal to external and potentially cause invalid operation. Similarly, do not instantly switch from external to internal memory. For example, do not select a maximum ROM address of 8kB from an external ROM address of 7kB (if ROMSIZE is set for 4kB or less).

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not available as I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the EA pin is logic 0. EA overrides all bit settings. The PSEN signal will go active (low) to serve as a chip enable or output enable when Ports 0 & 2 fetch from external ROM.

ROM MEMORY MAP Figure 2



DATA MEMORY

Unlike many 8051 derivatives, the DS87C550 contains additional on-chip data memory. In addition to the standard 256 bytes of data RAM accessed by direct instructions, the DS87C550 contains another 1kB of data memory that is accessed using the MOVX instruction. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is permanently located from address 0000h to 03FFh (when enabled).

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 1kB automatically go to external memory through Ports 0 & 2.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 & 2. This also is the default condition. This default allows the DS87C550 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using two bits in the Power Management Register (DME1, DME0). This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. These bits have the following operation:

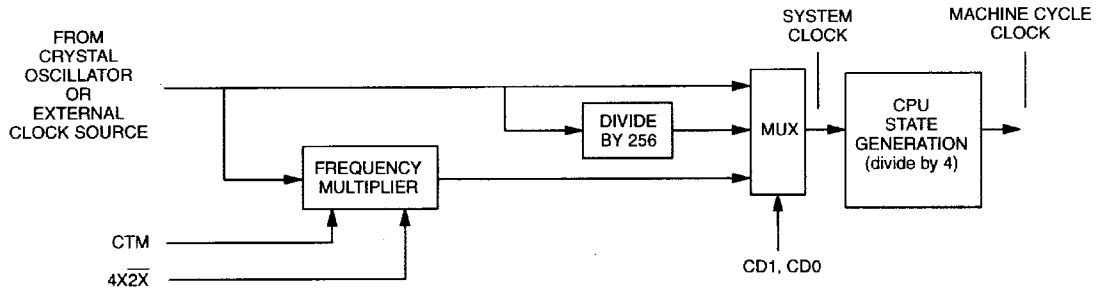
CLOCK SWITCHING RESTRICTIONS

To ensure clean "glitch-free" switching of the system clock and to ensure that all clocks are running and stable before they are used, there are minor restrictions on accessing the clock selection bits CD1:0 and the 4X/$\overline{2X}$ bit.

One restriction is that any change in the CD1 and CD0 bits from a condition other than a 1 0 state (i.e., clock divided by 4 mode) must pass through the divide-by-4 state before proceeding to the desired state. As a specific example, if the clock divisor bits are set to use the frequency multiplier in 4X mode, no other clock setting is possible until after the CD1:0 bits are set to divide-by-4 mode. After setting clock divided-by-4 mode, then clock divided by 1024 can be selected by setting CD1 and CD0 to "11b". Any attempt to change these bits to a disallowed state will be ignored by the hardware.

There are also some minor restrictions when changing from one clock multiplier to another. Changing the clock multiplier can only be performed when the Crystal Multiplier Enable bit CTM (PMR.4) is set to 0. This bit disables the clock multiplication function. However, the CTM bit can only be changed when CD1 and CD0 are set to divide-by-4 mode (i.e., "10b") and the ring mode (RNGMD = RCON.2) bit is 0 (discussed later). Changing the clock multiplication factor also requires that the new frequency be stable prior to effecting the change. The SFR bit CKRDY (RCON.3) indicates the state of the stabilization timeout. Setting the CTM bit to a 0 from a 1 disables the clock multiplier function, automatically clears the CKRDY bit, and starts the stabilization timeout.

SYSTEM CLOCK CONTROL Figure 3



During the stabilization period, CKRDY will remain low, and software will be unable to set the CD1:0 bits to select the frequency multiplier. After the stabilization delay, CKRDY will be set to a 1 by hardware. Note that this bit cannot be set to 1 by software. After hardware sets CKRDY bit, then the CD1:0 bits can be set to use the clock multiplier function. However, before changing CD1:0, the 4X/$\overline{2X}$ bit must be set to the desired state. Following this, the CTM bit must be set to 1 to enable the crystal multiplier. Finally the CD1:0 bits may be set to select the crystal multiplier function. By following this procedure, the processor is guaranteed to receive a stable, glitch-free clock.

OSCILLATOR-FAIL DETECT

The DS87C550 contains a unique safety mechanism called an on-chip Oscillator-Fail Detect circuit. When enabled, this circuit causes the processor to be reset if the oscillator frequency falls below 40kHz. The processor is held in reset until the oscillator frequency rises above 40kHz. In operation, this circuit can provide a backup for the watchdog timer. Normally, the watchdog timer is initialized so that it will timeout and will cause a processor reset in the event that the processor loses control. This works perfectly as long as there is a clock from the crystal or external oscillator, but if this clock fails, there is the potential for the processor to fail in an uncontrolled and possibly undesirable state. With the use of the

Switchback

One of the other unique features included on the DS87C550 is Switchback. Simply, Switchback when enabled will allow serial ports and interrupts to automatically switch back from divide-by-1024 (PMM) to divide-by-4 (standard speed operation). This feature makes it very convenient to use the Power Management Mode in real time applications. Of course to return to a divide-by-4 clock rate from divide-by-1024 PMM, software can simply select the CD1 & CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C550 provides hardware alternatives for automatic Switchback to standard speed operation.

The Switchback feature is enabled by setting the SFR bit SWB (PMR.5) to a 1. Once it is enabled and when PMM is selected, there are two possible events that can cause an automatic switchback to divide-by-4 mode. First, if an interrupt occurs and is set so that it will be acknowledged, this event will cause the system clock to revert from PMM to divide-by-4 mode. For example, if $\overline{\text{INT0}}$ is enabled then Switchback will occur on $\overline{\text{INT0}}$. However, if $\overline{\text{INT0}}$ is not enabled, then activity on $\overline{\text{INT0}}$ will not cause switchback to occur.

A Switchback can also occur when an enabled UART detects the start bit indicating the beginning of an incoming serial character or when the SBUF register is loaded initiating a serial transmission. Note that a serial character's start bit does not generate an interrupt. This occurs only on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception or transmission. So with Switchback enabled and a serial port enabled, the automatic switch to normal speed operation occurs automatically in time to receive or transmit a complete serial character as if nothing special had happened.

Once Switchback causes the processor to make the transition back to divide-by-4 mode, software must modify SFR bits CD1 & CD0 to re-enter Power Management Mode. However, if a serial port is in the process of transmitting or receiving a character, then this change back to PMM will not be allowed as the hardware prevents a write to CD1 & CD0 during any serial port activity.

Since the reception of a serial start bit or an interrupt priority lockout is normally undetectable by software in an 8051, the Status register features several new flags that are useful. These are described below.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C550 supports three levels of interrupt priority. These levels are Power-fail, High, and Low. Status bits STAT.7-5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS.7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The DS87C550 allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to a 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain inactive when performing on-chip memory access. The default state is ALEOFF = 0 so ALE normally toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C550 provides several of the most commonly needed peripheral functions in microcomputer-based systems. New functions include a second serial port, power-fail reset, power-fail interrupt flag, and a programmable watchdog timer. In addition, the DS87C550 contains an analog-to-digital converter and four channels of pulse width modulation for industrial control and measurement applications. Each of these peripherals is described below. More details are available in the *High-Speed Microcontroller User's Guide: DS87C550 Supplement*.

SERIAL PORTS

The DS87C550 provides a serial port (UART) that is identical to the 80C52. In addition, it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.6 (RXD1) and P1.7 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1, SBUF1) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

Control for serial port 0 is provided by the SCON0 register while its I/O buffer is SBUF0. The registers SCON1 and SBUF1 provide the same functions for the second serial port. A full description of the use and operation of both serial ports may be found in the *High-Speed Microcontroller User's Guide*, available from the Maxim website.

ANALOG TO DIGITAL CONVERTER

The DS87C550 contains a 10-bit successive approximation analog-to-digital converter. This converter provides eight multiplexed channels of analog input using an external voltage reference for the conversion process.

Before using the A/D converter, the converter must be configured by performing two actions:

1. The user must set the ADON bit (ADCON1.1). This enables the A/D converter. This bit defaults to 0 following a reset, disabling the A/D converter to conserve power.
2. In addition, the user must set the ADRS bit (PWMADR.7) to enable the external voltage reference pins. This bit defaults to 0 following a reset, disabling the A/D converter voltage reference pins.

A/D CONVERTER INPUTS

The A/D converter of the DS87C550 provides eight channels of analog input on device pins ADC7 through ADC0 (P5.7-P5.0). The signals on these pins are input into an analog multiplexer. The magnitude (and polarity) of these signals is limited by the external reference (A_{VREF+}, A_{VREF-}) voltages used by the converter. See the DC electrical characteristics section of this data sheet for more details.

Selecting a single analog signal for conversion is achieved by software writing the desired channel number (0 through 7) into the MUX2 -MUX0 bits (ADCON2.6-4). The selected input is then provided to a sample and hold circuit that maintains a steady signal during the conversion process.

A/D CONVERSION PROCESS

The A/D conversion process can be configured for one-shot or continuous mode operation. For one-shot operation, the SFR bit CONT/SS (ADCON1.5) must be a 0. The conversion process is then initiated by software writing a 1 to the STRT/BSY SFR bit (ADCON1.7) if the ADEX (ADCON1.4) bit is a 0. If the ADEX bit is a 1, then the conversion is initiated by an active low signal on the external pin STADC (P6.7). If continuous mode is selected (CONT/SS = 1), then the first conversion is initiated as described above, but another conversion will be automatically started at the completion of the previous conversion.

Once initiated, the conversion process requires 16 A/D clock periods (T_{ACLK}) to complete. Because of the dynamic nature of the converter, the A/D clock period can be no less that 1 µs and no more than 6.25 µs. This requirement is expressed as follows:

$$1.0\ \mu s \le T_{ACLK} \le 6.25\ \mu s$$

Therefore, any single conversion time can range from 16µs (min) to 100µs (max), depending on the selected A/D clock frequency.

The A/D clock frequency is a function of the processor's machine cycle clock and the A/D clock's prescaler setting as shown by the following equation:

$$T_{ACLK} = T_{MCLK} * (N+1)$$

where N is the prescaler setting in APS3:0.

The processor's machine cycle clock period (T_{MCLK}) is normally the external crystal (or oscillator) frequency multiplied by 4 (but can be affected by the CD1, CD0, and 4X/$\overline{2X}$ bits). The A/D clock period must be set by the user to ensure that it falls within the minimum and maximum values specified above. As an example, assume the processor's crystal frequency is 33MHz and that the processor is running in a standard divide-by-4 mode. This means that the period of the processors machine cycle clock, i.e., T_{MCLK}, will be (1/33MHz)*4 or 121.2 ns. If it is assumed that the application requires the fastest possible conversion time, then the desired T_{ACLK} is 1.0 µs. The necessary prescale value can then be calculated as:

$$N = (T_{ACLK}/T_{MCLK})-1$$

Therefore for this example, N = 7.25. Since N must be an integer, the value of N must be 8 (rounded up to the next integer). This results in a conversion clock T_{ACLK} = 1.091 µs.

The prescaler value must be stored in APS3-APS0 (ADCON2.3-0) to achieve the proper A/D clock. These bits default to 0 on reset, so they must be set as desired by the processor's initialization software.

A/D OUTPUT

There are two SFR locations that contain the result of the A/D conversion process. They are ADMSB (most significant byte) and ADLSB (least significant byte). The ADLSB byte always contains the 8 least significant bits of the 10-bit result. The ADMSB can be configured in two different ways through the use of the SFR bit OUTCF (ADCON2.7). If OUTCF is a 0, then ADMSB contains the 8 most significant bits

PULSE WIDTH MODULATION

The DS87C550 contains four independent 8-bit pulse width modulator (PWMs) functions each with independently selectable clock sources. For more precise modulation operations, two 8-bit PWM functions (PWM0 & PWM1 and/or PWM2 & PWM3) can be cascaded together to form a 16-bit PWM function.

The PWM function is divided into three major blocks: a clock prescaler, a clock generator, and a pulse generator. A single prescaler provides selectable clocks of different frequencies to each of the four clock generator blocks. Each clock generator is an 8-bit reloadable counter that determines the repetition rate (frequency) of its associated PWM. Each pulse generator PWM block is an 8-bit timer clocked by the clock generator's output. When this timer reaches zero, the output of the PWM is set to 1. When the timer reaches the user selected PWM match value stored in SFR PWMx, the PWM output is cleared to 0. In this way, the frequency and duty cycle of the PWM is varied under software control.

PWM PRESCALER

The prescaler block of the PWM function accepts as a clock input the system clock provided to the CPU (and other peripherals), and divides it by 1, 4, 16, and 64. Each of these clocks is available at the output of the prescaler, and is provided to all four of the PWM clock generator blocks. The actual clock used by the clock generator block is dependant on the setting of SFR bits PWxS2:0 (where x is the PWM channel number 0-3) located in the PW01CS or PW23CS registers. In addition to selecting one of the prescaler's CPU clock divided outputs, setting PWxS2 to a 1 allows an external clock to be used as an input to the clock generators. The external clocks are input on device pins PWMC0 (P6.4 for PWM0 or PWM1) or PWMC1 (P6.5 for PWM2 or PWM3). Like all other inputs to the 8051, these inputs are synchronized by sampling them using the internal machine cycle clock. Therefore these inputs must be of sufficient duration for the clock to sample them properly (i.e., 2 machine cycles). The complete functionality of the clock selection SFR bits is as follows:

Prescaler Output	**PWxS2:0**
Machine Cycle_Clock/1	000
Machine Cycle_Clock/4	001
Machine Cycle_Clock/16	010
Machine Cycle_Clock/64	011
PWMCx (external)	1xx

In determining the exact frequency output of the prescaler, it is important to note that the machine cycle clock provided to the prescaler is also software-selectable. The machine cycle clock can be the crystal (or oscillator frequency) divided by 1, 2, 4, or 1024 as determined by the CD1:0 and the 4X/$\overline{2X}$ SFR bits (see Clock Divide Control section for details).

PWM CLOCK GENERATOR

The clock generator blocks of the PWM modules are pre-loaded by software with an 8-bit value, and this value determines the frequency or repetition rate of the PWM function. A value of 0 causes the selected output of the prescaler to be passed directly to the pulse generator function (i.e., divide by 1). A value of FFh passes a clock to the pulse generator function that is the selected prescaler output divided by 256. In general, the clock generators provide a divide by N+1 selectable repetition rate (i.e., frequency) for their PWM channel.

interrupt. To enable the interrupt, the Timer 2 interrupt enable bit ET2 (EIE.7) must be set to a 1. The 8-bit overflow interrupt or the 16-bit overflow interrupt is then individually enabled by setting TF2BS (T2SEL.6) or TF2S (T2SEL.7). Since there is only one interrupt vector for both possible Timer 2 interrupts, the interrupt service routine must determine which event caused the interrupt by polling the available flags. For both interrupt flags, software must clear them upon servicing the interrupt. There is no automatic hardware clearing of these flags.

TIMER 2 CAPTURE FEATURE

One of the new features added to Timer 2 is the capture function. The output of Timer 2 is available to four independent 16-bit capture register pairs (CPTH3:CPTL3, CPTH2:CPTL2, CPTH1:CPTL1, & CPTH0:CPTL0). These registers are loaded with the 16-bit value contained in Timer 2 when transitions occur on the corresponding input pin INT5/CT3, INT4/CT2, INT3/CT1 or INT2/CT0 (P1.3, P1.2, P1.1, or P1.0) respectively. When the capture function is not being used, these input pins also serve as external interrupt inputs. The Capture Trigger Control register (CTCON) can be programmed to make the capture occur on a rising edge, a falling edge, or on either a rising or a falling edge on these input pins. The functionality of the CTCON register is illustrated below. Note that the edge sensitivity established by the setting of CTCON bits applies to both the capture function and the external interrupt function of these input pins. This addition allows maximum flexibility in selecting interrupt polarity. Whether these input pins are used as external interrupt inputs or as capture commands, the input will set the appropriate flag in the External Interrupt Flag register (T2IR.3:0) and will create an interrupt if the associated enable in the Extended Interrupt Enable (EIE.3:0) register is set.

CTCON REGISTER FUNCTIONALITY

CTCON.7	$\overline{CT3}$	Capture register 3 triggered by a falling edge on INT5/CT3
CTCON.6	CT3	Capture register 3 triggered by a rising edge on INT5/CT3
CTCON.5	$\overline{CT2}$	Capture register 2 triggered by a falling edge on INT4/CT2
CTCON.4	CT2	Capture register 2 triggered by a rising edge on INT4/CT2
CTCON.3	$\overline{CT1}$	Capture register 1 triggered by a falling edge on INT3/CT1
CTCON.2	CT1	Capture register 1 triggered by a rising edge on INT3/CT1
CTCON.1	$\overline{CT0}$	Capture register 0 triggered by a falling edge on INT2/CT0
CTCON.0	CT0	Capture register 0 triggered by a rising edge on INT2/CT0

TIMER 2 COMPARE FEATURE

Another new feature added to Timer 2 capabilities is the compare function. Prior to enabling this function, the associated compare register pair (CMPH0:CMPL0, CMPH1:CMPL1, CMPH2:CMPL2) is loaded by software with a 16-bit number. Each time Timer 2 is incremented, the contents of these registers are compared with the new value of the timer. When a match occurs, the corresponding interrupt flag (T2IR.6:4) is set to a 1 on the next machine cycle and an interrupt will occur if the corresponding enable bit is set in the Extended Interrupt Enable (EIE.6:4) register. When a match with CMPH0:CMPL0 occurs, port pins P4.0 through P4.5 are set to a 1 if the corresponding bits of the Set Enable register (SETR) are at logic 1. If the match is with CMPH1:CMPL1, port pins P4.0 through P4.5 are reset to 0 when the corresponding bits in the reset/toggle enable register RSTR are at logic 1. A match with CMPH2:CMPL2 toggles port pins P4.6 and 4.7 if the corresponding bits in the RSTR register are at logic 1. Note that for the toggle function it is not the port pin latch that is actually toggled. Instead, separate flip-flops output the SFR bits TGFF1 and TGFF0 that actually determine the state of the respective port pin. A 0 in a bit position in either the SETR or the RSTR register disables the corresponding port pin function. The functionality of the SETR and RSTR registers is shown below.

SETR REGISTER FUNCTIONALITY

SETR.7	TGFF1	This bit toggles if CMPH2:CMPL2 and Timer 2 match and CMTE1 is 1
SETR.6	TGFF0	This bit toggles if CMPH2:CMPL2 and Timer 2 match and CMTE0 is 1
SETR.5	CMS5	If 1 then P4.5 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.4	CMS4	If 1 then P4.4 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.3	CMS3	If 1 then P4.3 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.2	CMS2	If 1 then P4.2 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.1	CMS1	If 1 then P4.1 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.0	CMS0	If 1 then P4.0 is set on a match between CMPH0:CMPL0 and Timer 2

RSTR REGISTER FUNCTIONALITY

RSTR.7	CMTE1	If 1 then P4.7 toggles on a match between CMPH2:CMPL2 and Timer 2
RSTR.6	CMTE0	If 1 then P4.6 toggles on a match between CMPH2:CMPL2 and Timer 2
RSTR.5	CMR5	If 1 then P4.5 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.4	CMR4	If 1 then P4.4 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.3	CMR3	If 1 then P4.3 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.2	CMR2	If 1 then P4.2 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.1	CMR1	If 1 then P4.1 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.0	CMR0	If 1 then P4.0 is reset on a match between CMPH1:CMPL1 and Timer 2

WATCHDOG TIMER

The free-running watchdog timer, if enabled, will set a flag and cause a reset if not restarted by software within the user selectable timeout period.

A typical application is to allow the flag to cause a reset. When the watchdog times out, it sets the Watchdog Timer Reset Flag (WTRF=WDCON.2), which generates a reset if enabled by the Enable Watchdog Timer Reset (EWT=WDCON.1) bit. In this way if the code execution goes awry and software does not reset the watchdog as scheduled, the processor is put in a known good state: reset.

In a typical initialization, software selects the desired timeout period using the WD1:0 and the system clock control bits. Then, it resets the timer and enables the processor reset function. After enabling the processor reset function, software must then reset the timer before its timeout period or hardware will reset the CPU. A Timed Access circuit protects both the EWT and the Watchdog Reset control (RWT = WDCON.0) bits. This prevents errant software from accidentally clearing the watchdog.

The watchdog timer is controlled by the Clock Control (CKCON) and the Watchdog Control (WDCON) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively, and they select the watchdog timeout period. Of course, the 4X/$\overline{2X}$ (PMR.3) and CD1:0 (PMR.7:6) system clock control bits also affect the timeout period. Selection of timeout is shown in Table 8.

WATCHDOG TIMEOUT VALUES Table 8

		INTERRUPT TIMEOUT (CLOCKS)				RESET TIME-CLOCKS			
4X/$\overline{2X}$	CD1:0	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15}+512	2^{18}+512	2^{21}+512	2^{24}+512
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16}+512	2^{19}+512	2^{22}+512	2^{25}+512
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17}+512	2^{20}+512	2^{23}+512	2^{26}+512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17}+512	2^{20}+512	2^{23}+512	2^{26}+512
x	11	2^{25}	2^{28}	2^{31}	2^{34}	2^{25}+512	2^{28}+512	2^{31}+512	2^{34}+512

unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 10. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

EPROM ERASURE CHARACTERISTICS

Erasure of the information stored in the DS87C550's EPROM occurs when the isolated gate structure of the EPROM stage element is exposed to certain wavelengths of light. While the gate structure is to some degree sensitive to a wide range of wavelengths, it is mostly wavelengths shorter than approximately 4,000 angstroms that are most effective in erasing the EPROM. Since fluorescent lighting and sunlight have wavelengths in this range, they can cause erasure if the device is exposed to them over an extended period of time (weeks for sunlight, years in room-level fluorescent light). For this reason (and others mentioned previously), it is recommended that an opaque covering be placed over the window of the -K (windowed PLCC) package type.

For complete EPROM erasure, exposure to ultraviolet light at approximately 2537 angstroms to a dose of 15W-sec/cm^2 at minimum is recommended. In practice, exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes at a distance of approximately 1 inch will normally be sufficient.

OTHER EPROM OPTIONS

The DS87C550 has user-selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

The EPROM selectable options may be programmed as shown in Table 10. The Option Register sets or reads these selections. The bits in the Option Register have the following function:

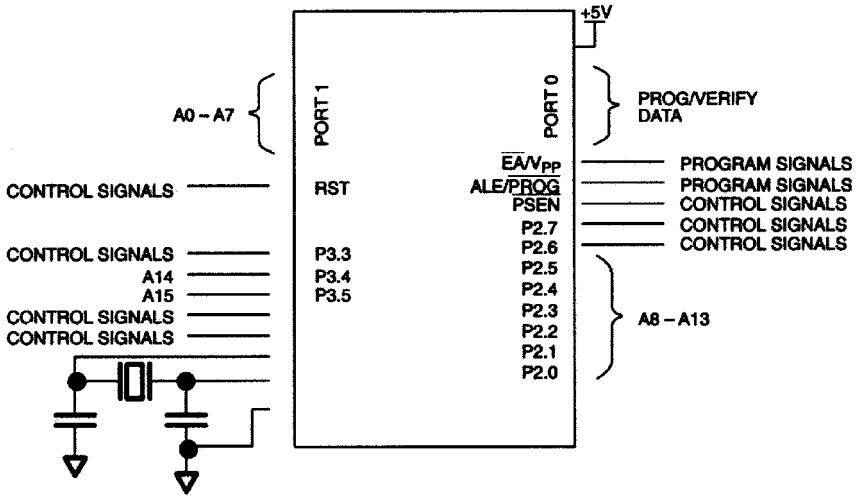
Bit 7 -4 Reserved. Program to a 1.
Bit 3 Watchdog POR default.
Set to 1: Watchdog reset function is disabled on power-up.
Set to 0: Watchdog reset function is enabled automatically on power up.
Bit 2-0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is located at programming addresses 30h, 31h, and 60h. This information is as follows:

Address	Value	Meaning
30h	DAh	Manufacturer
31h	55	Model
60h	00	Extension

EPROM PROGRAMMING CONFIGURATION Figure 5



A/D CONVERTER ELECTRICAL CHARACTERISTICS

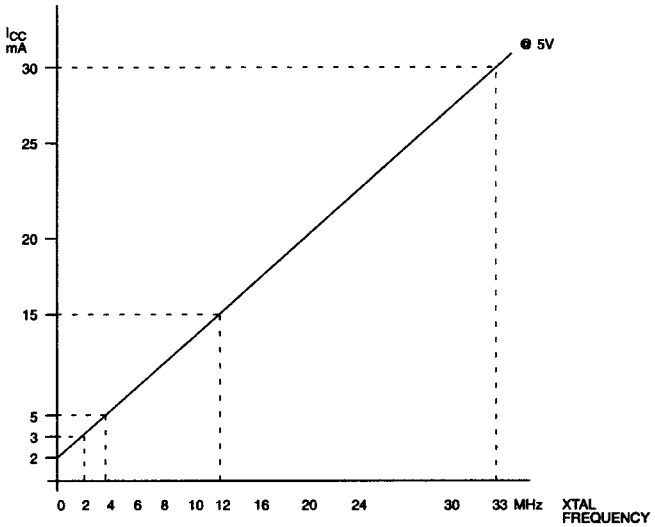
(AV_{CC}=V_{CC}=5V, V_{REF}=5V, f_{OSC}=4MHz, T_A=-40°C to 85°C, unless otherwise noted. Typical values are at T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Analog Supply Voltage	A_{VCC} A_{VSS}	V_{CC} GND		V_{CC} GND	V	
Analog Supply Current	AI_{DD}		0.7	2.3	mA	
Analog Idle Mode Current	AI_{DDI}			3.5	mA	
Analog Power-Down Mode Current	AI_{DDPD}		0.5	1	µA	
Analog Input Voltage	ADC7- ADC0	A_{VREF-}		A_{VREF+}	V	4
External Analog Reference Voltage	A_{VREF-} A_{VREF+}	AV_{SS}-0.2		AV_{CC} + 0.2	V	4
Analog Input Capacitance	C_{IN}		10	15	pF	4
A/D Clock	t_{ACLK}	1		6.25	µs	2, 4
Sampling Time	t_{ADS}	5 t_{ACLK}			t_{ACLK}	4
Conversion Time	t_{ADC}	16 t_{ACLK}			t_{ACLK}	3, 4
Resolution		10			Bits	4
Differential non-linearity	E_{DL}			±1.0	LSB	
Integral non-linearity	E_{IL}			±2.0	LSB	
Offset Error	E_{OS}			±2.0	LSB	
Gain Error	E_G			±1.0	%	
Cross-talk between A/D inputs	E_{CT}		-60		dB	4

NOTES FOR A/D CONVERTER ELECTRICAL CHARACTERISTICS

1. The following condition must not be exceeded: GND-0.2V < AV_{SS} < V_{CC} + 0.2V.
2. Due to the dynamic nature of the A/D converter, t_{ACLK} has both min and max specifications.
3. A complete conversion cycle requires 16 ACLK periods, including five input sampling periods.
4. This parameter is guaranteed by design.

TYPICAL I_{CC} VERSUS FREQUENCY



AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	33MHz		VARIABLE CLOCK		UNITS
		MIN	MAX	MIN	MAX	
Oscillator Freq. (Ext. Osc.) (Ext. Crystal)	$1/t_{CLCL}$	0 1	33 33	0 1	33 33	MHz
ALE Pulse Width	t_{LHLL}	40		0.375 t_{MCS} -5		ns
Port 0 Address Valid to ALE Low	t_{AVLL}	9		0.125 t_{MCS} -5		ns
Address Hold after ALE Low	t_{LLAX1}	10		0.125 t_{MCS} -5		ns
ALE Low to Valid Instruction In	t_{LLIV}		60		0.625 t_{MCS} -20	ns
ALE Low to $\overline{\text{PSEN}}$ Low	t_{LLPL}	10		0.125 t_{MCS} -5		ns
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	55		0.5 t_{MCS} -5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In	t_{PLIV}		41		$0.5t_{MCS}$ -20	ns
Input Instruction Hold after $\overline{\text{PSEN}}$	t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$	t_{PXIZ}	26			$0.25t_{MCS}$ -5	ns
Port 0 Address to Valid Instruction In	t_{AVIV}	77			$0.75t_{MCS}$ - 20	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}	81			0.875 t_{MCS} -25	ns
$\overline{\text{PSEN}}$ Low to Address Float	t_{PLAZ}	0			0	ns

NOTES FOR AC ELECTRICAL CHARACTERISTICS

- t_{MCS} is a time period related to the machine cycle clock and the processor's input clock frequency. Its value is highlighted in the table "STRETCH VALUE TIMING" for all possible settings of the 4X/$\overline{2X}$ and CD1:0 bits. The default condition is CD1 = 1 and CD0 = 0, where 4X/$\overline{2X}$ is disregarded.
- All parameters apply to both commercial and industrial temperature operation unless otherwise noted. Electrical characterizations are not 100% tested but are guaranteed by design and characterization.
- All signals characterized with load capacitance of 80 pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ with 100 pF.
- Interfacing to memory devices with float times (turn off times) over 25 ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
- Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH VALUES C_{ST} (MD2:0)
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$0.375t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5		ns	C_{ST}=0 C_{ST}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Pulse Width	t_{RLRH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{WR}$ Pulse Width	t_{WLWH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$0.5t_{MCS}$-20 C_{ST}*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=7
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-15	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to Valid Data In	t_{LLDV}		$0.625t_{MCS}$-25 (C_{ST}+0.25)*t_{MCS}-40 (C_{ST}+1.25)*t_{MCS}-40	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to Valid Data In	t_{AVDV1}		$0.75t_{MCS}$-40 (C_{ST}+0.5)*t_{MCS}-27 (C_{ST}+1.5)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to Valid Data In	t_{AVDV2}		$0.875t_{MCS}$-20 (C_{ST}+0.5)*t_{MCS}-20 (C_{ST}+1.5)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.125t_{MCS}$-10 $0.25t_{MCS}$-10 $1.25t_{MCS}$-10	$0.125t_{MCS}$+5 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	$0.25t_{MCS}$-12 $0.5t_{MCS}$-12 $2.5t_{MCS}$-12		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$0.25t_{MCS}$-12 $0.5t_{MCS}$-12 $2.5t_{MCS}$-12		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5		ns	
Data Hold after Write	t_{WHQX}	$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Low to Address Float	t_{RLAZ}		-((0.125 t_{MCS})-5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-10 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10	18 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7

NOTES FOR MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES

- t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.
- C_{ST} is the stretch cycle value as determined by the MD2, MD1, & MD0 bits of the CKCON register.

t_{MCS} TIME PERIODS

System Clock Selection	t_{MCS}
4X/$\overline{2X}$, CD1, CD0 = 100	1 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = 000	2 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x10	4 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x11	1024 t_{CLCL}

$\overline{RD}$, $\overline{WR}$ PULSE WIDTH WITH STRETCH CYCLES

MD2	MD1	MD0	MOVX Machine Cycles	$\overline{RD}$, $\overline{WR}$ Pulse Width (in oscillator clocks)			
				4X/$\overline{2X}$=1 CD1:0=00	4X/$\overline{2X}$=0 CD1:0=00	4X/$\overline{2X}$=x CD1:0=10	4X/$\overline{2X}$=x CD1:0=11
0	0	0	2	0.5 t_{CLCL}	1 t_{CLCL}	2 t_{CLCL}	2048 t_{CLCL}
0	0	1	3	t_{CLCL}	2 t_{CLCL}	4 t_{CLCL}	4096 t_{CLCL}
0	1	0	4	2 t_{CLCL}	4 t_{CLCL}	8 t_{CLCL}	8192 t_{CLCL}
0	1	1	5	3 t_{CLCL}	6 t_{CLCL}	12 t_{CLCL}	12288 t_{CLCL}
1	0	0	9	4 t_{CLCL}	8 t_{CLCL}	16 t_{CLCL}	16384 t_{CLCL}
1	0	1	10	5 t_{CLCL}	10 t_{CLCL}	20 t_{CLCL}	20480 t_{CLCL}
1	1	0	11	6 t_{CLCL}	12 t_{CLCL}	24 t_{CLCL}	24576 t_{CLCL}
1	1	1	12	7 t_{CLCL}	14 t_{CLCL}	28 t_{CLCL}	28672 t_{CLCL}

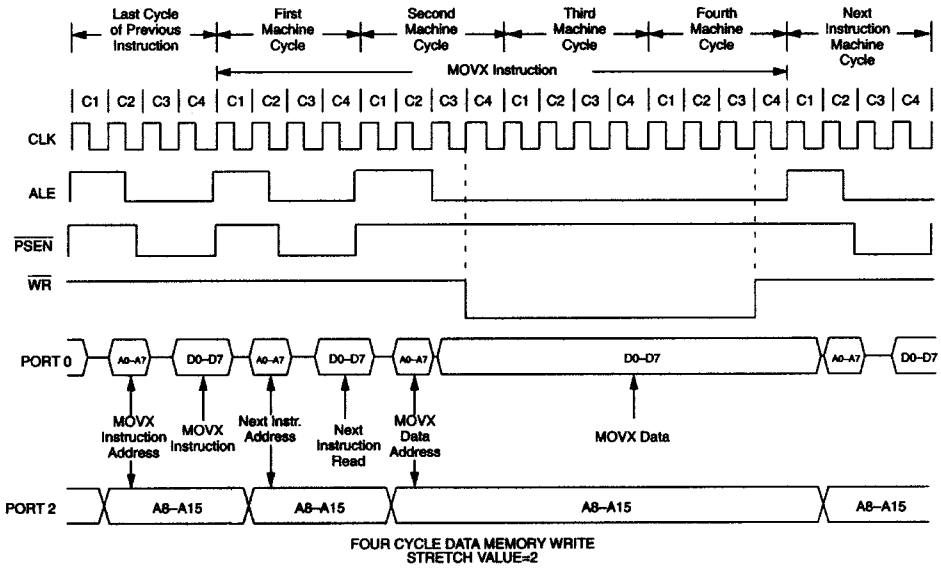
EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	10			ns	
Clock Low Time	t_{CLCX}	10			ns	
Clock Rise Time	t_{CLCL}			5	ns	
Clock Fall Time	t_{CHCL}			5	ns	

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

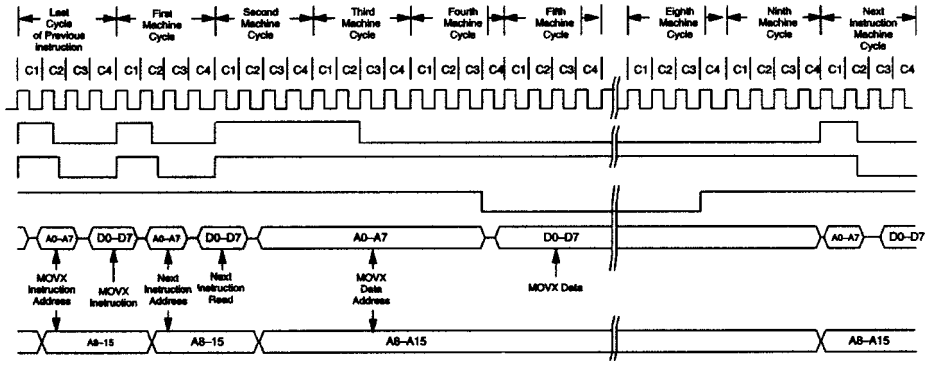
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHQX}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Input Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		 12t_{CLCL} 4t_{CLCL}		 ns ns	

DATA MEMORY WRITE WITH STRETCH=2

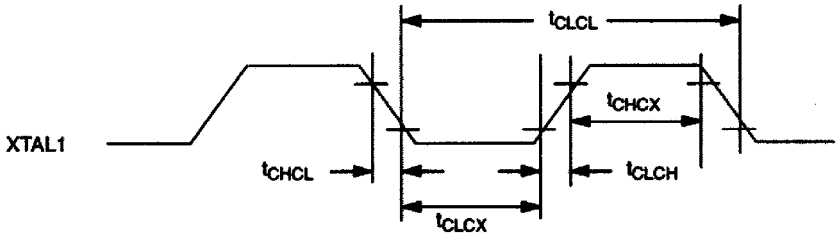


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

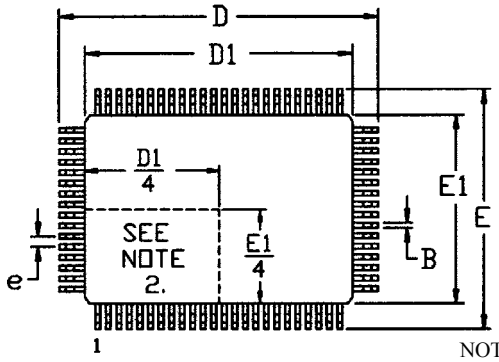
DATA MEMORY WRITE WITH STRETCH=4

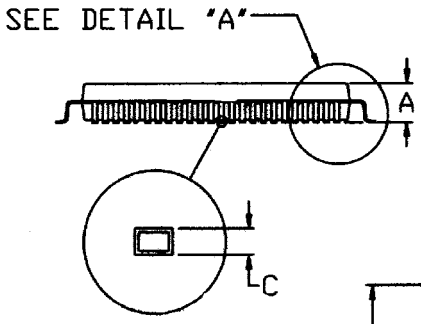


EXTERNAL CLOCK DRIVE



80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)

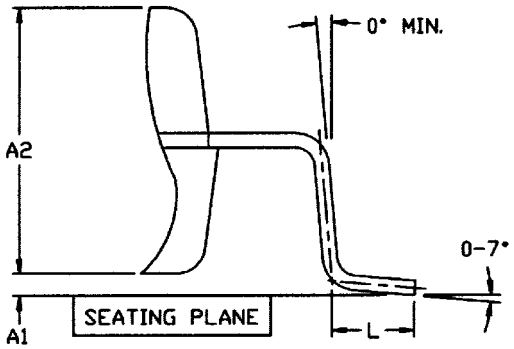




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSIONS; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.

DIM	MIN	MAX
A	-	3.40
A1	0.25	-
A2	2.55	2.87
B	0.30	0.45
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.70	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95



DETAIL A

DIMENSIONS ARE IN MILLIMETERS