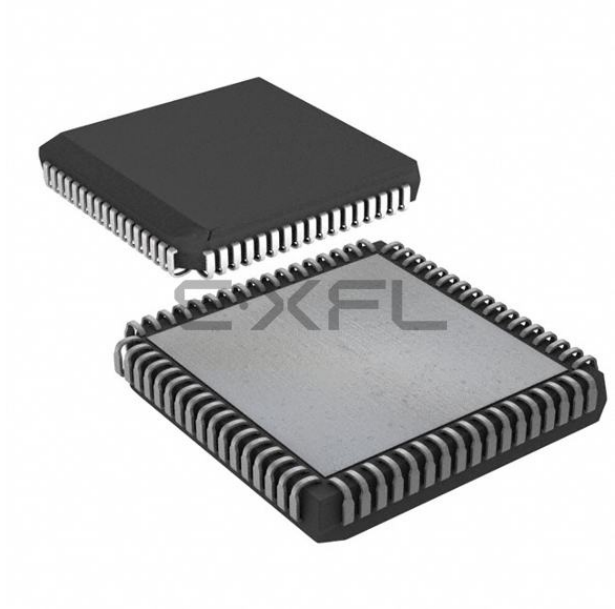
Analog Devices Inc./Maxim Integrated - DS87C550-QNL Datasheet



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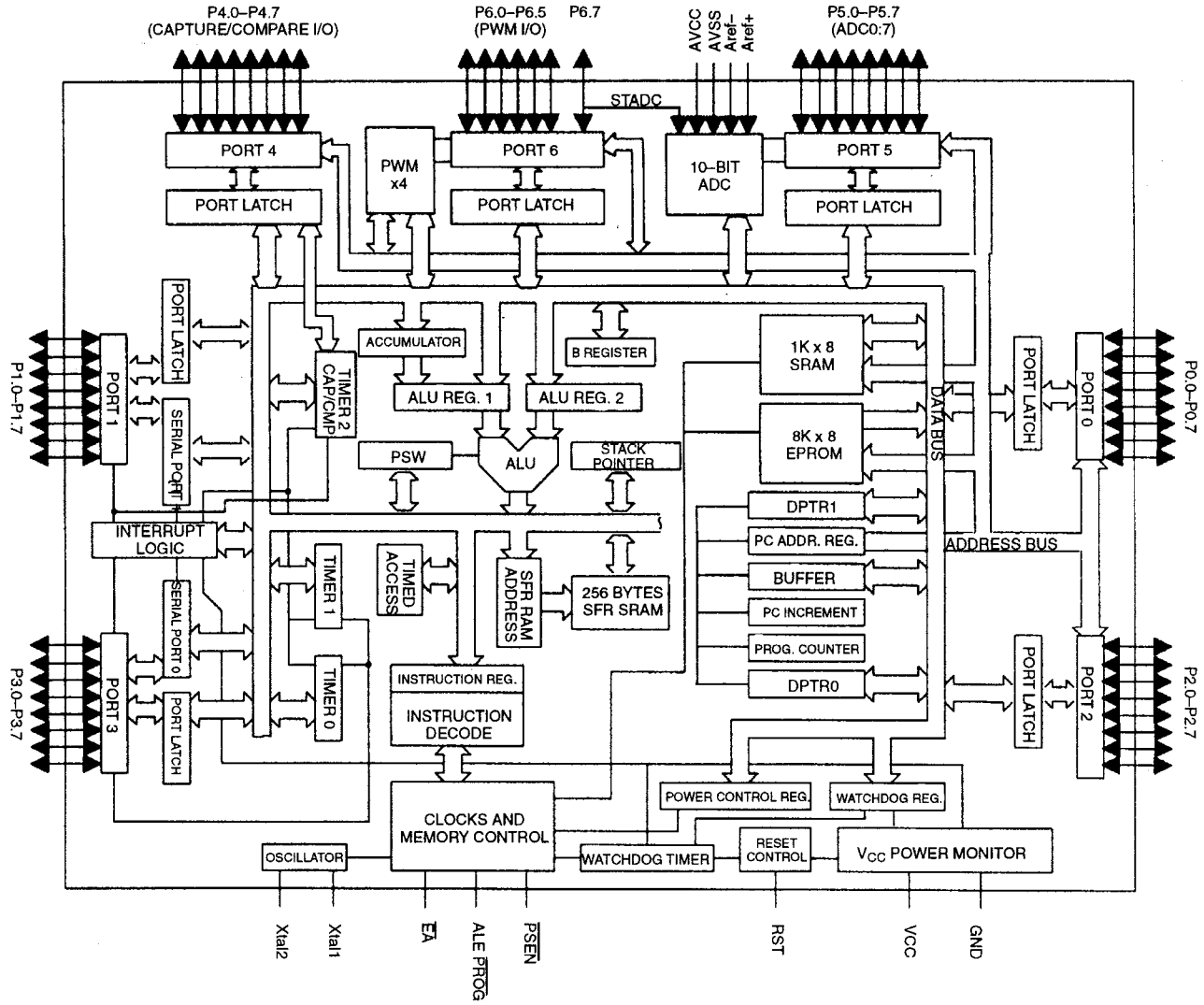
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, PWM, WDT
Number of I/O	55
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c550-qnl

DS87C550 BLOCK DIAGRAM Figure 1



PLCC/ CLCC	QFP	SIGNAL NAME	DESCRIPTION
1, 62-68	64-71	P5.0-P5.7	**Port 5 - I/O.** Port 5 functions as an open-drain 8-bit bi-directional I/O port or alternately as an interface to the A/D converter. When used for general purpose I/O, these pins operate in a quasi-bi-directional mode. Writing a logic 1 to these pins (reset condition) will cause them to tri-state. This allows the pins to serve as inputs since the tri-state condition can be overdriven by an external device. If a logic 0 is written to a pin, it is pulled down internally and therefore serves as an output pin containing a logic 0. Because these pins are open-drain, external pullup resistors are required to create a logic 1 level when they are used as outputs. As an alternate function Port 5 pins operate as the analog inputs for the A/D converter as described below. **Port Alternate Mode** P5.0 ADC0 Analog to Digital Converter input channel 0 P5.1 ADC1 Analog to Digital Converter input channel 1 P5.2 ADC2 Analog to Digital Converter input channel 2 P5.3 ADC3 Analog to Digital Converter input channel 3 P5.4 ADC4 Analog to Digital Converter input channel 4 P5.5 ADC5 Analog to Digital Converter input channel 5 P5.6 ADC6 Analog to Digital Converter input channel 6 P5.7 ADC7 Analog to Digital Converter input channel 7
1 68 67 66 65 64 63 62	71 70 69 68 67 66 65 64		
3-6, 32 33, 38	28, 29 37 74-77	P6.0-P6.5 P6.7	**Port 6 - I/O.** Port 6 functions as a 7-bit bi-directional I/O port or alternately as an interface to the PWM and A/D on-board peripherals. As an I/O port, these pins operate as described in Port 1. Note that P6.6 is not implemented. The alternate modes of Port 6 are detailed below. **Port Alternate Function** P6.0 PWMO0 PWM channel 0 output P6.1 PWMO1 PWM channel 1 output P6.2 PWMO2 PWM channel 2 output P6.3 PWMO3 PWM channel 3 output P6.4 PWMC0 PWM0 clock input P6.5 PWMC1 PWM1 clock input P6.7 STADC External A/D conversion start signal (active low)
4 5 32 33 6 38 3	75 76 28 29 77 37 74		
59	60	A_{vref+}	**A/D +Reference -** Input. Supplies the positive reference voltage for the A/D converter. This signal should be isolated from digital V_{CC} to prevent noise from affecting A/D measurements.
58	59	A_{vref-}	**A/D -Reference -** Input. Supplies the negative reference voltage for the A/D converter. This signal should be isolated from digital GND to prevent noise from affecting A/D measurements.
61	63	A_{VCC}	**Analog V_{CC}**
60	61	A_{VSS}	**Analog Ground**
	3, 21 22, 30 33, 36 43, 44 62, 73 78, 79	NC	**NC-Reserved.** These pins should not be connected. They are reserved for use with future devices in this family.

instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C550, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles, but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C550 usually uses one instruction cycle for each instruction byte. Examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High Speed Micro User's Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C550. This allows the DS87C550 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C550 duplicates the SFRs contained in the standard 80C52. Table 2 shows the register addresses and bit locations. Many are standard 80C52 registers. The High Speed Micro User's Guide describes all SFRs in full detail.

SPECIAL FUNCTION REGISTER LOCATION: Table 2

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
PORT0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	ID1	ID0	TSL	-	-	-	-	SEL	86h
PCON	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
RCON	-	-	-	-	CKRDY	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PMR	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEOFF	DEM1	DME0	9Fh
PORT2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
SADDR0									A1h
SADDR1									A2h
IE	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	A8h
CMPL0									A9h
CMPL1									AAh
CMPL2									ABh
CPTL0									ACh
CPTL1									ADh
CPTL2									AEh
CPTL3									AFh
PORT3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
ADCON1	STRT/BSY	EOC	CONT/SS	ADEX	WCQ	WCM	ADON	WCIO	B2h

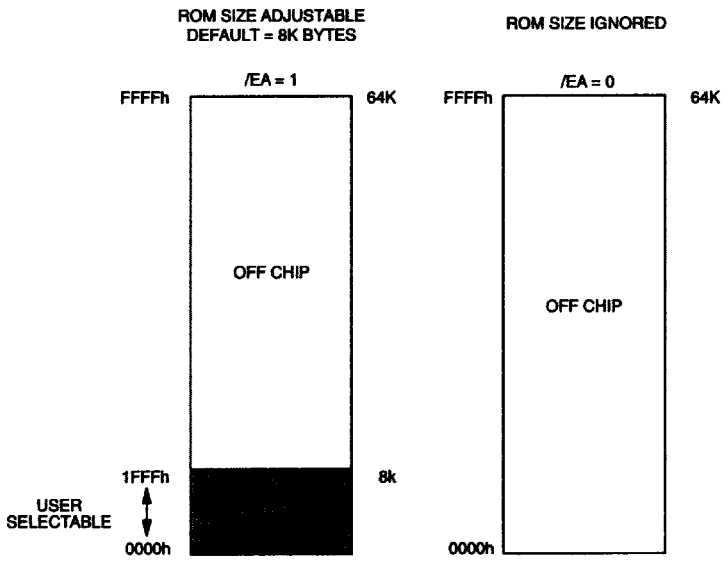
SPECIAL FUNCTION REGISTER LOCATION: Table 2 continued

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
ADCON2	OUTCF	MUX2	MUX1	MUX0	APS3	APS2	APS1	APS0	B3h
ADMSB									B4h
ADLSB									B5h
WINHI									B6h
WINLO									B7h
IP	-	PAD	PS1	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	$\overline{RL2}$	BEh
T2MOD	-	-	-	-	-	-	T2OE	DCEN	BFh
PORT4	CMT1	CMT0	CMSR5	CMSR4	CMSR3	CMSR2	CMSR1	CMSR0	C0h
ROMSIZE	-	-	-	-	-	RMS2	RMS1	RMS0	C2h
PORT5	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	C4h
STATUS	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA									C7h
T2IR	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF1	IE2/CF0	C8h
CMPH0									C9h
CMPH1									CAh
CMPH2									CBh
CPTH0									CCh
CPTH1									CDh
CPTH2									CEh
CPTH3									CFh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
PW0FG									D2h
PW1FG									D3h
PW2FG									D4h
PW3FG									D5h
PWMADR	ADRS	-	-	-	-	-	PWE1	PWE0	D6h
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	D8h
SBUF1									D9h
PWM0									DCh
PWM1									DDh
PWM2									DEh
PWM3									DFh
ACC									E0h
PW01CS	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN	E1h
PW23CS	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN	E2h
PW01CON	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C	E3h
PW23CON	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C	E4h
RLOADL									E6h
RLOADH									E7h
EIE	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EX1	EX2/EC0	E8h
T2SEL	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0	EAh
CTCON	$\overline{CT3}$	CT3	$\overline{CT2}$	CT2	$\overline{CT1}$	CT1	$\overline{CT0}$	CT0	EBh
TL2									ECh
TH2									EDh
SETR	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0	EEh
RSTR	CMTE1	CMTE0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	EFh
B									F0h
PORT6	STADC	-	PWMC1	PWMC0	PWMO3	PWMO2	PWMO1	PWMO0	F1h
EIP	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0	F8h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	FFh

ROM address of 5k. This would cause the current address to switch from internal to external and potentially cause invalid operation. Similarly, do not instantly switch from external to internal memory. For example, do not select a maximum ROM address of 8kB from an external ROM address of 7kB (if ROMSIZE is set for 4kB or less).

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not available as I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the EA pin is logic 0. EA overrides all bit settings. The PSEN signal will go active (low) to serve as a chip enable or output enable when Ports 0 & 2 fetch from external ROM.

ROM MEMORY MAP Figure 2



DATA MEMORY

Unlike many 8051 derivatives, the DS87C550 contains additional on-chip data memory. In addition to the standard 256 bytes of data RAM accessed by direct instructions, the DS87C550 contains another 1kB of data memory that is accessed using the MOVX instruction. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is permanently located from address 0000h to 03FFh (when enabled).

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 1kB automatically go to external memory through Ports 0 & 2.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 & 2. This also is the default condition. This default allows the DS87C550 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using two bits in the Power Management Register (DME1, DME0). This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. These bits have the following operation:

Another useful feature of the device is its ability to automatically switch the active data pointer after a DPTR-based instruction is executed. This feature can greatly reduce the software overhead associated with data memory block moves, which toggle between the source and destination registers. When the Toggle Select bit (TSL;DPS.5) is set to 1, the SEL bit (DPS.0) is automatically toggled every time one of the following DPTR related instructions are executed:

- INC DPTR
- MOV DPTR, #data16
- MOVC A, @A+DPTR
- MOVX A, @DPTR
- MOVX @DPTR, A

As a brief example, if TSL is set to 1, then both data pointers can be updated with the two instruction series shown.

```
INC DPTR
INC DPTR
```

With TSL set, the first increment instruction increments the active data pointer, and then causes the SEL bit to toggle making the other DPTR active. The second increment instruction increments the newly active data pointer and then toggles SEL to make the original data pointer active again.

CLOCK CONTROL and POWER MANAGEMENT

The DS87C550 includes a number of unique features that allow flexibility in selecting system clock sources and operating frequencies. To support the use of inexpensive crystals while allowing full-speed operation, a clock multiplier is included in the processor's clock circuit. Also, along with the Idle and power-down (Stop) modes of the standard 80C52, the DS87C550 provides a new Power Management mode. This mode allows the processor to continue instruction execution at a very low speed to significantly reduce power consumption (below even idle mode). The DS87C550 also features several enhancements to Stop mode that make this extremely low power mode more useful. Each of these features is discussed in detail below.

SYSTEM CLOCK CONTROL

As mentioned previously, the DS87C550 contains special clock control circuitry that simultaneously provides maximum timing flexibility and maximum availability and economy in crystal selection. There are two basic functions to this circuitry: a frequency multiplier and a clock divider. By including a frequency multiplier circuit, full-speed operation of the processor may be achieved with a lower frequency crystal. This allows the user the ability to choose a more cost-effective and easily obtainable crystal than would be possible otherwise.

The logical operation of the system clock divide control function is shown in Figure 3. The clock signal from the crystal oscillator (or external clock source) is provided to the frequency multiplier module, to a divide-by-256 module, and to a 3-to-1 multiplexer. The output of this multiplexer is considered the **system clock**. The system clock provides the time base for timers and internal peripherals, and feeds the CPU State Clock Generation circuitry. This circuitry divides the system clock by 4, and it is the four phases of this clock that make up the instruction execution clock. The four phases of a single instruction execution clock are also called a single **machine cycle clock**. Instructions in the DS87C550 all use the machine cycle as the fundamental unit of measure and are executed in from one to five of these machine

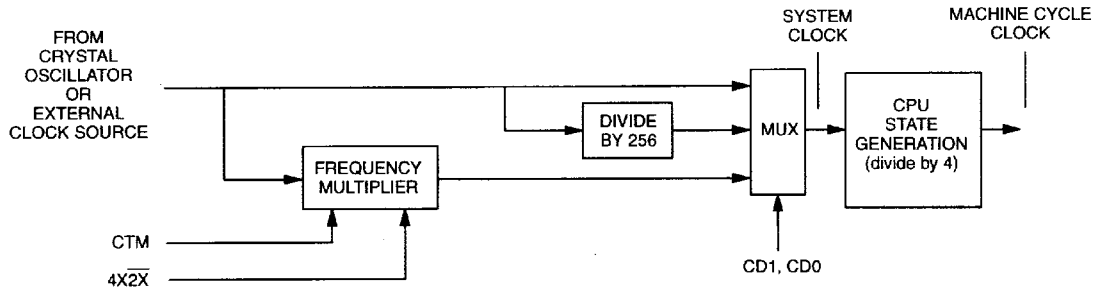
CLOCK SWITCHING RESTRICTIONS

To ensure clean "glitch-free" switching of the system clock and to ensure that all clocks are running and stable before they are used, there are minor restrictions on accessing the clock selection bits CD1:0 and the 4X/$\overline{2X}$ bit.

One restriction is that any change in the CD1 and CD0 bits from a condition other than a 1 0 state (i.e., clock divided by 4 mode) must pass through the divide-by-4 state before proceeding to the desired state. As a specific example, if the clock divisor bits are set to use the frequency multiplier in 4X mode, no other clock setting is possible until after the CD1:0 bits are set to divide-by-4 mode. After setting clock divided-by-4 mode, then clock divided by 1024 can be selected by setting CD1 and CD0 to "11b". Any attempt to change these bits to a disallowed state will be ignored by the hardware.

There are also some minor restrictions when changing from one clock multiplier to another. Changing the clock multiplier can only be performed when the Crystal Multiplier Enable bit CTM (PMR.4) is set to 0. This bit disables the clock multiplication function. However, the CTM bit can only be changed when CD1 and CD0 are set to divide-by-4 mode (i.e., "10b") and the ring mode (RNGMD = RCON.2) bit is 0 (discussed later). Changing the clock multiplication factor also requires that the new frequency be stable prior to effecting the change. The SFR bit CKRDY (RCON.3) indicates the state of the stabilization timeout. Setting the CTM bit to a 0 from a 1 disables the clock multiplier function, automatically clears the CKRDY bit, and starts the stabilization timeout.

SYSTEM CLOCK CONTROL Figure 3



During the stabilization period, CKRDY will remain low, and software will be unable to set the CD1:0 bits to select the frequency multiplier. After the stabilization delay, CKRDY will be set to a 1 by hardware. Note that this bit cannot be set to 1 by software. After hardware sets CKRDY bit, then the CD1:0 bits can be set to use the clock multiplier function. However, before changing CD1:0, the 4X/$\overline{2X}$ bit must be set to the desired state. Following this, the CTM bit must be set to 1 to enable the crystal multiplier. Finally the CD1:0 bits may be set to select the crystal multiplier function. By following this procedure, the processor is guaranteed to receive a stable, glitch-free clock.

OSCILLATOR-FAIL DETECT

The DS87C550 contains a unique safety mechanism called an on-chip Oscillator-Fail Detect circuit. When enabled, this circuit causes the processor to be reset if the oscillator frequency falls below 40kHz. The processor is held in reset until the oscillator frequency rises above 40kHz. In operation, this circuit can provide a backup for the watchdog timer. Normally, the watchdog timer is initialized so that it will timeout and will cause a processor reset in the event that the processor loses control. This works perfectly as long as there is a clock from the crystal or external oscillator, but if this clock fails, there is the potential for the processor to fail in an uncontrolled and possibly undesirable state. With the use of the

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The DS87C550 allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to a 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain inactive when performing on-chip memory access. The default state is ALEOFF = 0 so ALE normally toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C550 provides several of the most commonly needed peripheral functions in microcomputer-based systems. New functions include a second serial port, power-fail reset, power-fail interrupt flag, and a programmable watchdog timer. In addition, the DS87C550 contains an analog-to-digital converter and four channels of pulse width modulation for industrial control and measurement applications. Each of these peripherals is described below. More details are available in the *High-Speed Microcontroller User's Guide: DS87C550 Supplement*.

SERIAL PORTS

The DS87C550 provides a serial port (UART) that is identical to the 80C52. In addition, it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.6 (RXD1) and P1.7 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1, SBUF1) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

Control for serial port 0 is provided by the SCON0 register while its I/O buffer is SBUF0. The registers SCON1 and SBUF1 provide the same functions for the second serial port. A full description of the use and operation of both serial ports may be found in the *High-Speed Microcontroller User's Guide*, available from the Maxim website.

ANALOG TO DIGITAL CONVERTER

The DS87C550 contains a 10-bit successive approximation analog-to-digital converter. This converter provides eight multiplexed channels of analog input using an external voltage reference for the conversion process.

Before using the A/D converter, the converter must be configured by performing two actions:

1. The user must set the ADON bit (ADCON1.1). This enables the A/D converter. This bit defaults to 0 following a reset, disabling the A/D converter to conserve power.
2. In addition, the user must set the ADRS bit (PWMADR.7) to enable the external voltage reference pins. This bit defaults to 0 following a reset, disabling the A/D converter voltage reference pins.

A/D CONVERTER INPUTS

The A/D converter of the DS87C550 provides eight channels of analog input on device pins ADC7 through ADC0 (P5.7-P5.0). The signals on these pins are input into an analog multiplexer. The magnitude (and polarity) of these signals is limited by the external reference (A_{VREF+}, A_{VREF-}) voltages used by the converter. See the DC electrical characteristics section of this data sheet for more details.

PULSE WIDTH MODULATION

The DS87C550 contains four independent 8-bit pulse width modulator (PWMs) functions each with independently selectable clock sources. For more precise modulation operations, two 8-bit PWM functions (PWM0 & PWM1 and/or PWM2 & PWM3) can be cascaded together to form a 16-bit PWM function.

The PWM function is divided into three major blocks: a clock prescaler, a clock generator, and a pulse generator. A single prescaler provides selectable clocks of different frequencies to each of the four clock generator blocks. Each clock generator is an 8-bit reloadable counter that determines the repetition rate (frequency) of its associated PWM. Each pulse generator PWM block is an 8-bit timer clocked by the clock generator's output. When this timer reaches zero, the output of the PWM is set to 1. When the timer reaches the user selected PWM match value stored in SFR PWMx, the PWM output is cleared to 0. In this way, the frequency and duty cycle of the PWM is varied under software control.

PWM PRESCALER

The prescaler block of the PWM function accepts as a clock input the system clock provided to the CPU (and other peripherals), and divides it by 1, 4, 16, and 64. Each of these clocks is available at the output of the prescaler, and is provided to all four of the PWM clock generator blocks. The actual clock used by the clock generator block is dependant on the setting of SFR bits PWxS2:0 (where x is the PWM channel number 0-3) located in the PW01CS or PW23CS registers. In addition to selecting one of the prescaler's CPU clock divided outputs, setting PWxS2 to a 1 allows an external clock to be used as an input to the clock generators. The external clocks are input on device pins PWMC0 (P6.4 for PWM0 or PWM1) or PWMC1 (P6.5 for PWM2 or PWM3). Like all other inputs to the 8051, these inputs are synchronized by sampling them using the internal machine cycle clock. Therefore these inputs must be of sufficient duration for the clock to sample them properly (i.e., 2 machine cycles). The complete functionality of the clock selection SFR bits is as follows:

Prescaler Output	**PWxS2:0**
Machine Cycle_Clock/1	000
Machine Cycle_Clock/4	001
Machine Cycle_Clock/16	010
Machine Cycle_Clock/64	011
PWMCx (external)	1xx

In determining the exact frequency output of the prescaler, it is important to note that the machine cycle clock provided to the prescaler is also software-selectable. The machine cycle clock can be the crystal (or oscillator frequency) divided by 1, 2, 4, or 1024 as determined by the CD1:0 and the 4X/$\overline{2X}$ SFR bits (see Clock Divide Control section for details).

PWM CLOCK GENERATOR

The clock generator blocks of the PWM modules are pre-loaded by software with an 8-bit value, and this value determines the frequency or repetition rate of the PWM function. A value of 0 causes the selected output of the prescaler to be passed directly to the pulse generator function (i.e., divide by 1). A value of FFh passes a clock to the pulse generator function that is the selected prescaler output divided by 256. In general, the clock generators provide a divide by N+1 selectable repetition rate (i.e., frequency) for their PWM channel.

Each clock generator has an associated SFR that contains the 8-bit reload value. These registers are called PW0FG, PW1FG, PW2FG, and PW3FG (see SFR map for addresses). In addition, there is a frequency generator enable bit (PW0EN, PW1EN, PW2EN, & PW3EN) for each of the clock generator blocks that must be set to a 1 before these blocks will function. These bits are set to 0 after all resets so software must set them to 1 to enable the PWM clocks.

The output of the clock generator block is supplied to the input of the pulse generator block.

PWM PULSE GENERATOR

The pulse generator block of the PWM function produces the PWM output signal on device pins PWMO0 (P6.0), PWMO1(P6.1), PWMO2 (P6.2), and PWMO3 (P6.3). Each of these output bits has an enable bit: PW0OE (PW01CON.5), PW1OE (PW01CON.1), PW2OE (PW23CON.5), and PW3OE (PW23CON.1) that are cleared to 0 on all resets, and must be set to 1 by software before the PWMs will output a signal.

As described earlier, the pulse generator block is basically a free-running timer with a comparison register that is loaded with an 8-bit value by software. The value of this register establishes the duty cycle of the PWM function. The comparison values are stored in SFRs PWM0, PWM1, PWM2, and PWM3 for the respective PWM channels, and it is these values that determine the pulse duration.

Actually, in accessing these specific SFRs, software has access to both the compare registers and the timer registers of the pulse generator blocks. When the PWM Timer/Compare Value Select SFR bits PW0T/C (PW01CON.4), PW1T/C (PW01CON.0), PW2T/C (PW23CON.4), and PW3T/C (PW23CON.0) are cleared to 0, a read or write to the respective PWMx register accesses the compare register. When these bits are set to 1, a read or write accesses the timer value. With the use of these bits, the timers in the pulse generator sections of the PWM functions can be used as general-purpose timers if desired.

When the free-running timer of the pulse generator block rolls over from FFh to 00h, the PWM output is set to a 1. As the timer continues to count up from 0, the output of the PWM is cleared to 0 when the timer value is equal to the comparison register value. This cycle continues automatically without processor intervention until software or a reset changes some condition.

The value of 0 in the comparison register is a special case of each PWM function. Rather than allow a set and a reset of the PWM output bit, special hardware ensures that 0 will be output continuously if 0 is loaded into the compare register.

There are other SFR bits that affect PWM operation for special modes. Bits PW0DC (PW01CON.6), PW1DC (PW01CON.2), PW2DC (PW23CON.6), and PW3DC (PW23CON.2) cause the output of the respective PWM function to be a constant 1. This feature may be useful for driving a fixed DC voltage into any circuitry attached to the PWM output. Bits PW0F (PW01CON.7), PW1F (PW01CON.3), PW2F (PW23CON.7), and PW3F (PW23CON.3) are flags that are set by the hardware when the respective PWM pulse generator timer rolls over from FFh to 0. These flags must be cleared by software to remove their set condition.

16-BIT MODE

For more precise PWM operations, two 8-bit PWMs may be combined into a single 16-bit PWM function. By setting SFR bit PWE0 (PWMADR.0) to a 1, a new 16-bit PWM0 function is formed from the 8-bit PWM functions PWM0 (LSB) and PWM1 (MSB). Similarly, by setting PWE1 (PWMADR.1) to

The three available priority levels are low, high, and highest. The highest priority level is reserved for the Power-Fail Interrupt only. All other interrupt priority levels have individual priority bits that when set to a 1 establish the particular interrupt as high priority. In addition to the user selectable priorities, each interrupt also has an inherent or "natural priority". Given that all interrupt sources maintain the default low priority, the natural priority determines the priority of simultaneously occurring interrupts. Table 9 identifies the available interrupt sources and their flags, enables, natural priority, and available priority selection bits.

INTERRUPT SOURCES AND PRIORITIES Table 9

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY	FLAG BIT	ENABLE BIT	PRIORITY CONTROL BIT
PFI	Power Fail Interrupt	33h	0	PFI(WDCON.4)	EPFI(WDCON.5)	N/A
$\overline{\text{INT0}}$	External Interrupt 0	03h	1	IEO(TCON.1)	EX0(IE.0)	PX0(IP.0)
SCON1	TI1 or RI1 from serial port 1	0Bh	2	RI_1(SCON1.0) TI_1(SCON1.1)	ES1(IE.5)	PS1(IP.5)
A/D	A/D Converter Interrupt	13h	3	EOC(ADCON1.6)	EAD(IE.6)	PAD(IP.6)
TF0	Timer 0	1Bh	4	TF0(TCON.5)	ET0(IE.1)	PT0(IP.1)
INT2/CF0	External Interrupt 2 or Capture 0	23h	5	IE2/CF0(T2IR.0)	EX2/EC0(EIE.0)[1]	PX2/PC0(EIP.0)
CM0F	Compare Match 0	2Bh	6	CM0F(T2IR.4)	ECM0(EIE.4)	PCM0(EIP.4)
$\overline{\text{INT1}}$	External Interrupt 1	3Bh	7	IE1(TCON.3)	EX1(IE.2)	PX1(IP.2)
INT3/CF1	External Interrupt 3 or Capture 1	43h	8	IE3/CF1(T2IR.1)	EX3/EC1(EIE.1)[1]	PX3/PC1(EIP.1)
CM1F	Compare Match 1	4Bh	9	CM1F(T2IR.5)	ECM1(EIE.5)	PCM1(EIP.5)
TF1	Timer 1	53h	10	TF1(TCON.7)	ET1(IE.3)	PT1(IP.3)
INT4/CF2	External Interrupt 4 or Capture 2	5Bh	11	IE4/CF2(T2IR.2)	EX4/EC2(EIE.2)[1]	PX4/PC2(EIP.2)
CM2F	Compare Match 2	63h	12	CM2F(T2IR.6)	ECM2(EIE.6)	PCM2(EIP.6)
SCON0	TI0 or RI0 from serial port 0	6Bh	13	RI_0(SCON0.0) TI_0(SCON0.1)	ES0(IE.4)	PS0(IP.4)
INT5/CF3	External Interrupt 5 or Capture 3	73h	14	IE5/CF3(T2IR.3)	EX5/EC3(EIE.3)[1]	PX5/PC3(EIP.3)
TF2	Timer 2	7Bh	15	TF2(TCON.7) TF2B(T2SEL.4)	ET2(EIE.7)	PT2(EIP.7)

[1] External interrupts 2/3/4/5 also require the appropriate bits in the CTCON register to be configured before the interrupt is fully enabled.

EPROM PROGRAMMING

The DS87C550 follows 8kB EPROM standards for the 8051 family. It is available in a UV erasable, ceramic windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options.

PROGRAMMING PROCEDURE

The DS87C550 should run from a clock speed between 4 and 6MHz when programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 10. The diagram in Figure 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the Electrical Specifications.

unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 10. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

EPROM ERASURE CHARACTERISTICS

Erasure of the information stored in the DS87C550's EPROM occurs when the isolated gate structure of the EPROM stage element is exposed to certain wavelengths of light. While the gate structure is to some degree sensitive to a wide range of wavelengths, it is mostly wavelengths shorter than approximately 4,000 angstroms that are most effective in erasing the EPROM. Since fluorescent lighting and sunlight have wavelengths in this range, they can cause erasure if the device is exposed to them over an extended period of time (weeks for sunlight, years in room-level fluorescent light). For this reason (and others mentioned previously), it is recommended that an opaque covering be placed over the window of the -K (windowed PLCC) package type.

For complete EPROM erasure, exposure to ultraviolet light at approximately 2537 angstroms to a dose of 15W-sec/cm^2 at minimum is recommended. In practice, exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes at a distance of approximately 1 inch will normally be sufficient.

OTHER EPROM OPTIONS

The DS87C550 has user-selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

The EPROM selectable options may be programmed as shown in Table 10. The Option Register sets or reads these selections. The bits in the Option Register have the following function:

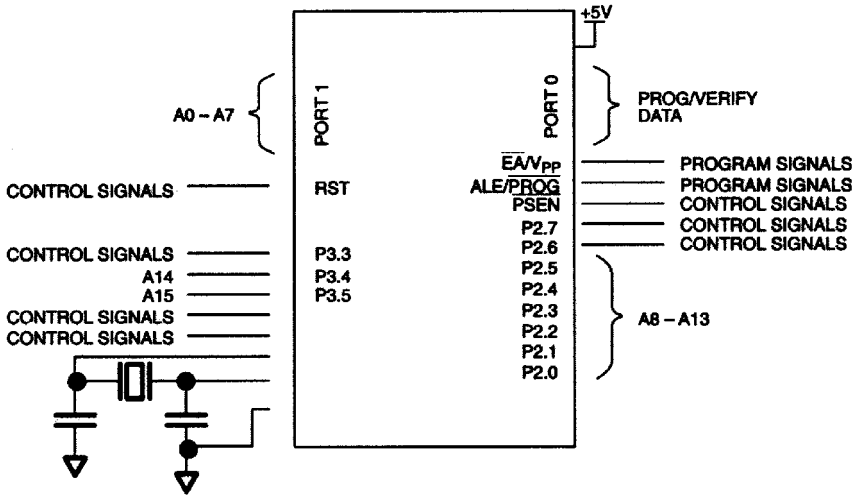
Bit 7 -4 Reserved. Program to a 1.
Bit 3 Watchdog POR default.
Set to 1: Watchdog reset function is disabled on power-up.
Set to 0: Watchdog reset function is enabled automatically on power up.
Bit 2-0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is located at programming addresses 30h, 31h, and 60h. This information is as follows:

Address	Value	Meaning
30h	DAh	Manufacturer
31h	55	Model
60h	00	Extension

EPROM PROGRAMMING CONFIGURATION Figure 5



NOTES FOR DS87C550 DC ELECTRICAL CHARACTERISTICS:

All parameters apply to both commercial and industrial temperature operation unless otherwise noted. These parameters are guaranteed by design.

1. Voltage referenced to digital ground (GND).

2. Active current measured with 33MHz clock source on XTAL1, V_{CC}=RST=5.5V, other pins disconnected.

3. Idle mode current measured with 33MHz clock source on XTAL1, V_{CC}=5.5V, RST at ground, other pins disconnected.

4. Stop mode current measured with XTAL1 and RST grounded, V_{CC}=5.5V, all other pins disconnected. This value is not guaranteed. Users that are sensitive to this specification should contact Dallas Semiconductor for more information.

5. When addressing external memory.

6. RST=V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

7. During a 0 to 1 transition, a one-shot drives the ports hard for two oscillator clock cycles. This measurement reflects port in transition mode.

8. Ports 1, 2, 3, 5, 6 source transition current when being pulled down externally. Current reaches its maximum at approximately 2V.

9. 0.45<V_{IN}<V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

10. 0.45< V_{IN} <V_{CC}. RST=V_{CC}. This condition mimics operation of pins in I/O mode.

11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

A/D CONVERTER ELECTRICAL CHARACTERISTICS

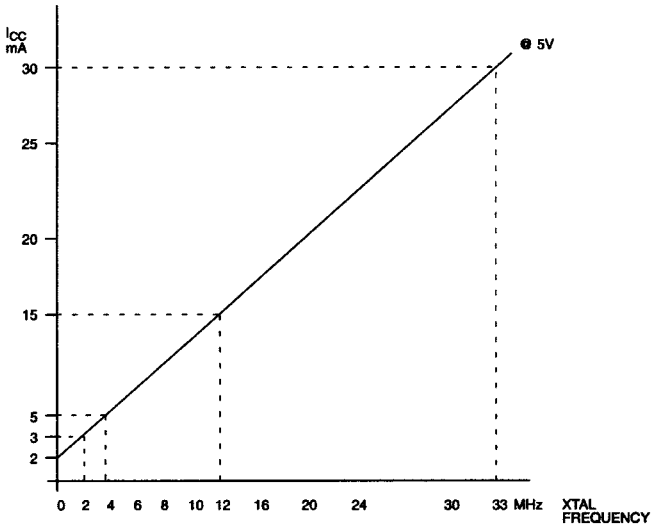
(AV_{CC}=V_{CC}=5V, V_{REF}=5V, f_{OSC}=4MHz, T_A=-40°C to 85°C, unless otherwise noted. Typical values are at T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Analog Supply Voltage	A_{VCC} A_{VSS}	V_{CC} GND		V_{CC} GND	V	
Analog Supply Current	AI_{DD}		0.7	2.3	mA	
Analog Idle Mode Current	AI_{DDI}			3.5	mA	
Analog Power-Down Mode Current	AI_{DDPD}		0.5	1	µA	
Analog Input Voltage	ADC7- ADC0	A_{VREF-}		A_{VREF+}	V	4
External Analog Reference Voltage	A_{VREF-} A_{VREF+}	AV_{SS}-0.2		AV_{CC} + 0.2	V	4
Analog Input Capacitance	C_{IN}		10	15	pF	4
A/D Clock	t_{ACLK}	1		6.25	µs	2, 4
Sampling Time	t_{ADS}	5 t_{ACLK}			t_{ACLK}	4
Conversion Time	t_{ADC}	16 t_{ACLK}			t_{ACLK}	3, 4
Resolution		10			Bits	4
Differential non-linearity	E_{DL}			±1.0	LSB	
Integral non-linearity	E_{IL}			±2.0	LSB	
Offset Error	E_{OS}			±2.0	LSB	
Gain Error	E_G			±1.0	%	
Cross-talk between A/D inputs	E_{CT}		-60		dB	4

NOTES FOR A/D CONVERTER ELECTRICAL CHARACTERISTICS

1. The following condition must not be exceeded: GND-0.2V < AV_{SS} < V_{CC} + 0.2V.
2. Due to the dynamic nature of the A/D converter, t_{ACLK} has both min and max specifications.
3. A complete conversion cycle requires 16 ACLK periods, including five input sampling periods.
4. This parameter is guaranteed by design.

TYPICAL I_{CC} VERSUS FREQUENCY



MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH VALUES C_{ST} (MD2:0)
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$0.375t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5		ns	C_{ST}=0 C_{ST}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Pulse Width	t_{RLRH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{WR}$ Pulse Width	t_{WLWH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$0.5t_{MCS}$-20 C_{ST}*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=7
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-15	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to Valid Data In	t_{LLDV}		$0.625t_{MCS}$-25 (C_{ST}+0.25)*t_{MCS}-40 (C_{ST}+1.25)*t_{MCS}-40	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to Valid Data In	t_{AVDV1}		$0.75t_{MCS}$-40 (C_{ST}+0.5)*t_{MCS}-27 (C_{ST}+1.5)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to Valid Data In	t_{AVDV2}		$0.875t_{MCS}$-20 (C_{ST}+0.5)*t_{MCS}-20 (C_{ST}+1.5)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.125t_{MCS}$-10 $0.25t_{MCS}$-10 $1.25t_{MCS}$-10	$0.125t_{MCS}$+5 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	$0.25t_{MCS}$-12 $0.5t_{MCS}$-12 $2.5t_{MCS}$-12		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$0.25t_{MCS}$-12 $0.5t_{MCS}$-12 $2.5t_{MCS}$-12		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5		ns	
Data Hold after Write	t_{WHQX}	$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Low to Address Float	t_{RLAZ}		-((0.125 t_{MCS})-5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-10 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10	18 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7

NOTES FOR MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES

- t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.
- C_{ST} is the stretch cycle value as determined by the MD2, MD1, & MD0 bits of the CKCON register.

t_{MCS} TIME PERIODS

System Clock Selection	t_{MCS}
4X/$\overline{2X}$, CD1, CD0 = 100	1 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = 000	2 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x10	4 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x11	1024 t_{CLCL}

$\overline{RD}$, $\overline{WR}$ PULSE WIDTH WITH STRETCH CYCLES

MD2	MD1	MD0	MOVX Machine Cycles	$\overline{RD}$, $\overline{WR}$ Pulse Width (in oscillator clocks)			
				4X/$\overline{2X}$=1 CD1:0=00	4X/$\overline{2X}$=0 CD1:0=00	4X/$\overline{2X}$=x CD1:0=10	4X/$\overline{2X}$=x CD1:0=11
0	0	0	2	0.5 t_{CLCL}	1 t_{CLCL}	2 t_{CLCL}	2048 t_{CLCL}
0	0	1	3	t_{CLCL}	2 t_{CLCL}	4 t_{CLCL}	4096 t_{CLCL}
0	1	0	4	2 t_{CLCL}	4 t_{CLCL}	8 t_{CLCL}	8192 t_{CLCL}
0	1	1	5	3 t_{CLCL}	6 t_{CLCL}	12 t_{CLCL}	12288 t_{CLCL}
1	0	0	9	4 t_{CLCL}	8 t_{CLCL}	16 t_{CLCL}	16384 t_{CLCL}
1	0	1	10	5 t_{CLCL}	10 t_{CLCL}	20 t_{CLCL}	20480 t_{CLCL}
1	1	0	11	6 t_{CLCL}	12 t_{CLCL}	24 t_{CLCL}	24576 t_{CLCL}
1	1	1	12	7 t_{CLCL}	14 t_{CLCL}	28 t_{CLCL}	28672 t_{CLCL}

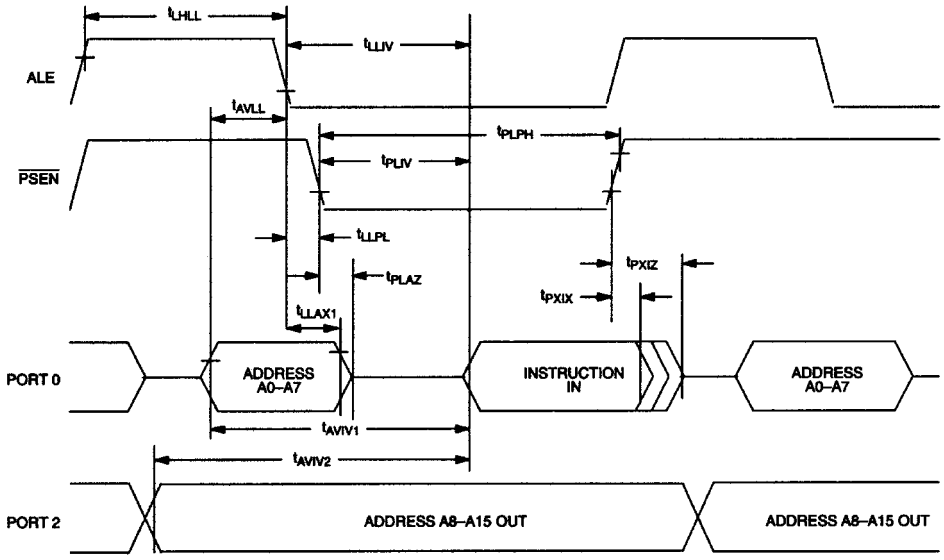
EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	10			ns	
Clock Low Time	t_{CLCX}	10			ns	
Clock Rise Time	t_{CLCL}			5	ns	
Clock Fall Time	t_{CHCL}			5	ns	

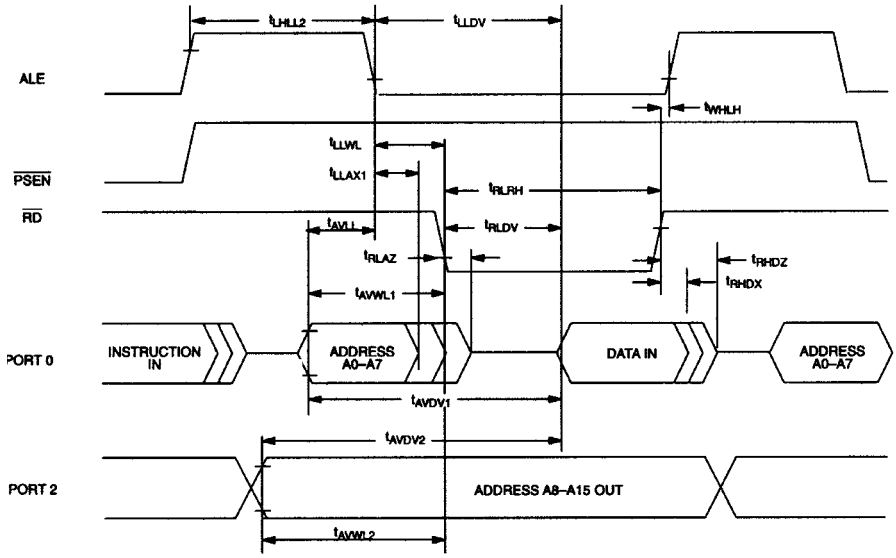
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHQX}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Input Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		 12t_{CLCL} 4t_{CLCL}		 ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		 12t_{CLCL} 4t_{CLCL}		 ns ns	

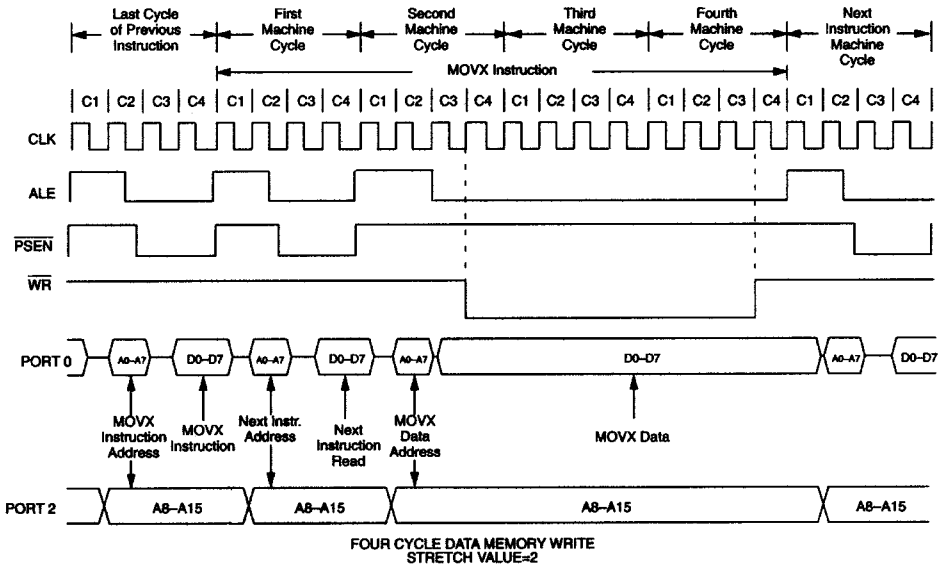
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE

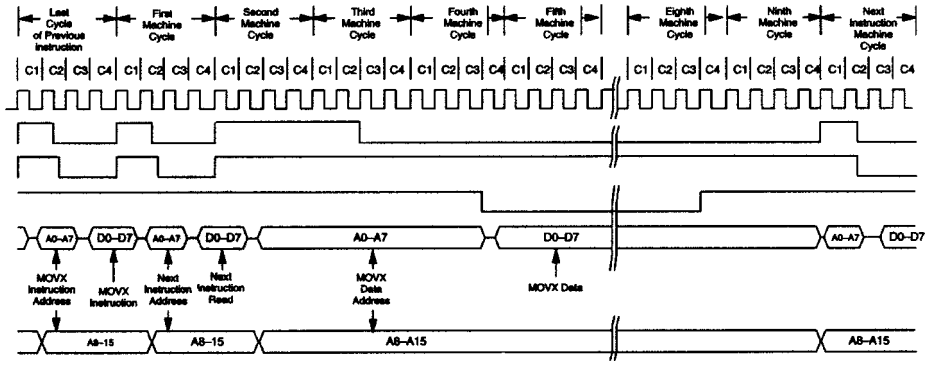


DATA MEMORY WRITE WITH STRETCH=2

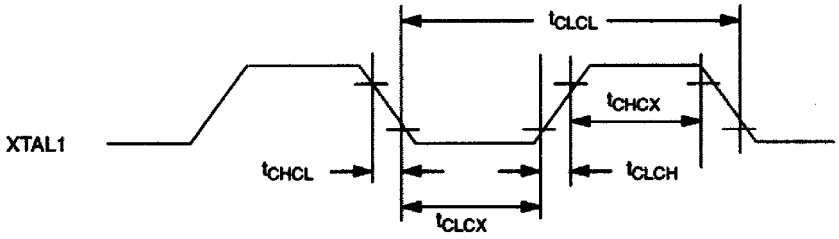


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

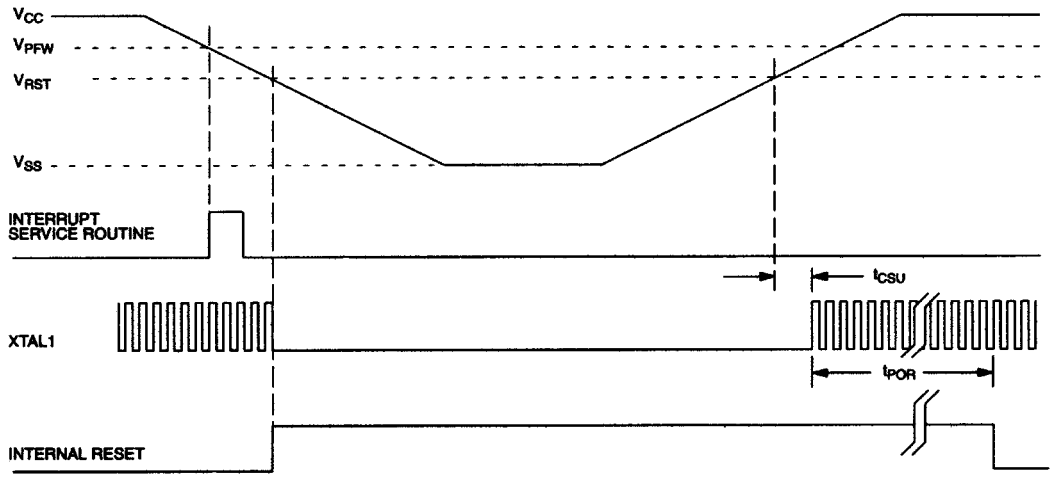
DATA MEMORY WRITE WITH STRETCH=4



EXTERNAL CLOCK DRIVE



POWER CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS