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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	33MHz
Connectivity	IrDA, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	115
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2667vfq33v

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5.2 Input/Output Pins

Table 5.1 shows the pin configuration of the interrupt controller.

Table 5.1 Pin Configuration

Name	I/O	Function
NMI	Input	Nonmaskable external interrupt Rising or falling edge can be selected.
IRQ7 to IRQ0	Input	Maskable external interrupts Rising, falling, or both edges, or level sensing, can be selected.

5.3 Register Descriptions

The interrupt controller has the following registers.

- Interrupt control register (INTCR)
- IRQ sense control register H (ISCRH)
- IRQ sense control register L (ISCRL)
- IRQ enable register (IER)
- IRQ status register (ISR)
- IRQ pin select register (ITSR)
- Software standby release IRQ enable register (SSIER)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt priority register F (IPRF)
- Interrupt priority register G (IPRG)
- Interrupt priority register H (IPRH)
- Interrupt priority register I (IPRI)
- Interrupt priority register J (IPRJ)
- Interrupt priority register K (IPRK)

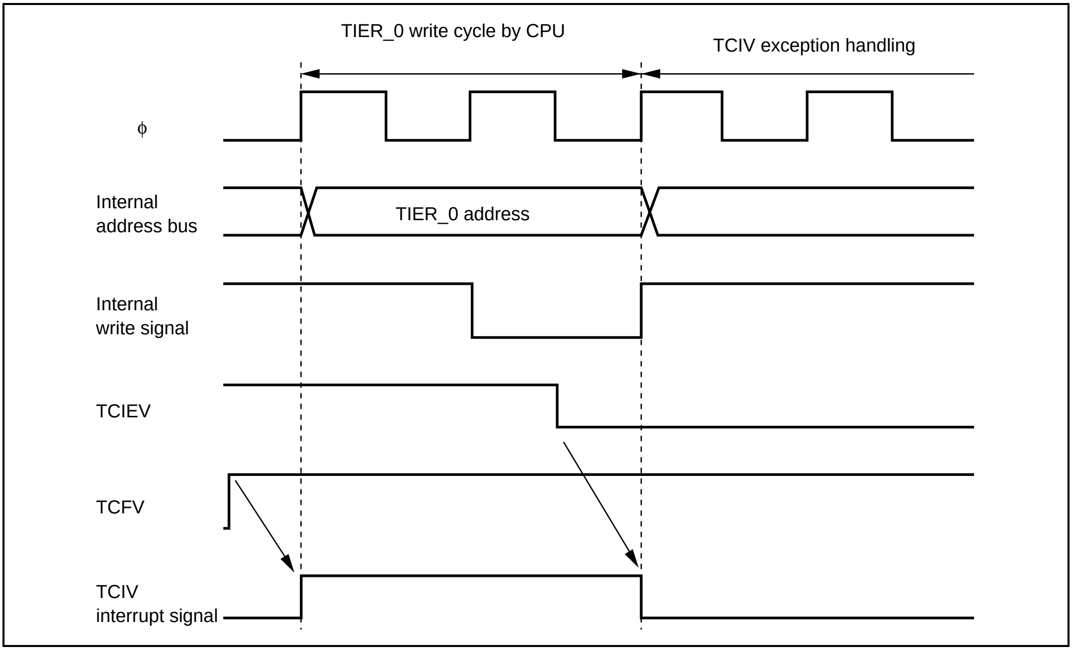


Figure 5.7 Contention between Interrupt Generation and Disabling

5.7.2 Instructions that Disable Interrupts

Instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions is executed, all interrupts including NMI are disabled and the next instruction is always executed. When the I bit is set by one of these instructions, the new value becomes valid two states after execution of the instruction ends.

5.7.3 Times when Interrupts are Disabled

There are times when interrupt acceptance is disabled by the interrupt controller.

The interrupt controller disables interrupt acceptance for a 3-state period after the CPU has updated the mask level with an LDC, ANDC, ORC, or XORC instruction.

6.2 Input/Output Pins

Table 6.1 summarizes the pin configuration of the bus controller.

Table 6.1 Pin Configuration

Name	Symbol	I/O	Function
Address strobe	AS	Output	Strobe signal indicating that an external address space is accessed and address output on address bus is enabled.
Read	RD	Output	Strobe signal indicating that an external address space is being read.
High write/write enable	HWR	Output	Strobe signal indicating that an external address space is written to, and upper half (D15 to D8) of data bus is enabled.
Low write	LWR	Output	Strobe signal indicating that an external address space is written to, and lower half (D7 to D0) of data bus is enabled.
Chip select 0	CS0	Output	Strobe signal indicating that area 0 is selected.
Chip select 1	CS1	Output	Strobe signal indicating that area 1 is selected
Chip select 2	CS2	Output	Strobe signal indicating that area 2 is selected.
Chip select 3	CS3	Output	Strobe signal indicating that area 3 is selected.
Chip select 4	CS4	Output	Strobe signal indicating that area 4 is selected.
Chip select 5	CS5	Output	Strobe signal indicating that area 5 is selected.
Chip select 6	CS6	Output	Strobe signal indicating that area 6 is selected.
Chip select 7	CS7	Output	Strobe signal indicating that area 7 is selected.
Wait	WAIT	Input	Wait request signal when accessing external address space.
Bus request	BREQ	Input	Request signal for release of bus to external bus master.
Bus request acknowledge	BACK	Output	Acknowledge signal indicating that bus has been released to external bus master.
Bus request output	BREQO	Output	External bus request signal used when internal bus master accesses external address space when external bus is released.

7.5.2 Repeat Mode

In repeat mode, one operation transfers one byte or one word of data. Table 7.4 lists the register function in repeat mode. From 1 to 256 transfers can be specified. Once the specified number of transfers has ended, the initial state of the transfer counter and the address register specified as the repeat area is restored, and transfer is repeated. In repeat mode the transfer counter value does not reach H'00, and therefore CPU interrupts cannot be requested when DISEL = 0.

Table 7.4 Register Function in Repeat Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register AH	CRAH	Holds number of transfers
DTC transfer count register AL	CRAL	Designates transfer count
DTC transfer count register B	CRB	Not used

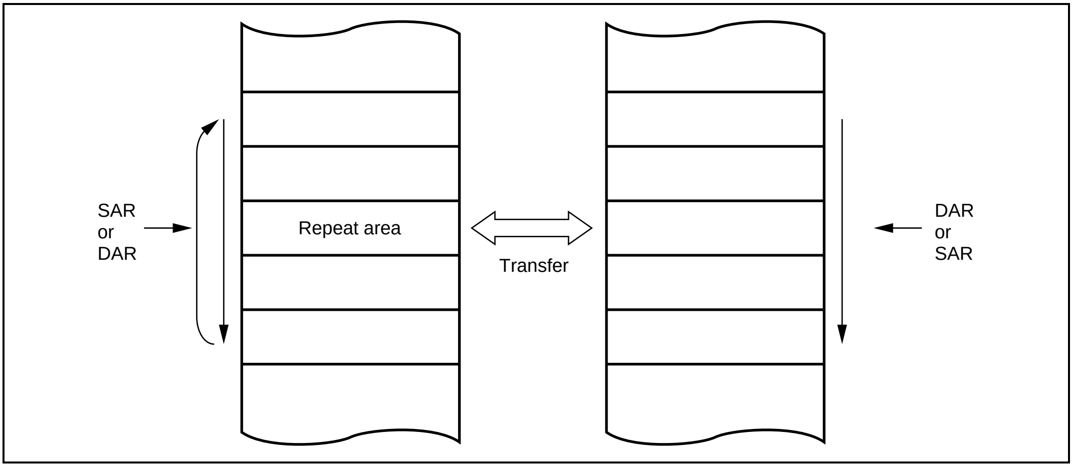


Figure 7.6 Memory Mapping in Repeat Mode

P11/PO9/TIOCB0: The pin function is switched as shown below according to the combination of the TPU channel 0 settings (by bits MD3 to MD0 in TMDR0 and bits IOB3 to IOB0 in TIOR0H), bit NDER9 in NDERH, and bit P11DDR.

TPU channel 0 settings	(1) in table below	(2) in table below		
P11DDR	—	0	1	1
NDER9	—	—	0	1
Pin function	TIOCB0 output	P11 input	P11 output	PO9 output
		TIOCB0 input*		

Note: * TIOCB0 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

TPU channel 0 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2, CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

8.2 Port 2

Port 2 is an 8-bit I/O port that also has other functions. The port 2 has the following registers.

- Port 2 data direction register (P2DDR)
- Port 2 data register (P2DR)
- Port 2 register (PORT2)

8.2.1 Port 2 Data Direction Register (P2DDR)

The individual bits of P2DDR specify input or output for the pins of port 2.

P2DDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	P27DDR	0	W	When a pin function is specified to a general purpose I/O, setting this bit to 1 makes the corresponding port 1 pin an output pin, while clearing this bit to 0 makes the pin an input pin.
6	P26DDR	0	W	
5	P25DDR	0	W	
4	P24DDR	0	W	
3	P23DDR	0	W	
2	P22DDR	0	W	
1	P21DDR	0	W	
0	P20DDR	0	W	

8.3.6 Pin Functions

Port 3 pins also function as SCI I/Os and a bus control signal output. The correspondence between the register specification and the pin functions is shown below.

P35/SCK1: The pin function is switched as shown below according to the combination of the C/$\overline{A}$ bit in SMR of SCI_1, bits CKE0 and CKE1, and bit P35DDR.

CKE1	0				1
C/A	0			1	—
CKE0	0		1	—	—
P35DDR	0	1	—	—	—
Pin function	P35 input	P35 output*	SCK1 output*	SCK1 output*	SCK1 input

Note: * NMOS open-drain output when P35ODR = 1.

P34/SCK0: The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in SMR of SCI_0, bits CKE0 and CKE1 in SCR, and bit P34DDR.

CKE1	0				1
C/A	0			1	—
CKE0	0		1	—	—
P34DDR	0	1	—	—	—
Pin function	P34 input	P34 output*	SCK0 output*	SCK0 output*	SCK0 input

Note: * NMOS open-drain output when P34ODR = 1.

P33/RxD1: The pin function is switched as shown below according to the combination of bit RE in SCR of SCI_1 and bit P33DDR.

RE	0		1
P33DDR	0	1	—
Pin function	P33 input	P33 output*	RxD1 input

Note: * NMOS open-drain output when P33ODR = 1.

8.9.1 Port A Data Direction Register (PADDR)

The individual bits of PADDR specify input or output for the pins of port A. PADDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7DDR	0	W	• Modes 1, 2, 5, and 6 Pins PA4 to PA0 are address outputs regardless of the PADDR settings. For pins PA7 to PA5, when the corresponding bit of A23E to A21E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A21E to 0 makes the corresponding port A pin an I/O port, and its function can be switched with PADDR. • Mode 4 When the corresponding bit of A23E to A16E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A16E to 0 makes the corresponding port A pin an I/O port, and its function can be switched with PADDR. • Mode 7 (when EXPE = 1) When the corresponding bit of A23E to A16E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A16E to 0 makes the corresponding port A pin an I/O port; setting the corresponding PADDR bit to 1 makes the pin an output port, while clearing the bit to 0 makes the pin an input port. • Mode 7 (when EXPE = 0) Port A is an I/O port, and its pin functions can be switched with PADDR.
6	PA6DDR	0	W	
5	PA5DDR	0	W	
4	PA4DDR	0	W	
3	PA3DDR	0	W	
2	PA2DDR	0	W	
1	PA1DDR	0	W	
0	PA0DDR	0	W	

8.12 Port D

Port D is an 8-bit I/O port that also has other functions. The port D has the following registers.

- Port D data direction register (PDDDR)
- Port D data register (PDDR)
- Port D register (PORTD)
- Port D pull-up MOS control register (PDPCR)

8.12.1 Port D Data Direction Register (PDDDR)

The individual bits of PDDDR specify input or output for the pins of port D.

PDDDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7DDR	0	W	• Modes 1, 2, 4, 5, 6, and 7 (when EXPE = 1) Port D is automatically designated for data input/output. • Mode 7 (when EXPE = 0) Port D is an I/O port, and its pin functions can be switched with PDDDR.
6	PD6DDR	0	W	
5	PD5DDR	0	W	
4	PD4DDR	0	W	
3	PD3DDR	0	W	
2	PD2DDR	0	W	
1	PD1DDR	0	W	
0	PD0DDR	0	W	

8.15.4 Port Function Control Register 0 (PFCR0)

PFCR0 performs I/O port control.

Bit	Bit Name	Initial Value	R/W	Description
7	CS7E	1	R/W	CS7 to CS0 Enable
6	CS6E	1	R/W	These bits enable or disable the corresponding CSn output.
5	CS5E	1	R/W	0: Pin is designated as I/O port
4	CS4E	1	R/W	1: Pin is designated as CSn output pin
3	CS3E	1	R/W	(n = 7 to 0)
2	CS2E	1	R/W	
1	CS1E	1	R/W	
0	CS0E	1	R/W	

8.15.5 Pin Functions

Port G pins also function as bus control signal I/Os. The correspondence between the register specification and the pin functions is shown below.

PG6/$\overline{\text{BREQ}}$: The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, and bit PG6DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
BRLE	0		1	—		0		1
PG6DDR	0	1	—	0	1	0	1	—
Pin function	PG6 input	PG6 output	$\overline{\text{BREQ}}$ input	PG6 input	PG6 output	PG6 input	PG6 output	$\overline{\text{BREQ}}$ input

Table 9.7 TPSC2 to TPSC0 (Channel 2)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
2	0	0	0	Internal clock: counts on $\phi/1$
			1	Internal clock: counts on $\phi/4$
		1	0	Internal clock: counts on $\phi/16$
			1	Internal clock: counts on $\phi/64$
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	Internal clock: counts on $\phi/1024$

Note: This setting is ignored when channel 2 is in phase counting mode.

Table 9.8 TPSC2 to TPSC0 (Channel 3)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
3	0	0	0	Internal clock: counts on $\phi/1$
			1	Internal clock: counts on $\phi/4$
		1	0	Internal clock: counts on $\phi/16$
			1	Internal clock: counts on $\phi/64$
	1	0	0	External clock: counts on TCLKA pin input
			1	Internal clock: counts on $\phi/1024$
		1	0	Internal clock: counts on $\phi/256$
			1	Internal clock: counts on $\phi/4096$

Table 9.11 MD3 to MD0

Bit 3 MD3*[1]	Bit 2 MD2*[2]	Bit 1 MD1	Bit 0 MD0	Description
0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	x	x	x	—

Legend: x: Don't care

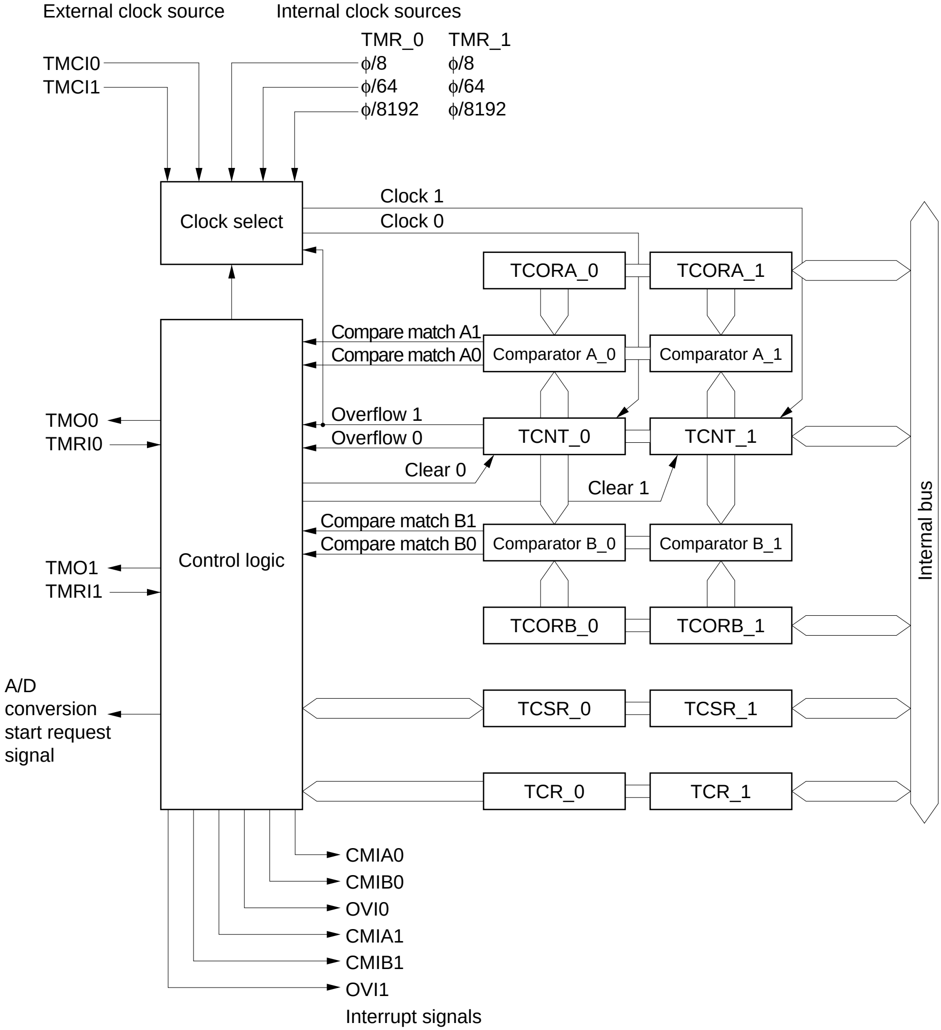
Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

Section 10 Programmable Pulse Generator (PPG)

The programmable pulse generator (PPG) provides pulse outputs by using the 16-bit timer pulse unit (TPU) as a time base. The PPG pulse outputs are divided into 4-bit groups (groups 3 to 0) that can operate both simultaneously and independently. The block diagram of PPG is shown in figure 10.1

10.1 Features

- 16-bit output data
- Four output groups
- Selectable output trigger signals
- Non-overlap mode
- Can operate together with the data transfer controller (DTC)
- Settable inverted output
- Module stop mode can be set



Legend:

TCORA_0: Time constant register A_0	TCORA_1: Time constant register A_1
TCORB_0: Time constant register B_0	TCORB_1: Time constant register B_1
TCNT_0: Timer counter_0	TCNT_1: Timer counter_1
TCSR_0: Timer control/status register_0	TCSR_1: Timer control/status register_1
TCR_0: Timer control register_0	TCR_1: Timer control register_1

Figure 11.1 Block Diagram of 8-Bit Timer Module

17.6 On-Board Programming Modes

In an on-board programming mode, programming, erasing, and verification for the on-chip flash memory can be performed. There are two on-board programming modes: boot mode and user program mode. Table 17.4 shows how to select boot mode. User program mode can be selected by setting the control bits by software. For a diagram that shows mode transitions of flash memory, see figure 17.2.

Table 17.4 Setting On-Board Programming Modes

Mode Setting		MD2	MD1	MD0
Boot mode	Single-chip activation expanded mode with on-chip ROM enabled	0	1	1

17.6.1 Boot Mode

When this LSI enters boot mode, the embedded boot program is started. The boot program transfers the programming control program from the externally connected host to the on-chip RAM via the SCI_1. When the flash memory is all erased, the programming control program is executed.

Table 17.5 shows the boot mode operations between reset end and branching to the programming control program.

1. When the boot program is initiated, the SCI_1 should be set to asynchronous mode, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI_1 bit rate to match that of the host. The transfer format is 8-bit data, 1 stop bit, and no parity. The reset should end with the RxD pin high. The RxD and TxD pins should be pulled up on the board if necessary. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period.
2. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 17.6.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	—	All 0	—	Reserved These bits are always read as 0. The initial value should not be changed.
3 2 1 0	STS3 STS2 STS1 STS0	1 1 1 1	R/W R/W R/W R/W	Standby Timer Select 3 to 0 These bits select the time the MCU waits for the clock to stabilize when software standby mode is cleared by an external interrupt. With crystal oscillation, refer to table 19.2 and make a selection according to the operating frequency so that the standby time is at least the oscillation stabilization time. With an external clock, a PLL circuit stabilization time is necessary. Refer to table 19.2 to set the wait time. 0000: Setting prohibited 0001: Setting prohibited 0010: Setting prohibited 0011: Setting prohibited 0100: Setting prohibited 0101: Standby time = 64 states 0110: Standby time = 512 states 0111: Standby time = 1024 states 1000: Standby time = 2048 states 1001: Standby time = 4096 states 1010: Standby time = 16384 states 1011: Standby time = 32768 states 1100: Standby time = 65536 states 1101: Standby time = 131072 states 1110: Standby time = 262144 states 1111: Standby time = 524288 states

Register Name	Abbrevia-tion	Bit No.	Address	Module	Data Width	Access States
Timer interrupt enable register_0	TIER_0	8	H'FFD4	TPU_0	16	2
Timer status register_0	TSR_0	8	H'FFD5	TPU_0	16	2
Timer counter_0	TCNT_0	16	H'FFD6	TPU_0	16	2
Timer general register A_0	TGRA_0	16	H'FFD8	TPU_0	16	2
Timer general register B_0	TGRB_0	16	H'FFDA	TPU_0	16	2
Timer general register C_0	TGRC_0	16	H'FFDC	TPU_0	16	2
Timer general register D_0	TGRD_0	16	H'FFDE	TPU_0	16	2
Timer control register_1	TCR_1	8	H'FFE0	TPU_1	16	2
Timer mode register_1	TMDR_1	8	H'FFE1	TPU_1	16	2
Timer I/O control register_1	TIOR_1	8	H'FFE2	TPU_1	16	2
Timer interrupt enable register_1	TIER_1	8	H'FFE4	TPU_1	16	2
Timer status register_1	TSR_1	8	H'FFE5	TPU_1	16	2
Timer counter_1	TCNT_1	16	H'FFE6	TPU_1	16	2
Timer general register A_1	TGRA_1	16	H'FFE8	TPU_1	16	2
Timer general register B_1	TGRB_1	16	H'FFEA	TPU_1	16	2
Timer control register_2	TCR_2	8	H'FFF0	TPU_2	16	2
Timer mode register_2	TMDR_2	8	H'FFF1	TPU_2	16	2
Timer I/O control register_2	TIOR_2	8	H'FFF2	TPU_2	16	2
Timer interrupt enable register_2	TIER_2	8	H'FFF4	TPU_2	16	2
Timer status rgister_2	TSR_2	8	H'FFF5	TPU_2	16	2
Timer counter_2	TCNT_2	16	H'FFF6	TPU_2	16	2
Timer general register A_2	TGRA_2	16	H'FFF8	TPU_2	16	2
Timer general register B_2	TGRB_2	16	H'FFFA	TPU_2	16	2

Notes: 1. Register of the flash memory version. Not available in the masked ROM version and ROM-less version.

2. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.

3. For writing, refer to section 12.6.1, Notes on register access.