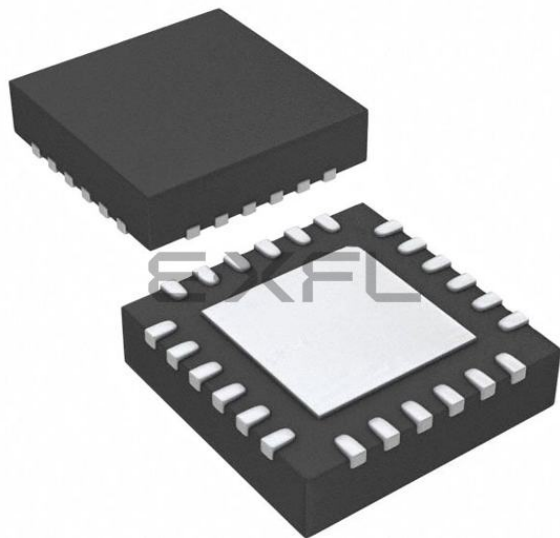




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 2x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32zg110f32-qfn24

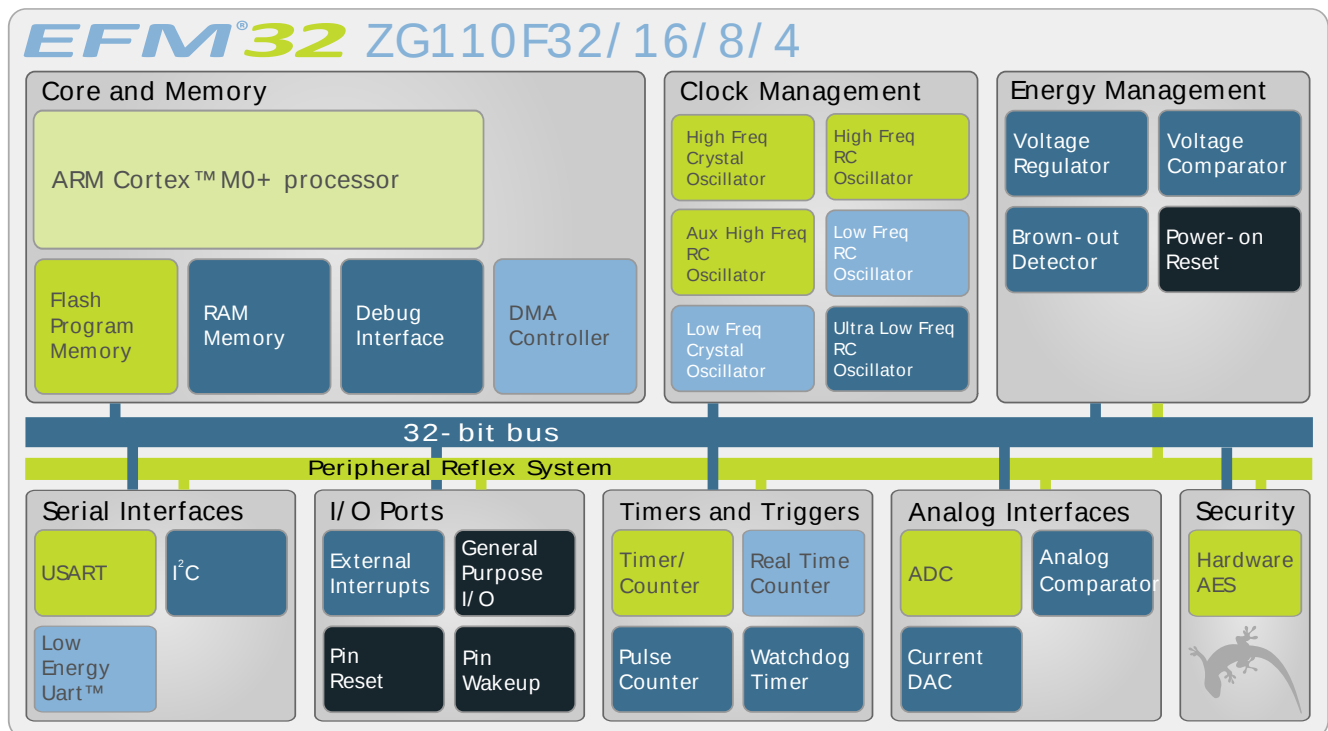
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32ZG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32ZG110 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32ZG Reference Manual*.

A block diagram of the EFM32ZG110 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface .

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32ZG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.22 General Purpose Input/Output (GPIO)

In the EFM32ZG110, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 11 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32ZG110 is a subset of the feature set described in the EFM32ZG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

Table 2.1. Configuration Summary

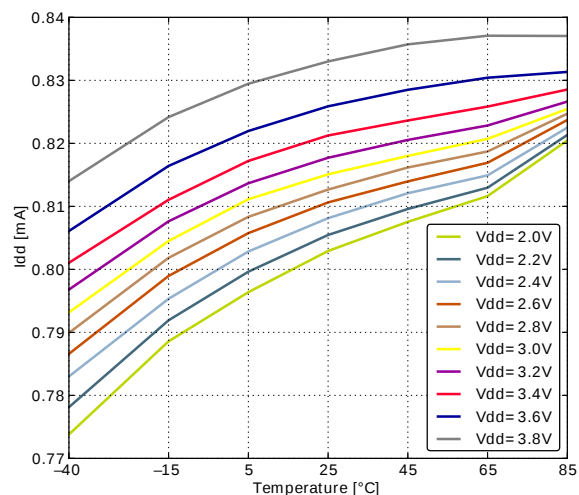
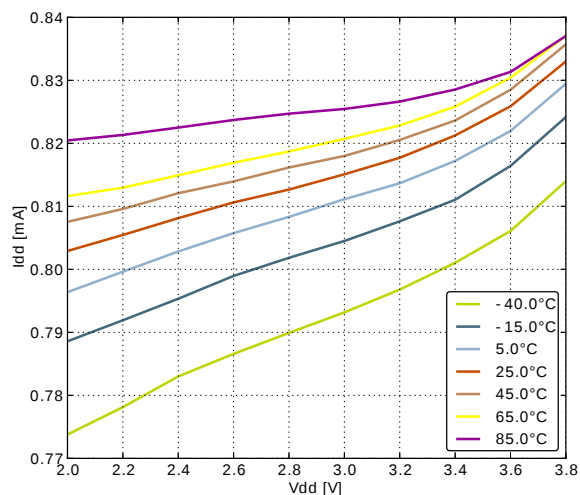
Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[1:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA

3.4 Current Consumption

Table 3.3. Current Consumption

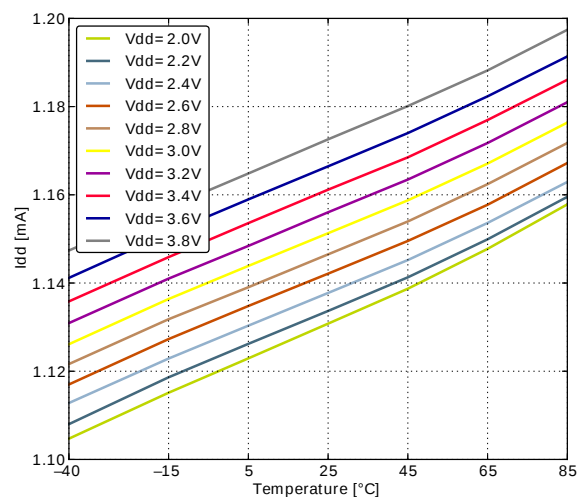
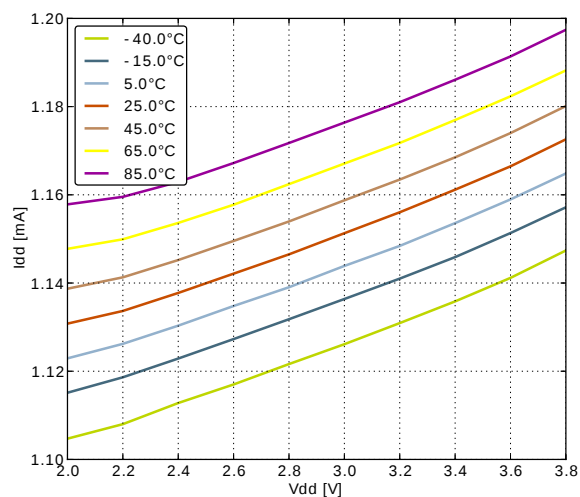
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		115	132	μA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		117	136	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		114	128	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		116	132	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		117	131	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		118	133	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		118	133	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		120	135	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		124	139	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		125	142	μA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		155	177	μA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		162	181	μA/MHz
I _{EM1}	EM1 current (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		48	57	μA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		49	59	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		48	52	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		49	53	μA/MHz

Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz

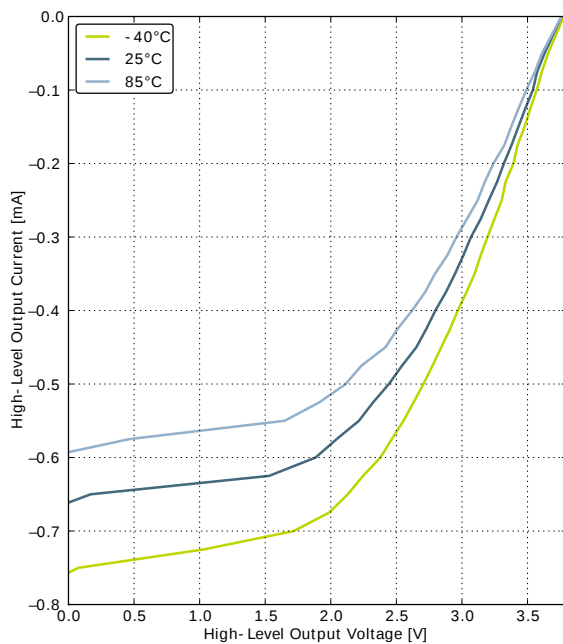


3.4.2 EM1 Current Consumption

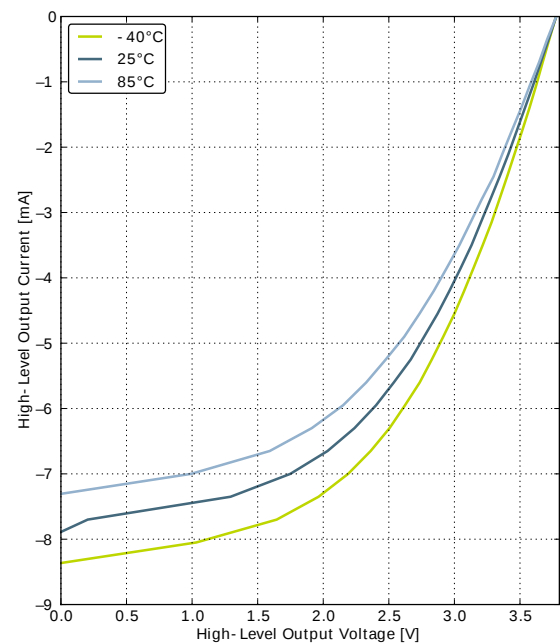
Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz



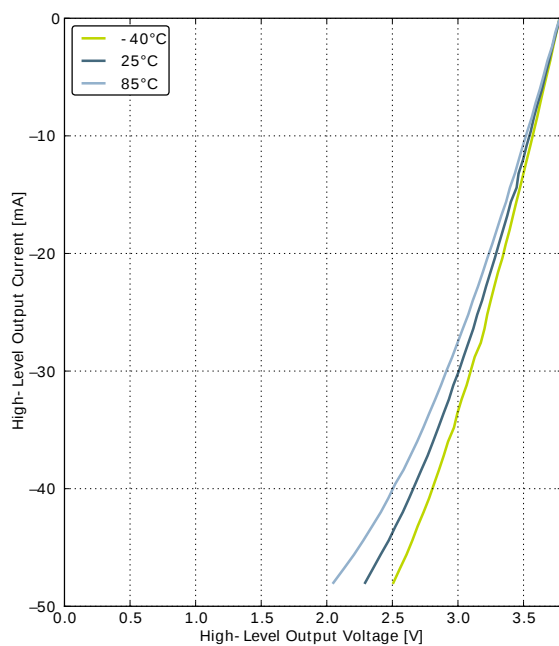
Symbol	Parameter	Condition	Min	Typ	Max	Unit
	by the glitch suppression filter					
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25pF$.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600pF$	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8 V$	$0.1V_{DD}$			V

Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage

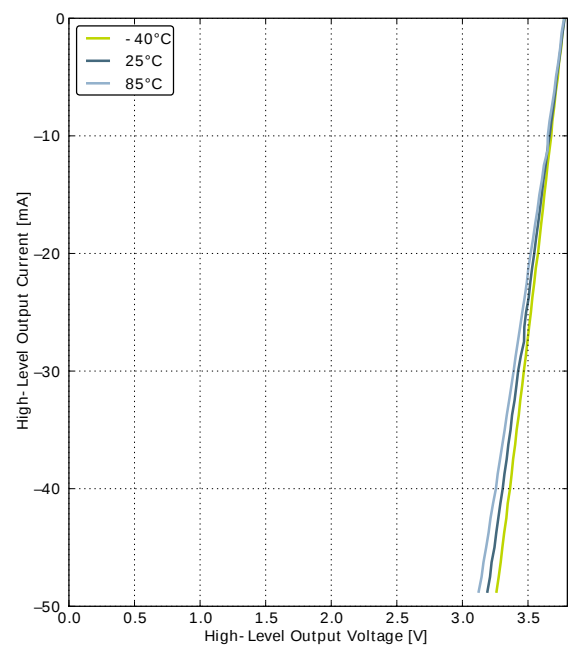
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)	$V_{DD} = 3.0$ V, external 2.5V reference	-1	± 0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method	$V_{DD} = 3.0$ V, external 2.5V reference		± 1.2	± 3	LSB
MC_{ADC}	No missing codes		11.999 ¹	12		bits

¹On the average every ADC will have one missing code, most likely to appear around $2048 \pm n \times 512$ where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.26 (p. 36) and Figure 3.27 (p. 36) , respectively.

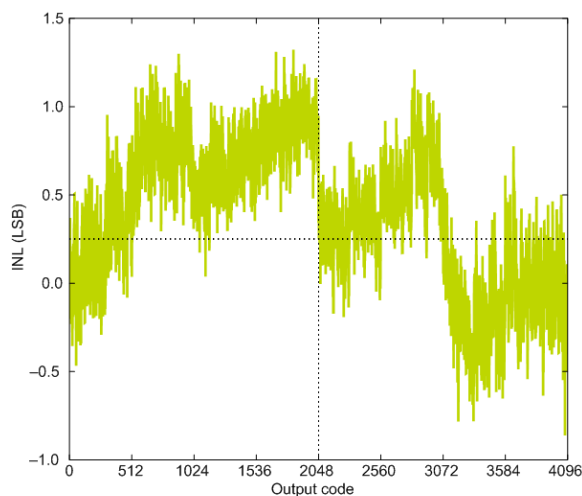
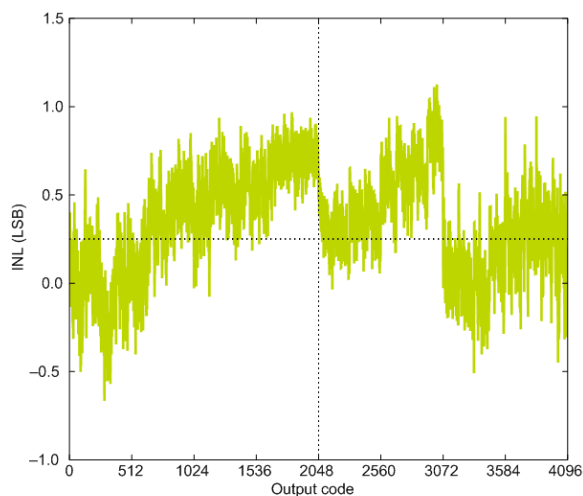
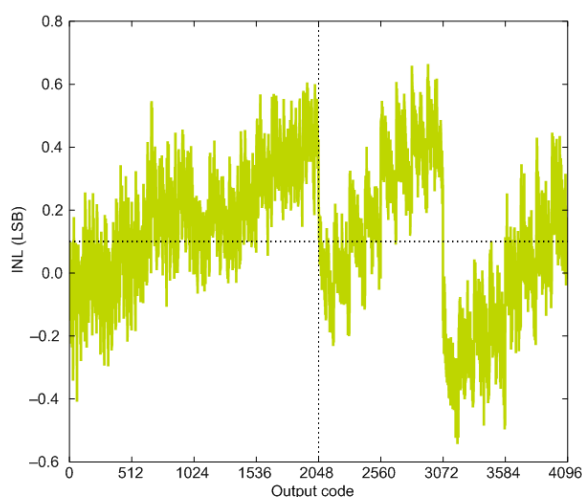
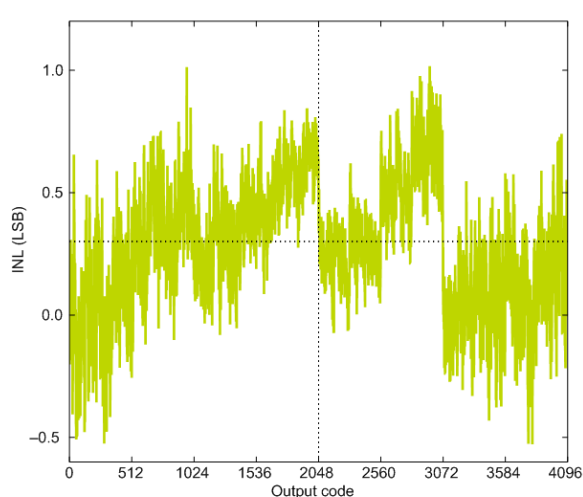
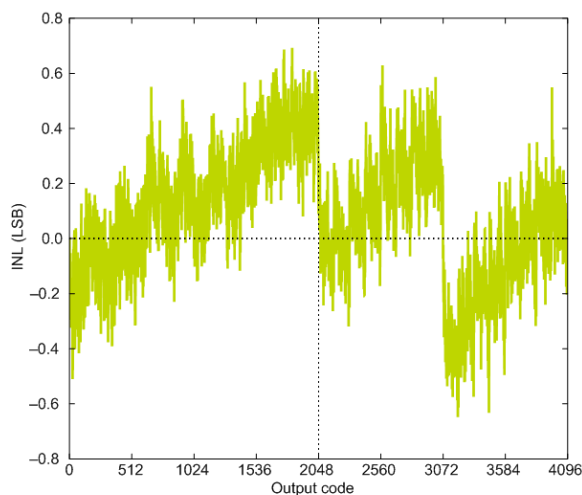
Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

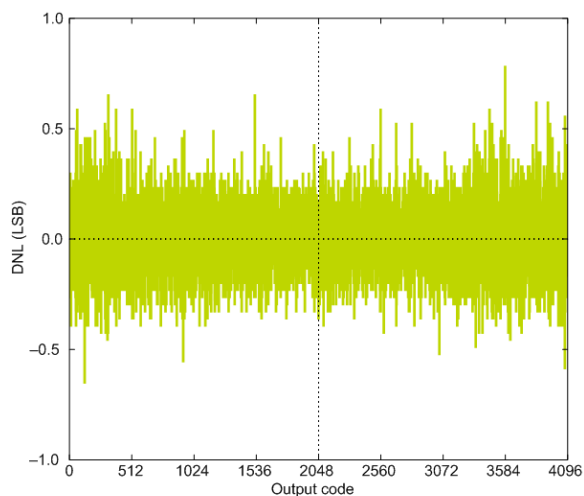
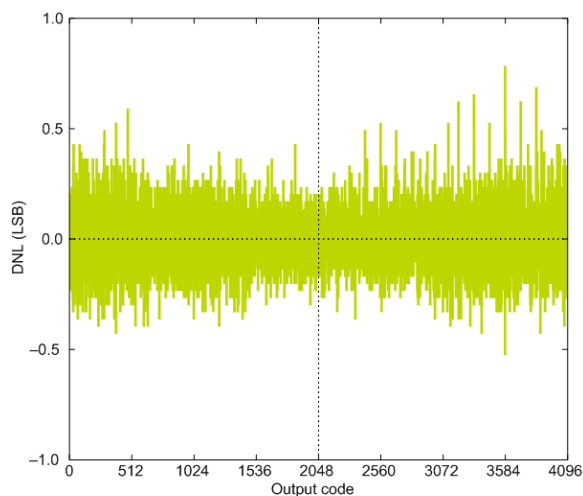
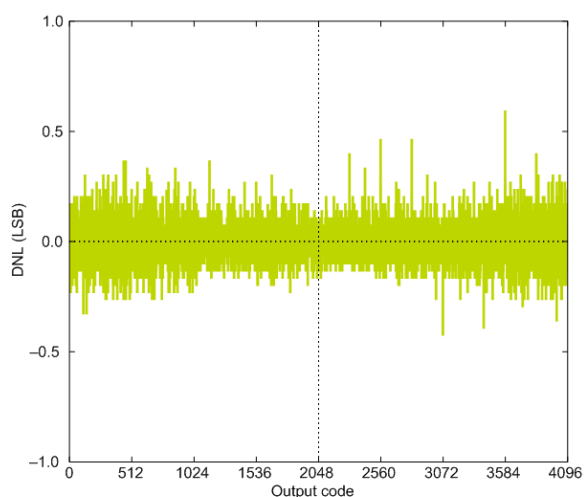
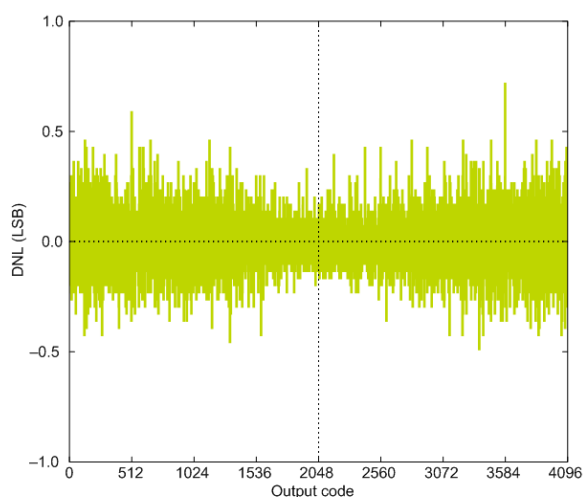
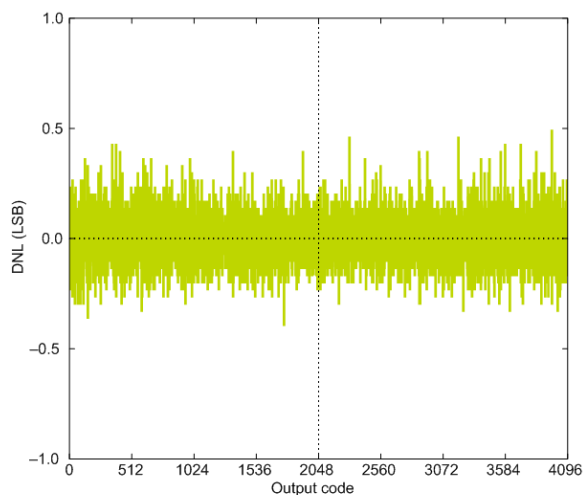
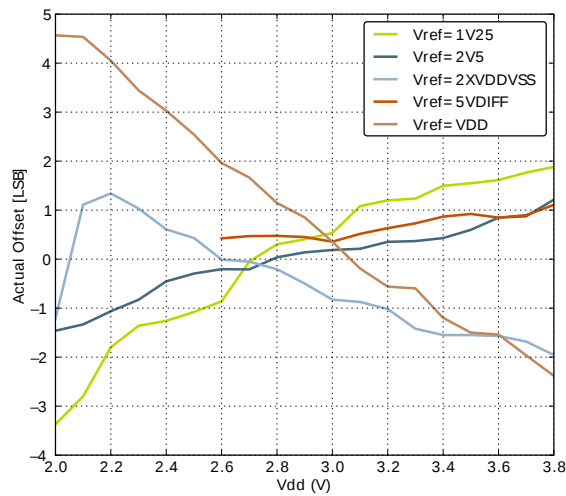
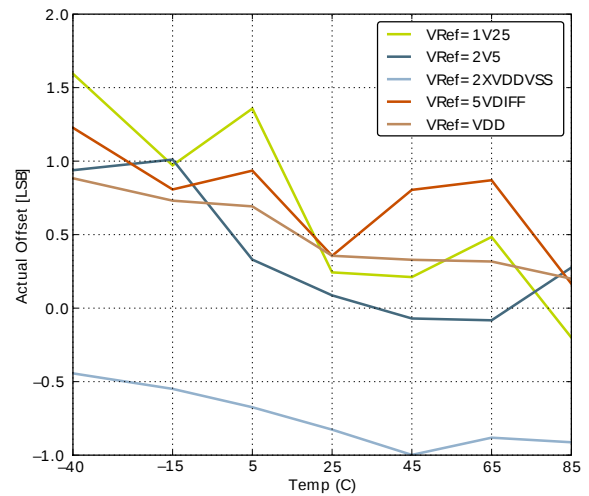
Figure 3.30. ADC Differential Linearity Error vs Code, $V_{dd} = 3V$, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.31. ADC Absolute Offset, Common Mode = $V_{dd}/2$

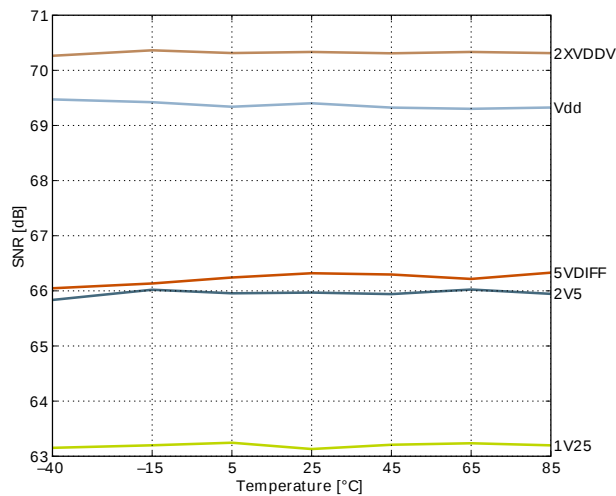


Offset vs Supply Voltage, Temp = 25°C

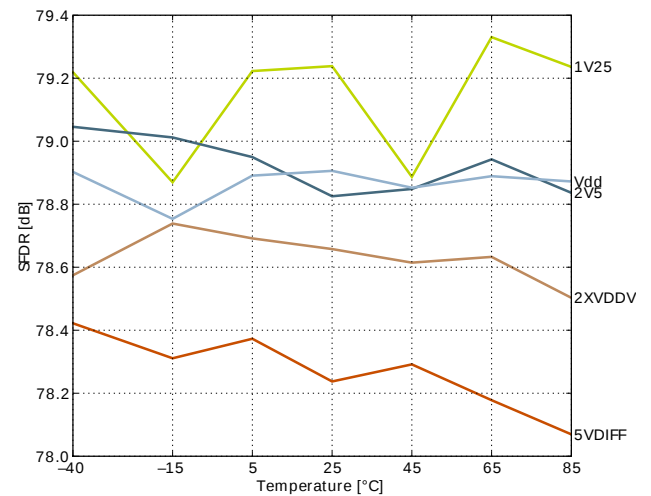


Offset vs Temperature, $V_{dd} = 3V$

Figure 3.32. ADC Dynamic Performance vs Temperature for all ADC References, $V_{dd} = 3V$

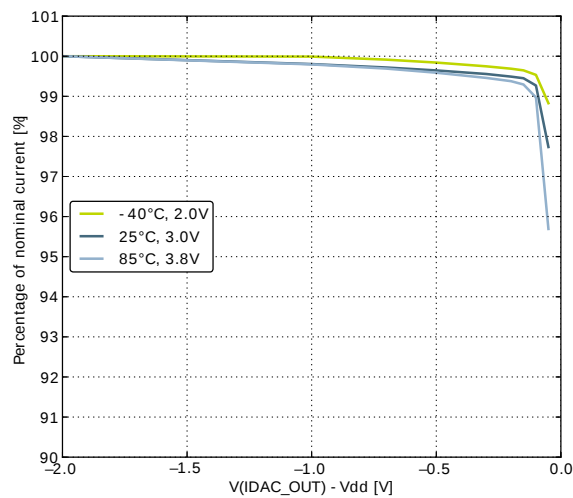


Signal to Noise Ratio (SNR)

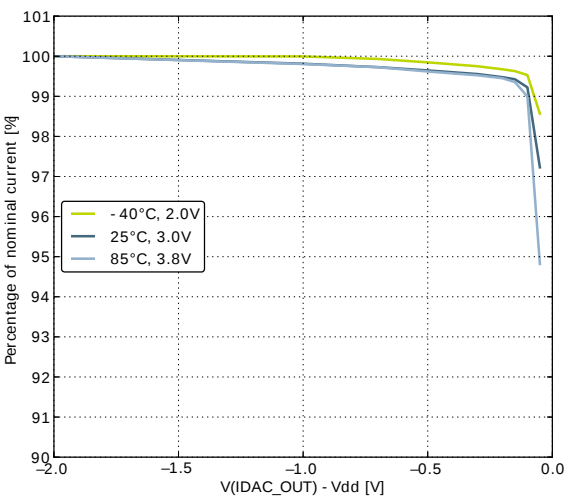


Spurious-Free Dynamic Range (SFDR)

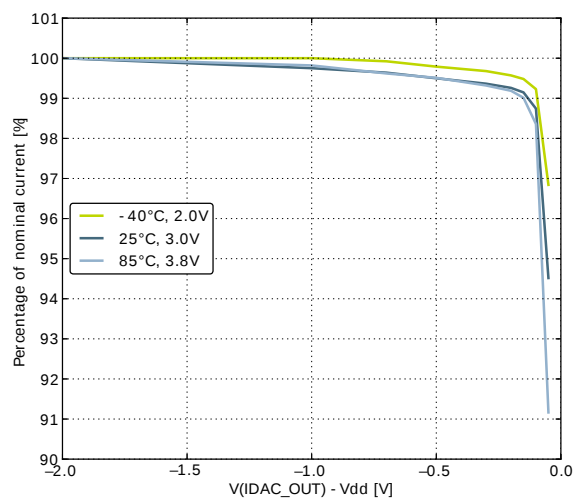
Figure 3.34. IDAC Source Current as a function of voltage on IDAC_OUT



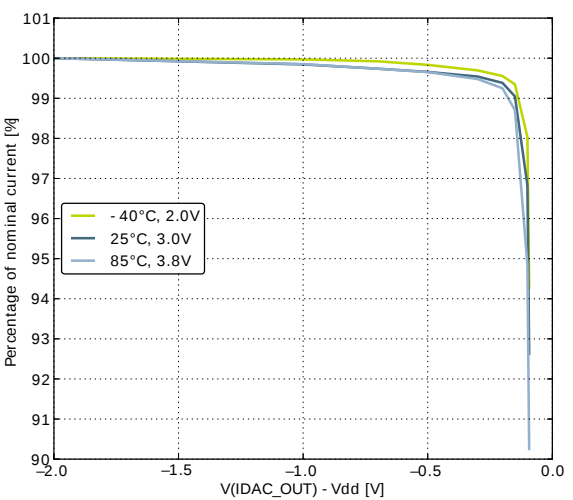
Range 0



Range 1

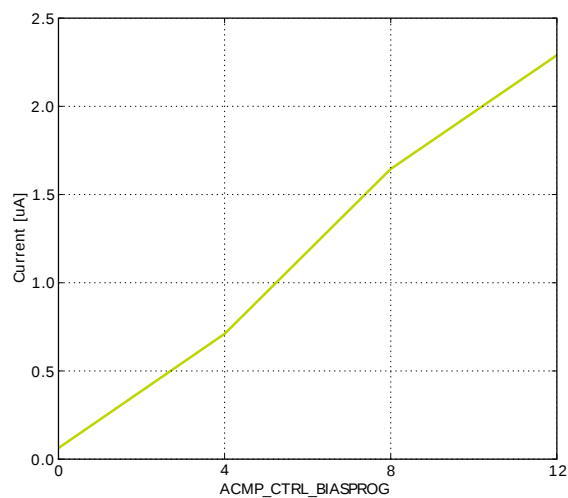


Range 2

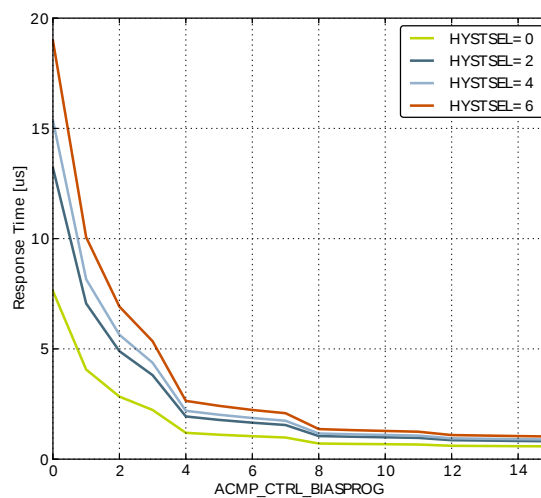


Range 3

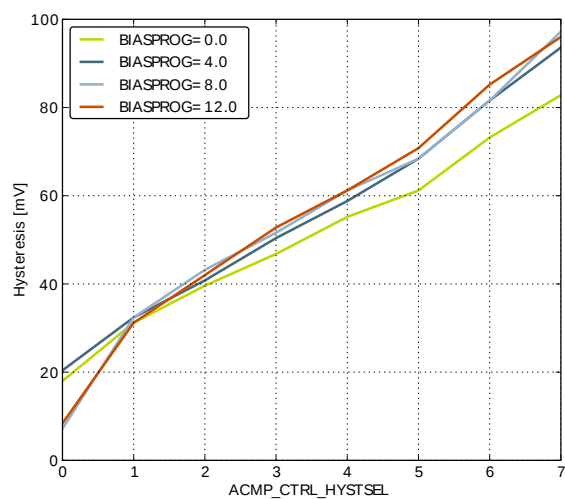
Figure 3.37. ACMP Characteristics, $V_{dd} = 3V$, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time , $V_{cm} = 1.25V$, CP+ to CP- = 100mV



Hysteresis

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		400 ¹	kHz
t _{LOW}	SCL clock low time	1.3			μs
t _{HIGH}	SCL clock high time	0.6			μs
t _{SU,DAT}	SDA set-up time	100			ns
t _{HD,DAT}	SDA hold time	8		900 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	0.6			μs
t _{HD,STA}	(Repeated) START condition hold time	0.6			μs
t _{SU,STO}	STOP condition set-up time	0.6			μs
t _{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32ZG Reference Manual.

²The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 5).

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0		1000 ¹	kHz
t _{LOW}	SCL clock low time	0.5			μs
t _{HIGH}	SCL clock high time	0.26			μs
t _{SU,DAT}	SDA set-up time	50			ns
t _{HD,DAT}	SDA hold time	8			ns
t _{SU,STA}	Repeated START condition set-up time	0.26			μs
t _{HD,STA}	(Repeated) START condition hold time	0.26			μs
t _{SU,STO}	STOP condition set-up time	0.26			μs
t _{BUF}	Bus free time between a STOP and START condition	0.5			μs

¹For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32ZG Reference Manual.

3.15 Digital Peripherals

Table 3.29. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{USART}	USART current	USART idle current, clock enabled		7.5		μA/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		6.25		μA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		μA/ MHz
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		100		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		100		nA

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32ZG110.

4.1 Pinout

The EFM32ZG110 pinout is shown in Figure 4.1 (p. 51) and Table 4.1 (p. 51). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32ZG110 Pinout (top view, not to scale)

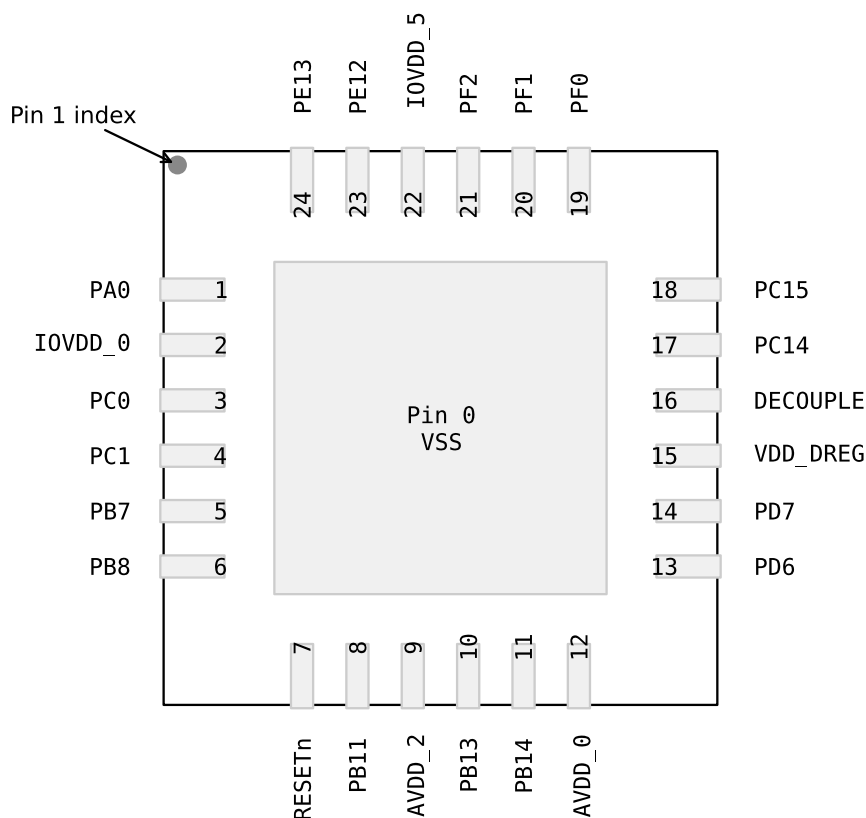
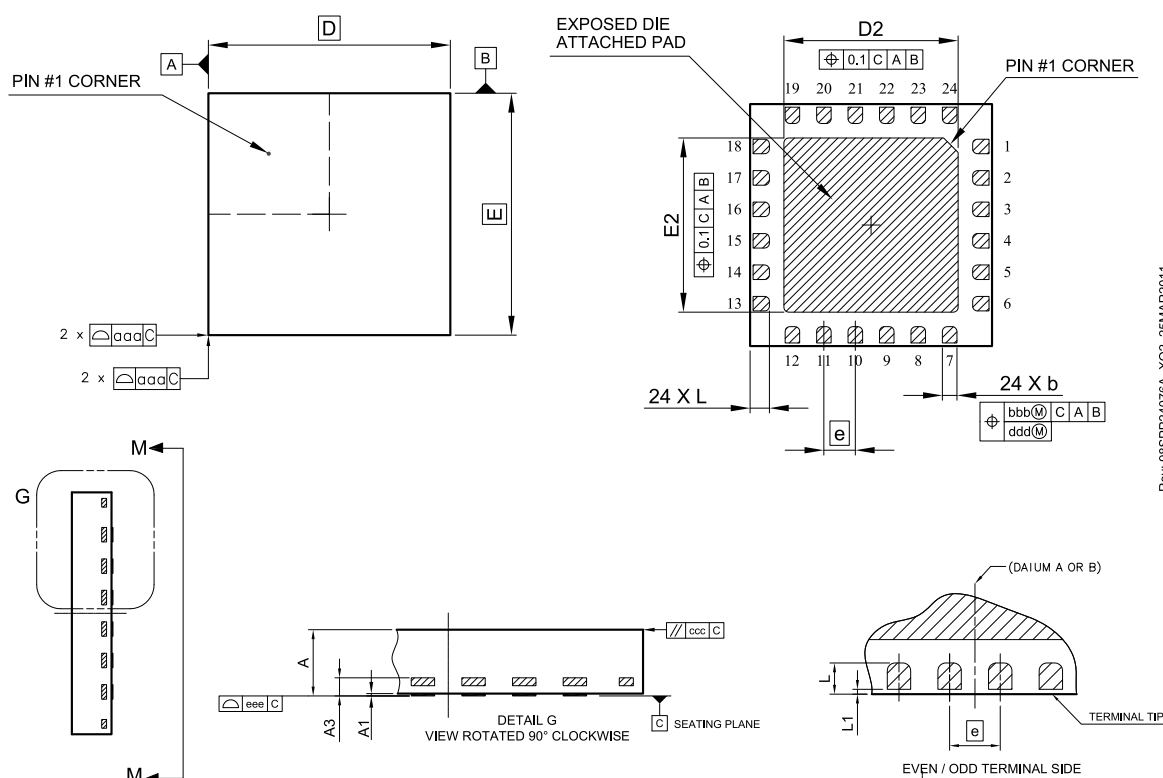


Table 4.1. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4	PRS_CH0 #0

4.4 QFN24 Package

Figure 4.2. QFN24



Rev: 98SPP24076A XO2 25MAR2011

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

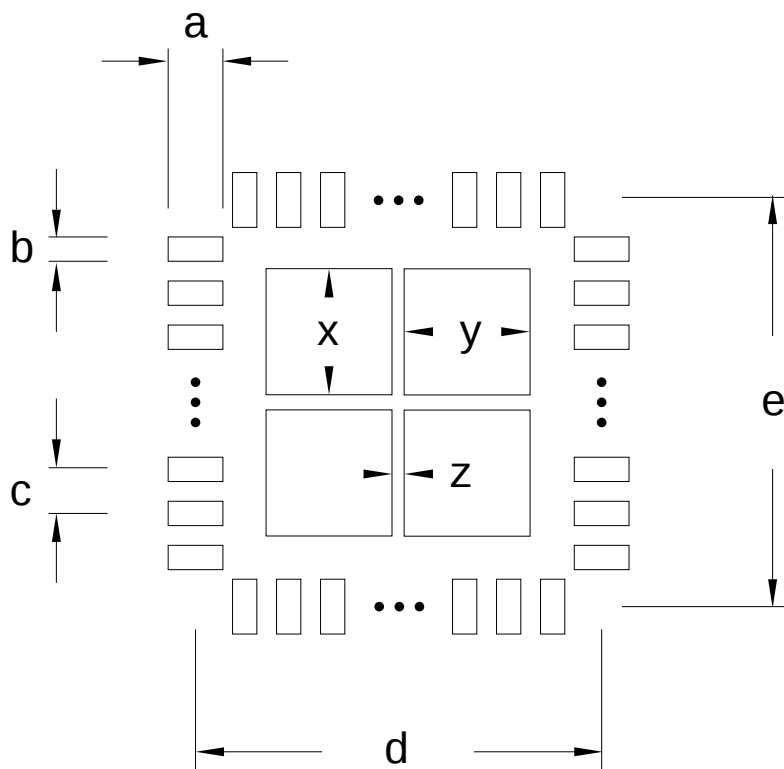
Table 4.4. QFN24 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00	0.203 REF	0.25	5.00 BSC	5.00 BSC	3.50	3.50	0.65 BSC	0.35	0.00	0.10	0.10	0.10	0.05	0.08
Nom	0.85	-		0.30			3.60	3.60		0.40						
Max	0.90	0.05		0.35			3.70	3.70		0.45	0.10					

The QFN24 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
<http://www.silabs.com/support/quality/pages/default.aspx>

Figure 5.3. QFN24 PCB Stencil Design**Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.60	e	5.00
b	0.25	x	1.00
c	0.65	y	1.00
d	5.00	z	0.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 55) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

7 Revision History

7.1 Revision 1.10

March 6th, 2015

Updated ADC data, updated temperature sensor graph and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Updated Max ESR_{HFXO} value for Crystal Frequency of 24 MHz.

Updated current consumption.

Updated LFXO and HFXO data.

Updated LFRCO and HFRCO data.

Updated ACMP data.

Updated VCMP data.

Updated Memory Map.

Added DMA current in Digital Peripherals section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated Package dimensions table.

Updated block diagram.

7.2 Revision 1.00

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Removed "Preliminary" markings.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ADC data.

Updated ACMP data.

7.3 Revision 0.61

November 21st, 2013

Corrected all current values in Electrical Characteristics section.

Updated Cortex M0 related items in the memory map.

7.9 Revision 0.10

June 7th, 2011

Initial preliminary release.

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