Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Sigma
Interface	I²C, SPI
Clock Rate	50MHz
Non-Volatile Memory	-
On-Chip RAM	12kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1401ystz-rl

TABLE OF CONTENTS

REVISION HISTORY

1/12—Rev. B to Rev. C

Changed Pin Number Range from 43 to 46 to Pin Number 43 Only (Table 11) 14
Changes to Ordering Guide 52

1/11—Rev. A to Rev. B

Changes to Figure 1 4
Changes to Figure 7 and Table 11 12
Changes to Figure 20 and Figure 21 25
Changes to Figure 27 27

4/08—Rev. 0 to Rev. A

Changes to Figure 1 4
Changes to Table 11 12
Replaced Figure 8 to Figure 11 15
Renamed Theory of Operation Section 17
Changes to Initialization Section 18
Change to Setting the Master Clock/PLL Mode Section 19
Replaced Figure 22 through Figure 25 26
Changes to EEPROM Format Section 28
Deleted Table 21, Renumbered Sequentially 29
Inserted Figure 28, Renumbered Sequentially 29
Changes to Figure 37 49
Changes to Figure 38 50
Changes to Figure 39 51

7/07—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz, unless otherwise noted.

ANALOG PERFORMANCE

Specifications are guaranteed at 25°C (ambient).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		µA rms (µA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	95	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	99	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

Specifications are guaranteed at 130°C (ambient).

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		µA rms (µA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	92	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	98	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

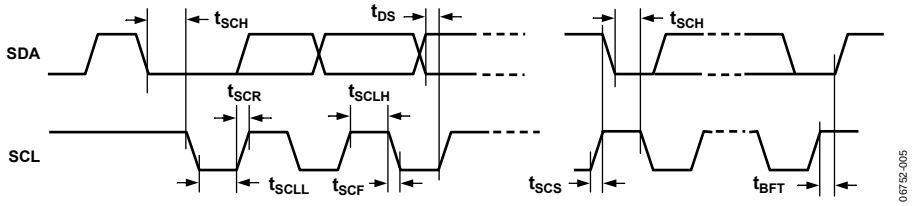

Figure 4. I²C Port Timing

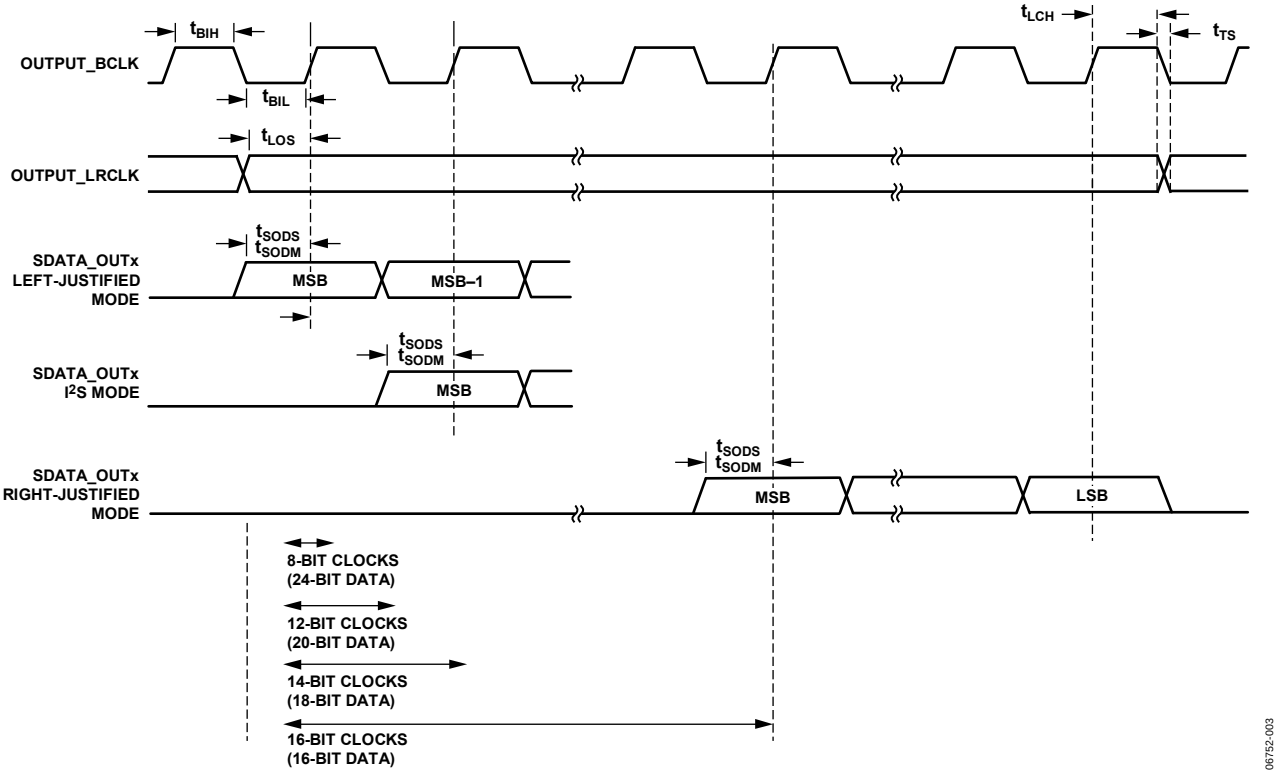

Figure 5. Serial Output Port Timing

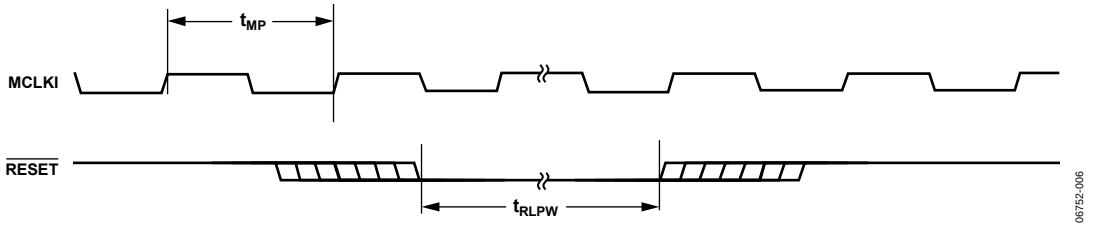

Figure 6. Master Clock and $\overline{RESET}$ Timing

THEORY OF OPERATION

The core of the ADAU1401 is a 28-bit DSP (56-bit with double-precision processing) optimized for audio processing. The program and parameter RAMs can be loaded with a custom audio processing signal flow built by using SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows for transparent parameter updates and prevents clicks in the output signals.

The program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1401 can self-boot on startup. In this standalone mode, parameters can be controlled through the on-board multipurpose pins. The ADAU1401 can accept controls from switches, potentiometers, rotary encoders, and IR receivers. Parameters such as volume and tone settings can be saved to the EEPROM on power-down and recalled again on power-up.

The ADAU1401 can operate with digital or analog inputs and outputs, or a mix of both. The stereo ADC and four DACs each have an SNR of at least +100 dB and a THD + N of at least −83 dB. The 8-channel, flexible serial data input/output ports allow glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers and transmitters, and sample rate converters. The serial ports of the ADAU1401 can be configured in I²S, left-justified, right-justified, or TDM serial port compatible modes.

Twelve multipurpose (MP) pins allow the ADAU1401 to receive external control signals as input and to output flags or controls to other devices in the system. The MP pins can be configured as digital I/Os, inputs to the 4-channel auxiliary ADC, or serial data I/O ports. As inputs, they can be connected to buttons, switches, rotary encoders, potentiometers, IR receivers, or other external circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs, control other ICs, or connect to other external circuitry in an application.

The ADAU1401 has a sophisticated control port that supports complete read/write capability of all memory locations. Control registers are provided to offer complete control of the configuration and serial modes of the chip. The ADAU1401 can be configured for either SPI or I²C control, or can self-boot from an external EEPROM.

An on-board oscillator can be connected to an external crystal to generate the master clock. In addition, a master clock phase-locked loop (PLL) allows the ADAU1401 to be clocked from a variety of different clock speeds. The PLL can accept inputs of $64 \times f_S$, $256 \times f_S$, $384 \times f_S$, or $512 \times f_S$ to generate the internal master clock of the core.

The SigmaStudio software is used to program and control the SigmaDSP® through the control port. Along with designing and tuning a signal flow, the tools can be used to configure all of the DSP registers and burn a new program into the external EEPROM. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design a DSP signal flow and port it to a target application. At the same time, it provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, dynamics processors, mixers, and delays), compile the design, and load the program and parameter files into the ADAU1401 memory through the control port. Signal processing blocks available in the provided libraries include

- Single- and double-precision biquad filters
- Processors with peak or rms detection for monochannel and multichannel dynamics
- Mixers and splitters
- Tone and noise generators
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone sources
- FIR filters
- Level detectors
- GPIO control and conditioning

Additional processing blocks are always being developed. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

The ADAU1401 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply. It is fabricated on a single monolithic, integrated circuit and is packaged in a 48-lead LQFP for operation over the −40°C to +105°C temperature range.

VOLTAGE REGULATOR

The digital voltage of the ADAU1401 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems without an available 1.8 V supply but with an available 3.3 V supply. The only external components needed in such instances are a PNP transistor, a resistor, and a few bypass capacitors. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 16. The 10 µF and 100 nF capacitors shown in this configuration are recommended for bypassing, but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF to 47 µF) is needed for both DVDD pins. With this configuration, 3.3 V is the main system voltage; 1.8 V is generated at the transistor's collector, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

Two specifications must be considered when choosing a regulator transistor: The transistor's current amplification factor (h_{FE} or beta) should be at least 100, and the transistor's collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current drawn from the ADAU1401 is 60 mA. The equation to determine the minimum power dissipation of the transistor is as follows:

$$(3.3\ V - 1.8\ V) \times 60\ mA = 90\ mW$$

There are many transistors, such as the FZT953 from Zetex Semiconductors, with these specifications available in small SOT-23 or SOT-223 packages.

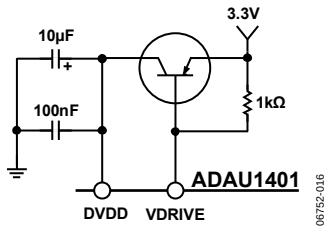

Figure 16. Voltage Regulator Configuration

AUDIO ADCs

The ADAU1401 has two Σ-Δ ADCs. The signal-to-noise ratio (SNR) of the ADCs is 100 dB, and the THD + N is −83 dB.

The stereo audio ADCs are current input; therefore, a voltage-to-current resistor is required on the inputs. This means that the voltage level of the input signals to the system can be set to any level; only the input resistors need to be scaled to provide the proper full-scale current input. The ADC0 and ADC1 input pins, as well as ADC_RES, have an internal 2 kΩ resistor for ESD protection. The voltage seen directly on the ADC input pins is the 1.5 V common mode.

The external resistor connected to ADC_RES sets the full-scale current input of the ADCs. The full range of the ADC inputs is 100 μA rms with an external 18 kΩ resistor on ADC_RES (20 kΩ total, because it is in series with the internal 2 kΩ). The only reason to change the ADC_RES resistor is if a sampling rate other than 48 kHz is used.

The voltage-to-current resistors connected to ADC0/ADC1 set the full-scale voltage input of the ADCs. With a full-scale current input of 100 μA rms, a 2.0 V rms signal with an external 18 kΩ resistor (in series with the 2 kΩ internal resistor) results in an input using the full range of the ADC. The matching of these resistors to the ADC_RES resistor is important to the operation of the ADCs. For these three resistors, a 1% tolerance is recommended.

Either the ADC0 and/or ADC1 input pins can be left unconnected if that channel of the ADC is unused.

These calculations of resistor values assume a 48 kHz sample rate. The recommended input and current setting resistors scale linearly with the sample rate because the ADCs have a switched-capacitor input. The total value (2 kΩ internal plus external resistor) of the ADC_RES resistor with sample rate f_{S_NEW} can be calculated as follows:

$$R_{total} = 20\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

The values of the resistors (internal plus external) in series with the ADC0 and ADC1 pins can be calculated as follows:

$$R_{Input\ Total} = (rms\ Input\ Voltage) \times 10\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

Table 14 lists the external and total resistor values for common signal input levels at a 48 kHz sampling rate. A full-scale rms input voltage of 0.9 V is shown in the table because a full-scale signal at this input level is equal to a full-scale output on the DACs.

Table 14. ADC Input Resistor Values

Full-Scale RMS Input Voltage (V)	ADC_RES Value (kΩ)	ADC0/ADC1 Resistor Value (kΩ)	Total ADC0/ADC1 Input Resistance (External + Internal) (kΩ)
0.9	18	7	9
1.0	18	8	10
2.0	18	18	20

Figure 17 shows a typical configuration of the ADC inputs for a 2.0 V rms input signal for a f_S of 48 kHz. The 47 μF capacitors are used to ac-couple the signals so that the inputs are biased at 1.5 V.

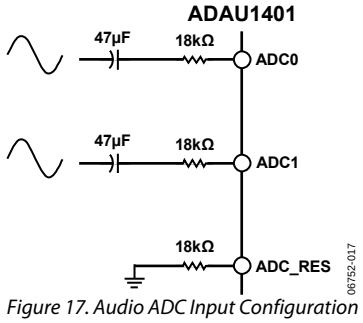

Figure 17. Audio ADC Input Configuration

CONTROL PORTS

The ADAU1401 can operate in one of three control modes:

- I²C control
- SPI control
- Self-boot (no external controller)

The ADAU1401 has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOOT pin is low at power-up, the part defaults to I²C mode but can be put into SPI control mode by pulling the CLATCH/WP pin low three times. When the SELFBOOT pin is set high at power-up, the ADAU1401 loads its program, parameters, and register settings from an external EEPROM on startup.

The control port is capable of full read/write operation for all addressable memory and registers. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in a single-address mode or a burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1401. This subaddress must be two bytes because the memory locations within the ADAU1401 are directly addressable and their sizes exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. The exact formats for specific types of writes are shown in Table 22 to Table 31.

The ADAU1401 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. If large blocks of data need to be downloaded, the output of the DSP core can be halted (using the CR bit in the DSP core control register (Address 2076)), new data can be loaded, and then the device can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 15 details these multiple functions.

Table 15. Control Port Pins and SELFBOOT Pin Functions

Pin	I²C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open-collector output	COUT—output	SDA—open-collector output
ADDR1/CDATA/WB	ADDR1—input	CDATA—input	WB—writeback trigger
CLATCH/WP	Unused input—tie to ground or IOVDD	CLATCH—input	WP—EEPROM write protect, open-collector output
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or IOVDD

I²C Read and Write Operations

Figure 22 shows the timing of a single-word write operation. Every ninth clock, the ADAU1401 issues an acknowledge by pulling SDA low.

Figure 23 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The ADAU1401 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The timing of a single-word read operation is shown in Figure 24. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the ADAU1401 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This causes the ADAU1401 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1401.

Figure 25 shows the timing of a burst mode read sequence. This figure shows an example where the target read registers are two bytes. The ADAU1401 increments its subaddress every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other addresses may have word lengths ranging from one to five bytes. The ADAU1401 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Figure 22 to Figure 25 use the following abbreviations:
S = start bit
P = stop bit
AM = acknowledge by master
AS = acknowledge by slave

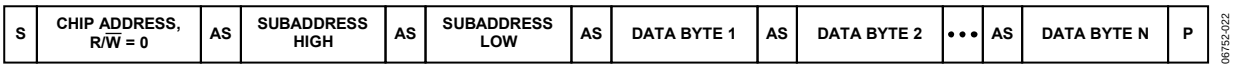

Figure 22. Single Word I²C Write Format

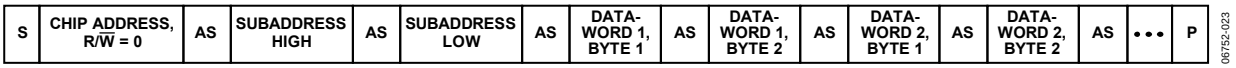

Figure 23. Burst Mode I²C Write Format

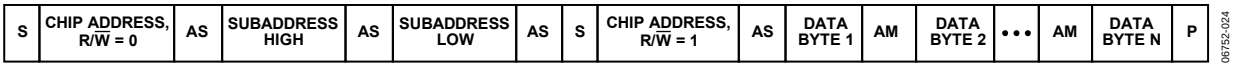

Figure 24. Single-Word I²C Read Format

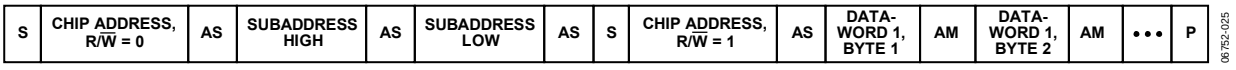

Figure 25. Burst Mode I²C Read Format

SIGNAL PROCESSING

The ADAU1401 is designed to provide all audio signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using the SigmaStudio software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic data. The input and output word lengths of the DSP core are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

NUMERIC FORMATS

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1401 uses the same numeric format for both the parameter and data values. The format is as follows.

Numerical Format: 5.23

Linear range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 0011 0011 0011 0011 0011 = −0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 − 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without internal clipping.

A digital clipper circuit is used between the output of the DSP core and the DACs or serial port outputs (see Figure 29). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to −1.0. Figure 29 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

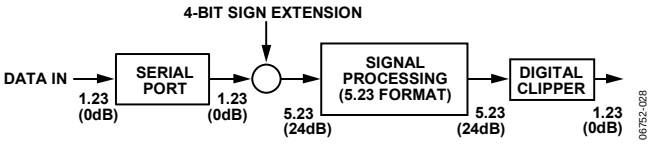

Figure 29. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the ADAU1401 default program passes the unprocessed input signals to the outputs (shown in Figure 13), but the outputs are muted by default (see the Power-Up Sequence section). There are 1024 instruction cycles per audio sample, resulting in about 50 MIPS available. The SigmaDSP runs in a stream-oriented manner, meaning that all 1024 instructions are executed each sample period. The ADAU1401 can also be set up to accept double- or quad-speed inputs by reducing the number of instructions per sample that are set in the core control register.

The part can be easily programmed using SigmaStudio (Figure 30), a graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required. More information about SigmaStudio can be found at www.analog.com.

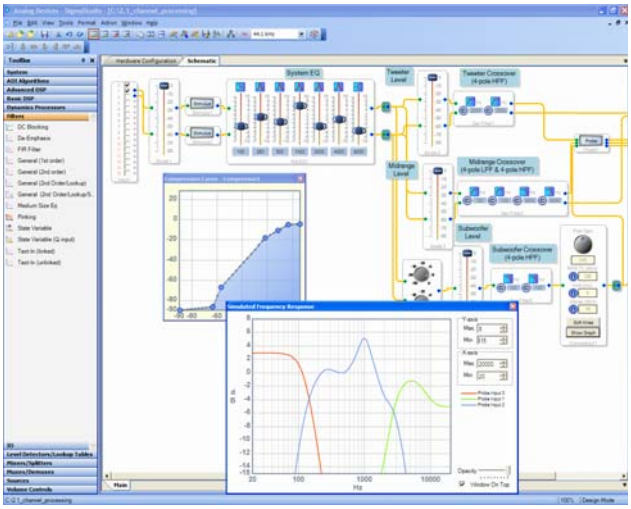

Figure 30. SigmaStudio Screen Shot

RAMS AND REGISTERS

Table 21. RAM Map and Read/Write Modes

Memory	Size	Address Range	Read	Write	Write Modes
Parameter RAM	1024 × 32	0 to 1023 (0x0000 to 0x03FF)	Yes	Yes	Direct write[1] safeload write
Program RAM	1024 × 40	1024 to 2047 (0x0400 to 0x07FF)	Yes	Yes	Direct write[1]

[1] Internal registers should be cleared first to avoid clicks/pops.

ADDRESS MAPS

Table 21 shows the RAM map and Table 32 shows the ADAU1401 register map. The address space encompasses a set of registers and two RAMs: one holds signal processing parameters and one holds the program instructions. The program RAM and parameter RAM are initialized on power-up from on-board boot ROMs (see the Power-Up Sequence section).

All RAMs and registers have a default value of all 0s, except for the program RAM, which is loaded with the default program (see the Initialization section).

PARAMETER RAM

The parameter RAM is 32 bits wide and occupies Address 0 to Address 1023. Each parameter is padded with four 0s before the MSB to extend the 28-bit word to a full 4-byte width. The parameter RAM is initialized to all 0s on power-up. The data format of the parameter RAM is twos complement, 5.23. This means that the coefficients can range from +16.0 (minus 1 LSB) to −16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000 or by the hexadecimal word 0x00 0x80 0x00 0x00.

The parameter RAM can be written using one of the two following methods: a direct read/write or a safeload write.

Direct Read/Write

The direct read/write method allows direct access to the program RAM and parameter RAM. This mode of operation is typically used when loading a new RAM using burst mode addressing. The clear registers bit in the core control register should be set to 0 using this mode to avoid any clicks or pops in the outputs. Note that this mode can be used during live program execution, but because there is no handshaking between the core and the control port, the parameter RAM is unavailable to the DSP core during control writes, resulting in clicks and pops in the audio stream.

Safeload Write

Up to five safeload registers can be loaded with the parameter RAM address/data. The data is then transferred to the requested address when the RAM is not busy. This method can be used for dynamic updates while live program material is playing through the ADAU1401. For example, a complete update of one biquad section can occur in one audio frame while the RAM is not busy. This method is not available for writing to the program RAM or control registers.

DATA RAM

The ADAU1401 data RAM is used to store audio data words for processing. For the most part, this process is transparent to the user. The user cannot address this RAM space, which has a size of 2k words, directly from the control port.

Data RAM utilization should be considered when implementing blocks that require large amounts of data RAM space, such as delays. The SigmaDSP core processes delay times in one-sample increments; therefore, the total pool of delay available to the user equals 2048 multiplied by the sample period. For a f_S of 48 kHz, the pool of available delay is a maximum of about 43 ms. In practice, this much data memory is not available to the user because every block in a design uses a few data memory locations for its processing. In most DSP programs, this does not significantly impact the total delay time. The SigmaStudio compiler manages the data RAM and indicates if the number of addresses needed in the design exceeds the maximum available.

READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte oriented. This allows easy programming of common microcontroller chips. To fit into a byte-oriented format, 0s are appended to the data fields before the MSB to extend the data-word to eight bits. For example, 28-bit words written to the parameter RAM are appended with four leading 0s to equal 32 bits (four bytes); 40-bit words written to the program RAM are not appended with 0s because they are already a full five bytes. These zero-padded data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address. The control port knows how many data bytes to expect based on the address given in the first three bytes.

The total number of bytes for a single-location write command can vary from four bytes (for a control register write) to eight bytes (for a program RAM write). Burst mode can be used to fill contiguous register or RAM locations. A burst mode write begins by writing the address and data of the first RAM or register location to be written. Rather than ending the control port transaction (by issuing a stop command in I^2C mode or by bringing the CLATCH signal high in SPI mode after the data-word), as would be done in a single-address write, the next data-word can be immediately written without specifying its address. The ADAU1401 control port auto-increments the address of each write even across the boundaries of the different RAMs and registers. Table 23 and Table 25 show examples of burst mode writes.

Table 22. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]
chip_adr[6:0], $\overline{W}$/R	000000, param_adr[9:8]	param_adr[7:0]	0000, param[27:24]	param[23:0]

Table 23. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]	Bytes[7:10]	Bytes[11:14]
chip_adr[6:0], $\overline{W}$/R	000000, param_adr[9:8]	param_adr[7:0]	0000, param[27:24]	param[23:0]		
			<—param_adr—>		param_adr + 1	param_adr + 2

Table 24. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes[3:7]
chip_adr[6:0], $\overline{W}$/R	00000, prog_adr[10:8]	prog_adr[7:0]	prog[39:0]

Table 25. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes[3:7]	Bytes[8:12]	Bytes[13:17]
chip_adr[6:0], $\overline{W}$/R	00000, prog_adr[10:8]	prog_adr[7:0]	prog[39:0]		
			<—prog_adr—>	prog_adr + 1	prog_adr + 2

Table 26. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[15:8]	data[7:0]

Table 27. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte 1	Byte 2	Byte 3
chip_adr[6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[7:0]

Table 28. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	000, progCount[10:6][1]	progCount[5:0][1], regSel[1:0][2]

[1] progCount[10:0] is the value of the program counter when the data capture occurs (the table of values is generated by the SigmaStudio compiler).
[2] regSel[1:0] selects one of four registers (see the 2074 to 2075 (0x081A to 0x081B)—Data Capture Registers section).

Table 29. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes[3:5]
chip_adr[6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	data[23:0]

Table 30. Safeload Address Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	000000, param_adr[9:8]	param_adr[7:0]

Table 31. Safeload Data Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Bytes[5:7]
chip_adr[6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	00000000	0000, data[27:24]	data[23:0]

Register Address		No. of		MSB								D39	D38	D37	D36	D35	D34	D33	LSB	
				D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
Hex	Dec	Bytes	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0820	2080	3	MP Pin Config. 0[23:16]									MP53	MP52	MP51	MP50	MP43	MP42	MP41	MP40	0x00
			MP Pin Config. 0[15:0]	MP33	MP32	MP31	MP30	MP23	MP22	MP21	MP20	MP13	MP12	MP11	MP10	MP03	MP02	MP01	MP00	0x0000
0x0821	2081	3	MP Pin Config. 1[23:16]									MP113	MP112	MP111	MP110	MP103	MP102	MP101	MP100	0x00
			MP Pin Config. 1[15:0]	MP93	MP92	MP91	MP90	MP83	MP82	MP81	MP80	MP73	MP72	MP71	MP70	MP63	MP62	MP61	MP60	0x0000
0x0822	2082	2	Auxiliary ADC and power control	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FIL1	FIL0	AAPD	VBPD	VRPD	RSVD	D0PD	D1PD	D2PD	D3PD	0x0000
0x0823	2083	2	Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x0000
0x0824	2084	2	Auxiliary ADC enable	AAEN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x0000
0x0825	2085	2	Reserved	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x0000
0x0826	2086	2	Oscillator power-down	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OPD	RSVD	RSVD	0x0000
0x0827	2087	2	DAC setup	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	DS1	DS0	0x0000

[1] Shading indicates that registers do not fill these locations, so control bits do not exist in these locations.

CONTROL REGISTER DETAILS

2048 TO 2055 (0x0800 TO 0x0807)—INTERFACE REGISTERS

The interface registers are used in self-boot mode to save parameters that need to be written to the external EEPROM. The ADAU1401 then recalls these parameters from the EEPROM after the next reset or power-up. Therefore, system parameters such as volume and EQ settings can be saved during power-down and recalled the next time the system is turned on.

There are eight 32-bit interface registers, which allow eight 28-bit (plus zero-padding) parameters to be saved. The parameters to be saved in these registers are selected in the graphical programming tools. These registers are updated with their corresponding parameter RAM data once per sample period.

An edge, which can be set to be either rising or falling, triggers the ADAU1401 to write the current contents of the interface registers to the EEPROM. See the Self-Boot section for details.

The user can write directly to the interface registers after the interface registers control port write mode (IFCW) in the DSP core control register has been set. In this mode, the data in the registers is written from the control port, not from the DSP core.

Table 33. Interface Register Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D23 D7	D22 D6	D21 D5	D20 D4	D19 D3	D18 D2	D17 D1	D16 D0	Default
0	0	0	0	IF27	IF26	IF25	IF24	IF23	IF22	IF21	IF20	IF19	IF18	IF17	IF16	0x0000
IF15	IF14	IF13	IF12	IF11	IF10	IF09	IF08	IF07	IF06	IF05	IF04	IF03	IF02	IF01	IF00	0x0000

Table 34.

Bit Name	Description
IF[27:0]	Interface register 28-bit parameter

2057 TO 2060 (0x809 TO 0x80C)—AUXILIARY ADC DATA REGISTERS

These registers hold the data generated by the 4-channel auxiliary ADC. The ADCs have eight bits of precision and can be extended to 12 bits if filtering is selected via Bits FIL[1:0] of the auxiliary ADC and power control register. The SigmaDSP program reads this data as a 1.11 format data-word with a range of 0 to 1.0. This data-word is mapped to the 5.23 format parameter word with the four MSBs and 12 LSBs set to 0. A full-scale code of 255 results in a value of 1.0. These registers can be written to directly if the auxiliary ADC data registers control port write mode (AACW) bit is set in the DSP core control register.

Table 37. Auxiliary ADC Data Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	AA11	AA10	AA09	AA08	AA07	AA06	AA05	AA04	AA03	AA02	AA01	AA00	0x0000

Table 38.

Bit Name	Description
AA[11:0]	Auxiliary ADC output data, MSB first

2064 TO 2068 (0x0810 TO 0x814)—SAFELOAD DATA REGISTERS

Many applications require real-time microcontroller control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. When controlling a biquad filter, for example, all of the parameters must be updated at the same time. Doing so prevents the filter from executing with a mix of old and new coefficients for one or two audio frames, thus avoiding temporary instability and transients that may take a long time to decay. To accomplish this, the ADAU1401 uses safeload data registers to simultaneously load a set of five 28-bit values to the desired parameter RAM address. Five registers are used because a biquad filter uses five coefficients and, as previously mentioned, it is desirable to do a complete update in one transaction.

The first step in performing a safeload operation is writing the parameter address to one of the safeload address registers (2069 to 2073). The 10-bit data-word to be written is the address in parameter RAM to which the safeload is being performed. After this address is written, the 28-bit data-word can be written to the corresponding safeload data register (2064 to 2068).

The data formats for these writes are detailed in Table 30 and Table 31. Table 39 shows how each of the five address registers maps to its corresponding data register.

After the address and data registers are loaded, set the initiate safeload transfer bit in the core control register to initiate the loading into RAM. Each of the five safeload registers takes one of the 1024 core instructions to load into the parameter RAM. The total program lengths should, therefore, be limited to 1019 cycles (1024 minus 5) to ensure that the SigmaDSP core always has at least five cycles available. The safeload is guaranteed to occur within one LRCLK period (21 µs for a f_S of 48 kHz) of the initiate safeload transfer bit being set.

The safeload logic automatically sends data to be loaded into RAM from only those safeload registers that have been written to since the last safeload operation. For example, if two parameters are to be updated in the RAM, only two of the five safeload registers must be written. When the initiate safeload transfer bit is asserted, only data from those two registers are sent to the RAM; the other three registers are not sent to the RAM and may hold old or invalid data.

Table 39. Safeload Address and Data Register Mapping

Safeload Register	Safeload Address Register	Safeload Data Register
0	2069	2064
1	2070	2065
2	2071	2066
3	2072	2067
4	2073	2068

Table 40. Safeload Registers Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D39 D23 D7	D38 D22 D6	D37 D21 D5	D36 D20 D4	D35 D19 D3	D34 D18 D2	D33 D17 D1	D32 D16 D0	Default
								SD39	SD38	SD37	SD36	SD35	SD34	SD33	SD32	0x00
SD31	SD30	SD29	SD28	SD27	SD26	SD25	SD24	SD23	SD22	SD21	SD20	SD19	SD18	SD17	SD16	0x0000
SD15	SD14	SD13	SD12	SD11	SD10	SD09	SD08	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00	0x0000

Table 41.

Bit Name	Description
SD[39:0]	Safeload Data. Data (program, parameters, register contents) to be loaded into the RAMs or registers.

2069 TO 2073 (0x0815 TO 0x819)—SAFELOAD ADDRESS REGISTERS

Table 42. Safeload Address Registers Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	SA11	SA10	SA09	SA08	SA07	SA06	SA05	SA04	SA03	SA02	SA01	SA00	0x0000

Table 43.

Bit Name	Description
SA[11:0]	Safeload Address. Address of data that is to be loaded into the RAMs or registers.

2078 (0x081E)—SERIAL OUTPUT CONTROL REGISTER

Table 48. Serial Output Control Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	OLRP	OBP	M/S	OBF1	OBF0	OLF1	OLF0	FST	TDM	MSB2	MSB1	MSB0	OWL1	OWL0	0x0000

Table 49.

Bit Name	Description	
OLRP	OUTPUT_LRCLK Polarity. When this bit is set to 0, the left-channel data is clocked when OUTPUT_LRCLK is low and the right-channel data is clocked when OUTPUT_LRCLK is high. When this bit is set to 1, the right-channel data is clocked when OUTPUT_LRCLK is low and the left-channel data is clocked when OUTPUT_LRCLK is high.	
OBP	OUTPUT_BCLK Polarity. This bit controls on which edge of the bit clock the output data is clocked. Data changes on the falling edge of OUTPUT_BCLK when this bit is set to 0 and on the rising edge when this bit is set to 1.	
M/S	Master/Slave. This bit sets whether the output port is a clock master or slave. The default setting is slave; on power-up, the OUTPUT_BCLK and OUTPUT_LRCLK pins are set as inputs until this bit is set to 1, at which time they become clock outputs.	
OBF[1:0]	OUTPUT_BCLK Frequency (Master Mode Only). When the output port is being used as a clock master, these bits set the frequency of the output bit clock, which is divided down from an internal 1024 × f_S clock (49.152 MHz for a f_S of 48 kHz).	
	OBF[1:0]	**Setting**
	00	Internal clock/16
	01	Internal clock/8
	10	Internal clock/4
	11	Internal clock/2
OLF[1:0]	OUTPUT_LRCLK Frequency (Master Mode Only). When the output port is used as a clock master, these bits set the frequency of the output word clock on the OUTPUT_LRCLK pins, which is divided down from an internal 1024 × f_S clock (49.152 MHz for a f_S of 48 kHz).	
	OLF[1:0]	**Setting**
	00	Internal clock/1024
	01	Internal clock/512
	10	Internal clock/256
	11	Reserved
FST	Frame Sync Type. This bit sets the type of signal on the OUTPUT_LRCLK pins. When this bit is set to 0, the signal is a word clock with a 50% duty cycle; when this bit is set to 1, the signal is a pulse with a duration of one bit clock at the beginning of the data frame.	
TDM	TDM Enable. Setting this bit to 1 changes the output port from four serial stereo outputs to a single 8-channel TDM output stream on the SDATA_OUT0 pin (MP6).	
MSB[2:0]	MSB Position. These three bits set the position of the MSB of data with respect to the LRCLK edge. The data output of the ADAU1401 is always MSB first.	
	MSB[2:0]	**Setting**
	000	Delay by 1
	001	Delay by 0
	010	Delay by 8
	011	Delay by 12
	100	Delay by 16
	101	Reserved
	111	Reserved
OWL[1:0]	Output Word Length. These bits set the word length of the output data-word. All bits following the LSB are set to 0.	
	OWL[1:0]	**Setting**
	00	24 bits
	01	20 bits
	10	16 bits
	11	Reserved

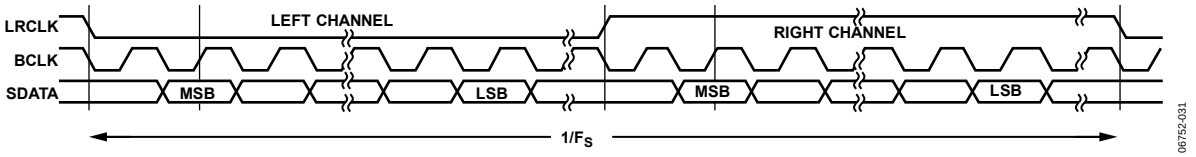

Figure 32. I²S Mode—16 Bits to 24 Bits per Channel

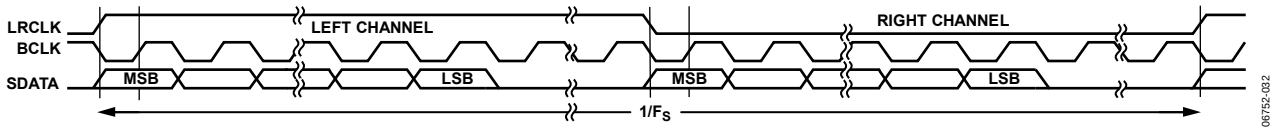

Figure 33. Left-Justified Mode—16 Bits to 24 Bits per Channel

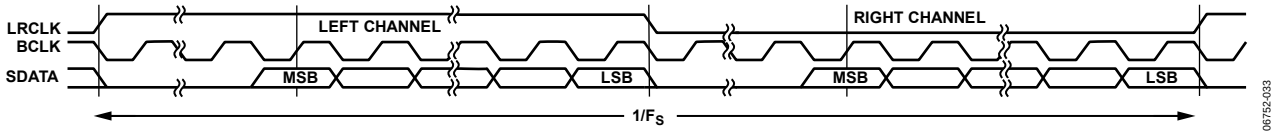

Figure 34. Right-Justified Mode—16 Bits to 24 Bits per Channel

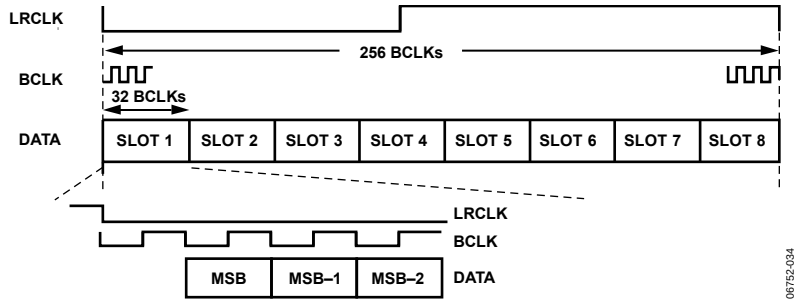

Figure 35. TDM Mode

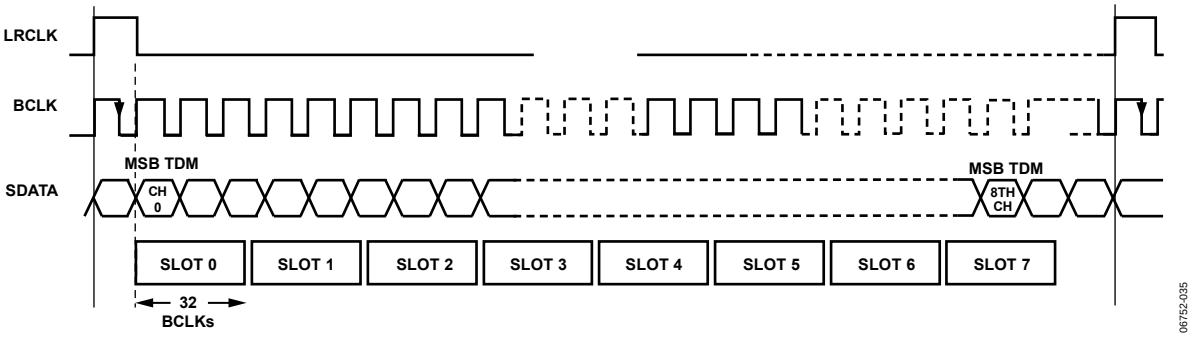

Figure 36. TDM Mode with Pulse Word Clock

TYPICAL APPLICATION SCHEMATICS

SELF-BOOT MODE

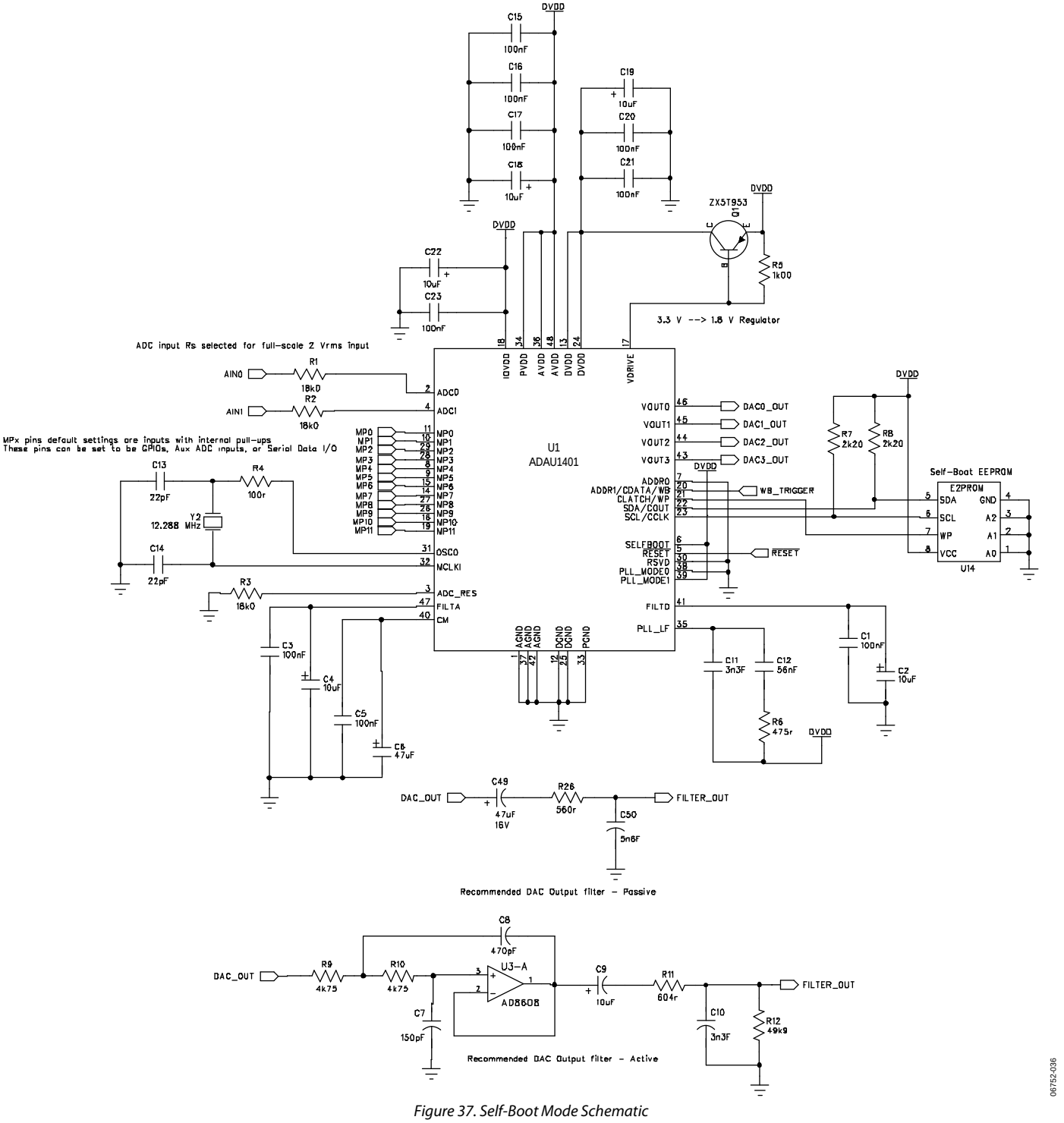

Figure 37. Self-Boot Mode Schematic