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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Sigma
Interface	I²C, SPI
Clock Rate	50MHz
Non-Volatile Memory	-
On-Chip RAM	12kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1401ystz

FUNCTIONAL BLOCK DIAGRAM

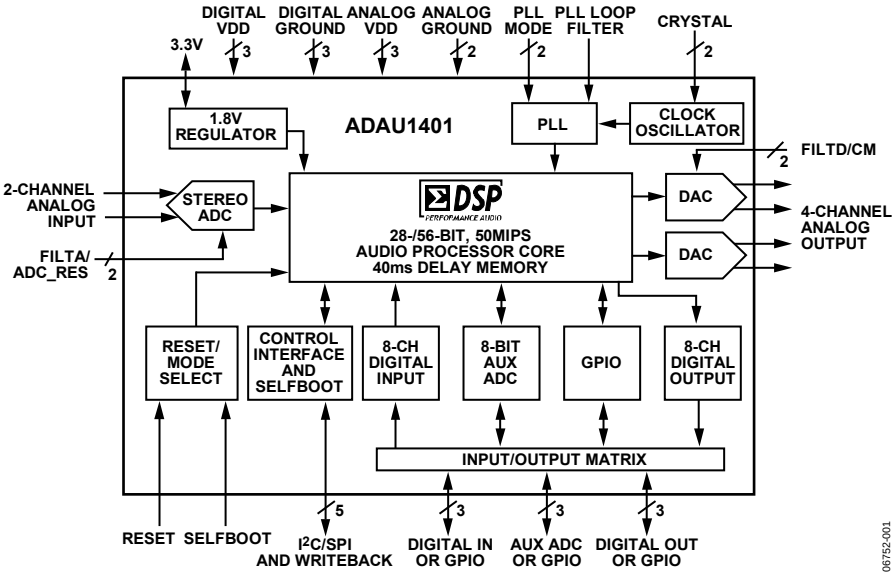

Figure 1.

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz, unless otherwise noted.

ANALOG PERFORMANCE

Specifications are guaranteed at 25°C (ambient).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		µA rms (µA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	95	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	99	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

DIGITAL INPUT/OUTPUT

Table 3.

Parameter	Min	Typ	Max[1]	Unit	Comments
Input Voltage, High (V_{IH})	2.0		IOVDD	V	
Input Voltage, Low (V_{IL})			0.8	V	
Input Leakage, High (I_{IH})			1	µA	Excluding MCLKI
Input Leakage, Low (I_{IL})			1	µA	Excluding MCLKI and bidirectional pins
Bidirectional Pin Pull-Up Current, Low			150	µA	
MCLKI Input Leakage, High (I_{IH})			3	µA	
MCLKI Input Leakage, Low (I_{IL})			3	µA	
High Level Output Voltage (V_{OH}), I_{OH} = 2 mA	2.0			V	
Low Level Output Voltage (V_{OL}), I_{OL} = 2 mA			0.8	V	
Input Capacitance			5	pF	
GPIO Output Drive		2		mA	

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

POWER

Table 4.

Parameter	Min	Typ	Max[1]	Unit
SUPPLY VOLTAGE				
Analog Voltage		3.3		V
Digital Voltage		1.8		V
PLL Voltage		3.3		V
IOVDD Voltage		3.3		V
SUPPLY CURRENT				
Analog Current (AVDD and PVDD)		50	85	mA
Digital Current (DVDD)		40	60	mA
Analog Current, Reset		35	55	mA
Digital Current, Reset		1.5	4.5	mA
DISSIPATION				
Operation (AVDD, DVDD, PVDD)[2]		286.5		mW
Reset, All Supplies		118		mW
POWER SUPPLY REJECTION RATIO (PSRR)				
1 kHz, 200 mV p-p Signal at AVDD		50		dB

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.
[2] Power dissipation does not include IOVDD power because the current drawn from this supply is dependent on the loads at the digital output pins.

TEMPERATURE RANGE

Table 5.

Parameter	Min	Typ	Max	Unit
Functionality Guaranteed	−40		+105	°C ambient

PLL AND OSCILLATOR

Table 6. PLL and Oscillator[1]

Parameter	Min	Typ	Max	Unit
PLL Operating Range	MCLK_Nom − 20%		MCLK_Nom + 20%	MHz
PLL Lock Time			20	ms
Crystal Oscillator Transconductance (g_m)		78		mmho

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

Parameter	Limit t_{MIN}	Limit t_{MAX}	Unit	Description
MULTIPURPOSE PINS AND RESET				
t_{GRT}		50	ns	GPIO rise time
t_{GFT}		50	ns	GPIO fall time
t_{GIL}		$1.5 \times 1/f_S$	µs	GPIO input latency; time until high/low value is read by core
t_{RLPW}	20		ns	$\overline{\text{RESET}}$ low pulse width

[1] All timing specifications are given for the default (I^2S) states of the serial input port and the serial output port (see Table 66).

Digital Timing Diagrams

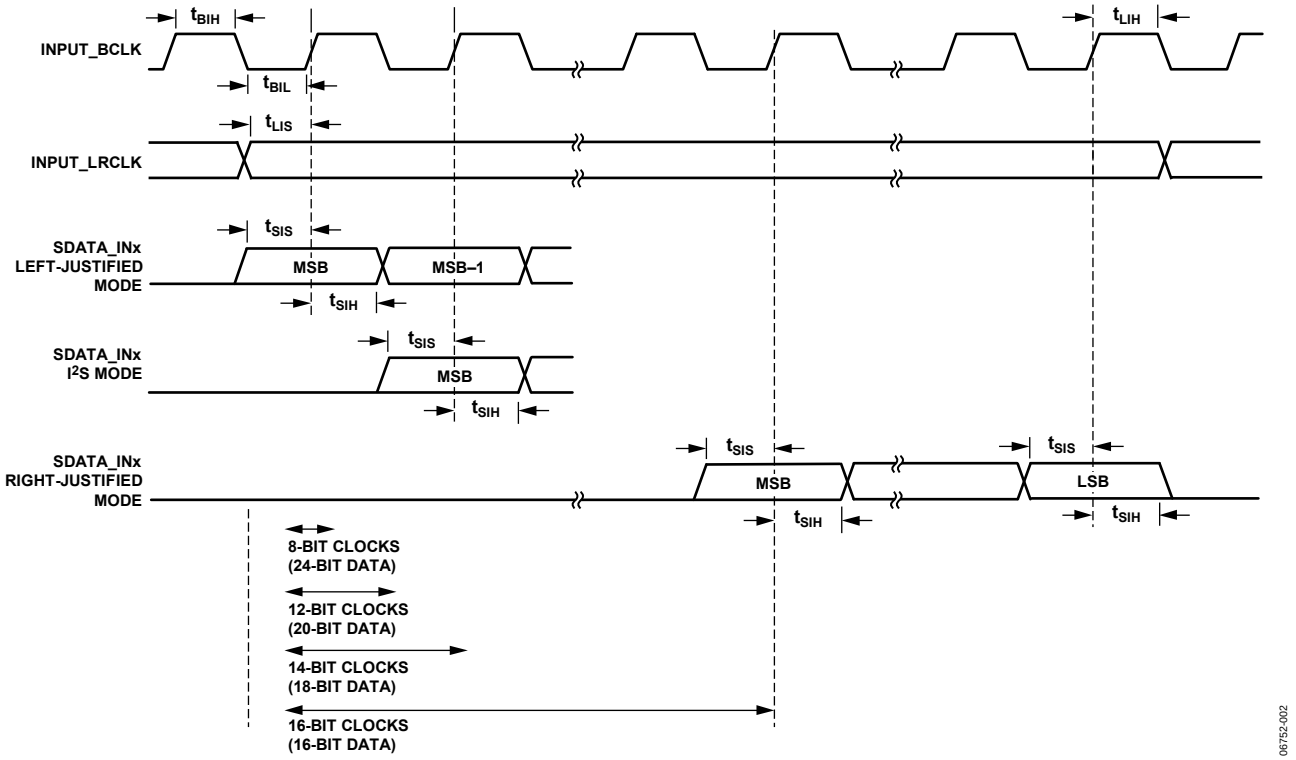

Figure 2. Serial Input Port Timing

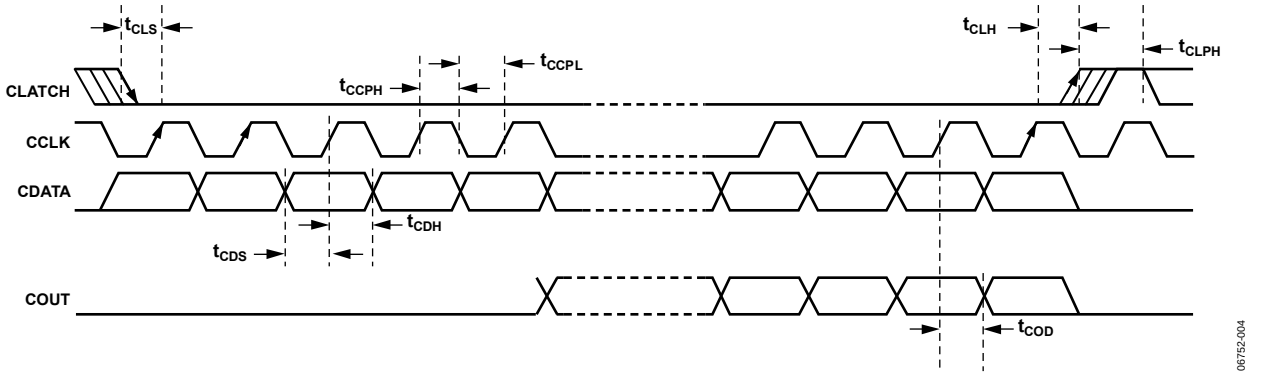

Figure 3. SPI Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
DVDD to GND	0 V to 2.2 V
AVDD to GND	0 V to 4.0 V
IOVDD to GND	0 V to 4.0 V
Digital Inputs	DGND − 0.3 V, IOVDD + 0.3 V
Maximum Junction Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP	72	19.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

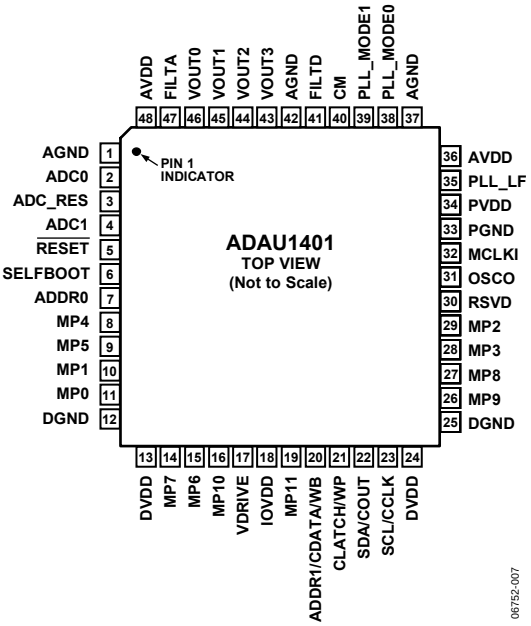

Figure 7. 48-Lead LQFP Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 37, 42	AGND	PWR	Analog Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. AGND should be decoupled to an AVDD pin with a 100 nF capacitor.
2	ADC0	A_IN	Analog Audio Input 0. Full-scale 100 µA rms input. Current input allows input voltage level to be scaled with an external resistor. An 18 kΩ resistor gives a 2 V rms full-scale input.
3	ADC_RES	A_IN	ADC Reference Current. The full-scale current of the ADCs can be set with an external 18 kΩ resistor connected between this pin and ground. See the Audio ADCS section for details.
4	ADC1	A_IN	Analog Audio Input 1. Full-scale 100 µA rms input. Current input allows input voltage level to be scaled with an external resistor. An 18 kΩ resistor gives a 2 V rms full-scale input. See the Audio ADCS section for details.
5	$\overline{\text{RESET}}$	D_IN	Active Low Reset Input. Reset is triggered on a high-to-low edge, and the ADAU1401 exits reset on a low-to-high edge. For more information about initialization, see the Power-Up Sequence section for details.
6	SELFBOOT	D_IN	Enable/Disable Self-Boot. SELFBOOT selects control port (low) or self-boot (high). Setting this pin high initiates a self-boot operation when the ADAU1401 is brought out of a reset. This pin can be tied directly to the control voltage or pulled up/down with a resistor. See the Self-Boot section for details.
7	ADDR0	D_IN	I^2C and SPI Address 0. In combination with ADDR1, this pin allows up to four ADAU1401s to be used on the same I^2C bus and up to two ICs to be used with a common SPI CLATCH signal. See the I^2C Port section for details.
8	MP4	D_IO	Multipurpose GPIO or Serial Input Port LRCLK (INPUT_LRCLK). See the Multipurpose Pins section for more details.
9	MP5	D_IO	Multipurpose GPIO or Serial Input Port BCLK (INPUT_BCLK). See the Multipurpose Pins section for more details.
10	MP1	D_IO	Multipurpose GPIO or Serial Input Port Data 1 (SDATA_IN0). See the Multipurpose Pins section for more details.
11	MP0	D_IO	Multipurpose GPIO or Serial Input Port Data 0 (SDATA_IN1). See the Multipurpose Pins section for more details.
12, 25	DGND	PWR	Digital Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. DGND should be decoupled to a DVDD pin with a 100 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

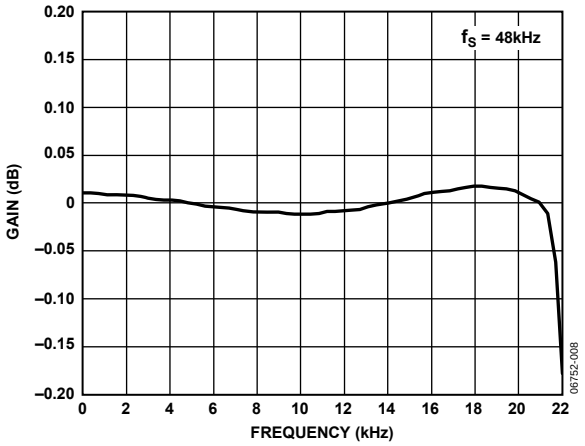

Figure 8. ADC Pass-Band Filter Response

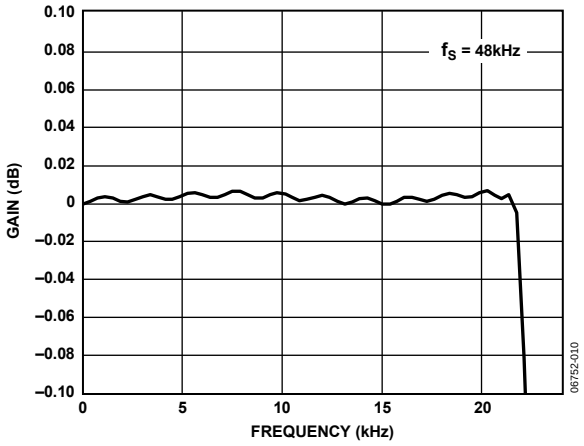

Figure 10. DAC Pass-Band Filter Response

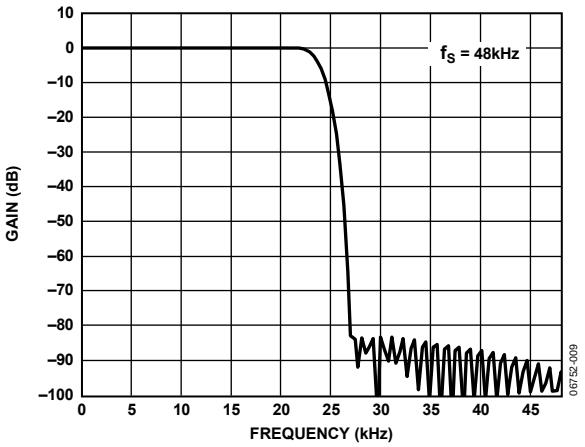

Figure 9. ADC Stop-Band Filter Response

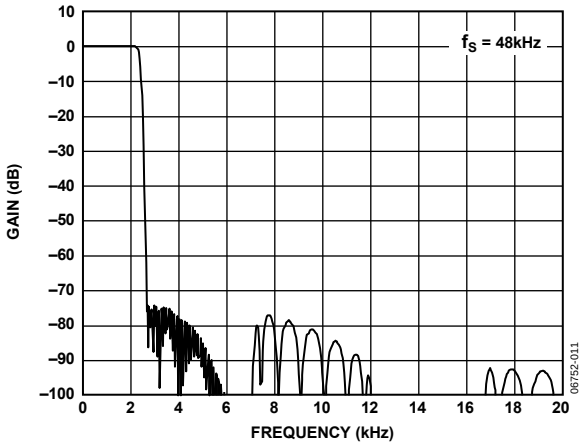

Figure 11. DAC Stop-Band Filter Response

THEORY OF OPERATION

The core of the ADAU1401 is a 28-bit DSP (56-bit with double-precision processing) optimized for audio processing. The program and parameter RAMs can be loaded with a custom audio processing signal flow built by using SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows for transparent parameter updates and prevents clicks in the output signals.

The program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1401 can self-boot on startup. In this standalone mode, parameters can be controlled through the on-board multipurpose pins. The ADAU1401 can accept controls from switches, potentiometers, rotary encoders, and IR receivers. Parameters such as volume and tone settings can be saved to the EEPROM on power-down and recalled again on power-up.

The ADAU1401 can operate with digital or analog inputs and outputs, or a mix of both. The stereo ADC and four DACs each have an SNR of at least +100 dB and a THD + N of at least −83 dB. The 8-channel, flexible serial data input/output ports allow glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers and transmitters, and sample rate converters. The serial ports of the ADAU1401 can be configured in I²S, left-justified, right-justified, or TDM serial port compatible modes.

Twelve multipurpose (MP) pins allow the ADAU1401 to receive external control signals as input and to output flags or controls to other devices in the system. The MP pins can be configured as digital I/Os, inputs to the 4-channel auxiliary ADC, or serial data I/O ports. As inputs, they can be connected to buttons, switches, rotary encoders, potentiometers, IR receivers, or other external circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs, control other ICs, or connect to other external circuitry in an application.

The ADAU1401 has a sophisticated control port that supports complete read/write capability of all memory locations. Control registers are provided to offer complete control of the configuration and serial modes of the chip. The ADAU1401 can be configured for either SPI or I²C control, or can self-boot from an external EEPROM.

An on-board oscillator can be connected to an external crystal to generate the master clock. In addition, a master clock phase-locked loop (PLL) allows the ADAU1401 to be clocked from a variety of different clock speeds. The PLL can accept inputs of $64 \times f_S$, $256 \times f_S$, $384 \times f_S$, or $512 \times f_S$ to generate the internal master clock of the core.

The SigmaStudio software is used to program and control the SigmaDSP® through the control port. Along with designing and tuning a signal flow, the tools can be used to configure all of the DSP registers and burn a new program into the external EEPROM. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design a DSP signal flow and port it to a target application. At the same time, it provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, dynamics processors, mixers, and delays), compile the design, and load the program and parameter files into the ADAU1401 memory through the control port. Signal processing blocks available in the provided libraries include

- Single- and double-precision biquad filters
- Processors with peak or rms detection for monochannel and multichannel dynamics
- Mixers and splitters
- Tone and noise generators
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone sources
- FIR filters
- Level detectors
- GPIO control and conditioning

Additional processing blocks are always being developed. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

The ADAU1401 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply. It is fabricated on a single monolithic, integrated circuit and is packaged in a 48-lead LQFP for operation over the −40°C to +105°C temperature range.

INITIALIZATION

This section details the procedure for properly setting up the ADAU1401. The following five-step sequence provides an overview of how to initialize the IC:

1. Apply power to ADAU1401.
2. Wait for PLL to lock.
3. Load SigmaDSP program and parameters.
4. Set up registers (including multipurpose pins and digital interfaces).
5. Turn off the default muting of the converters, clear the data registers, and initialize the DAC setup register (see the Control Registers Setup section for specific settings).

To only test analog audio pass-through (ADCs to DACs), skip Step 3 and Step 4 and use the default internal program.

POWER-UP SEQUENCE

The ADAU1401 has a built-in power-up sequence that initializes the contents of all internal RAMs on power-up or when the device is brought out of a reset. On the positive edge of $\overline{\text{RESET}}$, the contents of the internal program boot ROM are copied to the internal program RAM memory, the parameter RAM is filled with values (all 0s) from its associated boot ROM, and all registers are initialized to 0s. The default boot ROM program copies audio from the inputs to the outputs without processing it (see Figure 13). In this program, serial digital Input 0 and Input 1 are output on DAC0 and DAC1 and serial digital Output 0 and Output 1. ADC0 and ADC1 are output on DAC2 and DAC3. The data memories are also zeroed at power-up. New values should not be written to the control port until the initialization is complete.

Table 12. Power-Up Time

MCLKI Input	Init. Time	Max Program/ Parameter/Register Boot Time (I^2C)	Total
3.072 MHz (64 × f_S)	85 ms	175 ms	260 ms
11.289 MHz (256 × f_S)	23 ms	175 ms	198 ms
12.288 MHz (256 × f_S)	21 ms	175 ms	196 ms
18.432 MHz (384 × f_S)	16 ms	175 ms	191 ms
24.576 MHz (512 × f_S)	11 ms	175 ms	186 ms

The PLL start-up time lasts for 2^{18} cycles of the clock on the MCLKI pin. This time ranges from 10.7 ms for a 24.576 MHz (512 × f_S) input clock to 85.3 ms for a 3.072 MHz (64 × f_S) input clock and is measured from the rising edge of $\overline{\text{RESET}}$. Following the PLL startup, the duration of the ADAU1401 boot cycle is about 42 µs for a f_S of 48 kHz. The user should avoid writing to or reading from the ADAU1401 during this start-up time. For an MCLK input of 12.288 MHz, the full initialization sequence (PLL startup plus boot cycle) is approximately 21 ms. As the device comes out of a reset, the clock mode is immediately set by the PLL_MODE0 and PLL_MODE1 pins. The reset is synchronized to the falling edge of the internal clock.

Table 12 lists typical times to boot the ADAU1401 into an operational state of an application, assuming a 400 kHz I^2C clock loading a full program, parameter set, and all registers (about 8.5 kB). In reality, most applications do not fill the RAMs and therefore boot time (Column 3 of Table 12) is less.

CONTROL REGISTERS SETUP

The following registers must be set as described in this section to initialize the ADAU1401. These settings are the basic minimum settings needed to operate the IC with an analog input/output of 48 kHz. More registers may need to be set, depending on the application. See the RAMs and Registers section for additional settings.

DSP Core Control Register (Address 2076)

Set Bits[4:2] (ADM, DAM, and CR) each to 1.

DAC Setup Register (Address 2087)

Set Bits[0:1] (DS[1:0]) to 01.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURE

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing in the audio output.

1. Set Bit 3 and Bit 4 (active low) of the core control register to 1 to mute the ADCs and DACs. This begins a volume ramp-down.
2. Set Bit 2 (active low) of the core control register to 1. This zeroes the SigmaDSP accumulators, the data output registers, and the data input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Deassert Bit 2 to Bit 4 of the core control register.

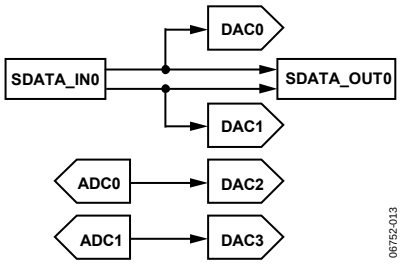

Figure 13. Default Program Signal Flow

POWER REDUCTION MODES

Sections of the ADAU1401 chip can be turned on and off as needed to reduce power consumption. These include the ADCs, DACs, and voltage reference.

The individual analog sections can be turned off by writing to the auxiliary ADC and power control register. By default, the ADCs, DACs, and reference are enabled (all bits set to 0). Each of these can be turned off by writing a 1 to the appropriate bits

in this register. The ADC power-down mode powers down both ADCs, and each DAC can be powered down individually. The current savings is about 15 mA when the ADCs are powered down and about 4 mA for each DAC that is powered down. The voltage reference, which is supplied to both the ADCs and DACs, should only be powered down if all ADCs and DACs are powered down. The reference is powered down by setting both Bit 6 and Bit 7 of the control register.

USING THE OSCILLATOR

The ADAU1401 can use an on-board oscillator to generate its master clock. The oscillator is designed to work with a 256 × f_S master clock, which is 12.288 MHz for a f_S of 48 kHz and 11.2896 MHz for a f_S of 44.1 kHz. The crystal in the oscillator circuit should be an AT-cut, parallel resonator operating at its fundamental frequency. Figure 14 shows the external circuit recommended for proper operation.

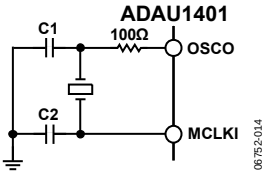

Figure 14. Crystal Oscillator Circuit

The 100 Ω damping resistor on OSCO gives the oscillator a voltage swing of approximately 2.2 V. The crystal shunt capacitance should be 7 pF. Its load capacitance should be about 18 pF, although the circuit supports values of up to 25 pF. The necessary values of the C1 and C2 load capacitors can be calculated from the crystal load capacitance as follows:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where C_{stray} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

OSCO should not be used to directly drive the crystal signal to another IC. This signal is an analog sine wave, and it is not appropriate to use it to drive a digital input. There are two options for using the ADAU1401 to provide a master clock to other ICs in the system. The first, and less recommended, method is to use a high impedance input digital buffer on the OSCO signal. If this is done, minimize the trace length to the buffer input. The second method is to use a clock from the serial output port. Pin MP11 can be set as an output (master) clock divided down from the internal core clock. If this pin is set to serial output port (OUTPUT_BCLK) mode in the multipurpose pin configuration register (2081) and the port is set to master in the serial output control register (2078), the desired output frequency can also be set in the serial output control register with Bits[OBF<1:0>] (see Table 49).

If the oscillator is not utilized in the design, it can be powered down to save power. This can be done if a system master clock is already available in the system. By default, the oscillator is powered on. The oscillator powers down when a 1 is written to the OPD bit of the oscillator power-down register (see Table 60).

SETTING MASTER CLOCK/PLL MODE

The MCLKI input of the ADAU1401 feeds a PLL, which generates the 50 MIPS SigmaDSP core clock. In normal operation, the input to MCLKI must be one of the following: 64 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S, where f_S is the input sampling rate. The mode is set on PLL_MODE0 and PLL_MODE1 as described in Table 13. If the ADAU1401 is set to receive double-rate signals (by reducing the number of program steps per sample by a factor of 2 using the core control register), the master clock frequency must be 32 × f_S, 128 × f_S, 192 × f_S, or 256 × f_S. If the ADAU1401 is set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the core control register), the master clock frequency must be 16 × f_S, 64 × f_S, 96 × f_S, or 128 × f_S. On power-up, a clock signal must be present on the MCLKI pin so that the ADAU1401 can complete its initialization routine.

Table 13. PLL Modes

MCLKI Input	PLL_MODE0	PLL_MODE1
64 × f_S	0	0
256 × f_S	0	1
384 × f_S	1	0
512 × f_S	1	1

The clock mode should not be changed without also resetting the ADAU1401. If the mode is changed during operation, a click or pop can result in the output signals. The state of the PLL_MODEx pins should be changed while $\overline{\text{RESET}}$ is held low.

The PLL loop filter should be connected to the PLL_LF pin. This filter, shown in Figure 15, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for the capacitors. The 3.3 V signal shown in Figure 15 can be connected to the AVDD supply of the chip.

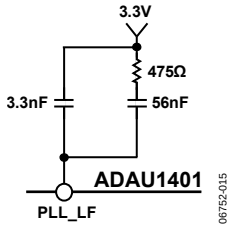

Figure 15. PLL Loop Filter

CONTROL PORTS

The ADAU1401 can operate in one of three control modes:

- I²C control
- SPI control
- Self-boot (no external controller)

The ADAU1401 has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOOT pin is low at power-up, the part defaults to I²C mode but can be put into SPI control mode by pulling the CLATCH/WP pin low three times. When the SELFBOOT pin is set high at power-up, the ADAU1401 loads its program, parameters, and register settings from an external EEPROM on startup.

The control port is capable of full read/write operation for all addressable memory and registers. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in a single-address mode or a burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1401. This subaddress must be two bytes because the memory locations within the ADAU1401 are directly addressable and their sizes exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. The exact formats for specific types of writes are shown in Table 22 to Table 31.

The ADAU1401 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. If large blocks of data need to be downloaded, the output of the DSP core can be halted (using the CR bit in the DSP core control register (Address 2076)), new data can be loaded, and then the device can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 15 details these multiple functions.

Table 15. Control Port Pins and SELFBOOT Pin Functions

Pin	I²C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open-collector output	COUT—output	SDA—open-collector output
ADDR1/CDATA/WB	ADDR1—input	CDATA—input	WB—writeback trigger
CLATCH/WP	Unused input—tie to ground or IOVDD	CLATCH—input	WP—EEPROM write protect, open-collector output
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or IOVDD

SIGNAL PROCESSING

The ADAU1401 is designed to provide all audio signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using the SigmaStudio software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic data. The input and output word lengths of the DSP core are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

NUMERIC FORMATS

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1401 uses the same numeric format for both the parameter and data values. The format is as follows.

Numerical Format: 5.23

Linear range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 0011 0011 0011 0011 0011 = −0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 − 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without internal clipping.

A digital clipper circuit is used between the output of the DSP core and the DACs or serial port outputs (see Figure 29). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to −1.0. Figure 29 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

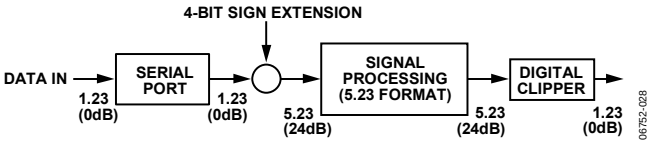

Figure 29. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the ADAU1401 default program passes the unprocessed input signals to the outputs (shown in Figure 13), but the outputs are muted by default (see the Power-Up Sequence section). There are 1024 instruction cycles per audio sample, resulting in about 50 MIPS available. The SigmaDSP runs in a stream-oriented manner, meaning that all 1024 instructions are executed each sample period. The ADAU1401 can also be set up to accept double- or quad-speed inputs by reducing the number of instructions per sample that are set in the core control register.

The part can be easily programmed using SigmaStudio (Figure 30), a graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required. More information about SigmaStudio can be found at www.analog.com.

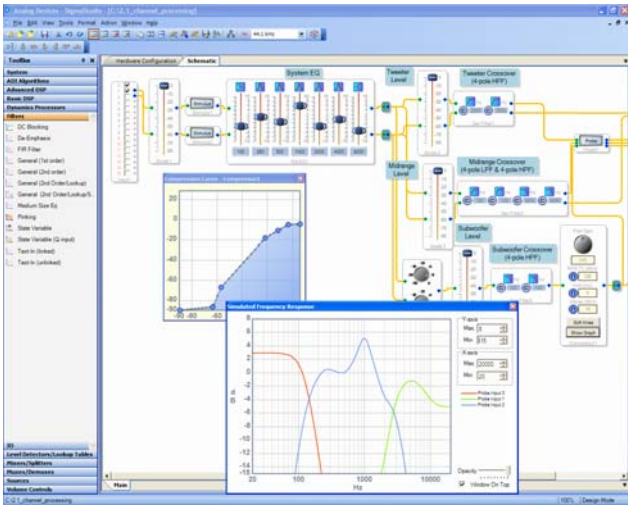

Figure 30. SigmaStudio Screen Shot

Table 22. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]
chip_adr[6:0], $\overline{W}$/R	000000, param_adr[9:8]	param_adr[7:0]	0000, param[27:24]	param[23:0]

Table 23. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]	Bytes[7:10]	Bytes[11:14]
chip_adr[6:0], $\overline{W}$/R	000000, param_adr[9:8]	param_adr[7:0]	0000, param[27:24]	param[23:0]		
			<—param_adr—>		param_adr + 1	param_adr + 2

Table 24. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes[3:7]
chip_adr[6:0], $\overline{W}$/R	00000, prog_adr[10:8]	prog_adr[7:0]	prog[39:0]

Table 25. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes[3:7]	Bytes[8:12]	Bytes[13:17]
chip_adr[6:0], $\overline{W}$/R	00000, prog_adr[10:8]	prog_adr[7:0]	prog[39:0]		
			<—prog_adr—>	prog_adr + 1	prog_adr + 2

Table 26. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[15:8]	data[7:0]

Table 27. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte 1	Byte 2	Byte 3
chip_adr[6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[7:0]

Table 28. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	000, progCount[10:6][1]	progCount[5:0][1], regSel[1:0][2]

[1] progCount[10:0] is the value of the program counter when the data capture occurs (the table of values is generated by the SigmaStudio compiler).
[2] regSel[1:0] selects one of four registers (see the 2074 to 2075 (0x081A to 0x081B)—Data Capture Registers section).

Table 29. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes[3:5]
chip_adr[6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	data[23:0]

Table 30. Safeload Address Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr[6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	000000, param_adr[9:8]	param_adr[7:0]

Table 31. Safeload Data Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Bytes[5:7]
chip_adr[6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	00000000	0000, data[27:24]	data[23:0]

CONTROL REGISTER DETAILS

2048 TO 2055 (0x0800 TO 0x0807)—INTERFACE REGISTERS

The interface registers are used in self-boot mode to save parameters that need to be written to the external EEPROM. The ADAU1401 then recalls these parameters from the EEPROM after the next reset or power-up. Therefore, system parameters such as volume and EQ settings can be saved during power-down and recalled the next time the system is turned on.

There are eight 32-bit interface registers, which allow eight 28-bit (plus zero-padding) parameters to be saved. The parameters to be saved in these registers are selected in the graphical programming tools. These registers are updated with their corresponding parameter RAM data once per sample period.

An edge, which can be set to be either rising or falling, triggers the ADAU1401 to write the current contents of the interface registers to the EEPROM. See the Self-Boot section for details.

The user can write directly to the interface registers after the interface registers control port write mode (IFCW) in the DSP core control register has been set. In this mode, the data in the registers is written from the control port, not from the DSP core.

Table 33. Interface Register Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D23 D7	D22 D6	D21 D5	D20 D4	D19 D3	D18 D2	D17 D1	D16 D0	Default
0	0	0	0	IF27	IF26	IF25	IF24	IF23	IF22	IF21	IF20	IF19	IF18	IF17	IF16	0x0000
IF15	IF14	IF13	IF12	IF11	IF10	IF09	IF08	IF07	IF06	IF05	IF04	IF03	IF02	IF01	IF00	0x0000

Table 34.

Bit Name	Description
IF[27:0]	Interface register 28-bit parameter

2056 (0x808)—GPIO PIN SETTING REGISTER

This register allows the user to set the GPIO pins through the control port. High or low settings can be directly written to or read from this register after setting the GPIO pin setting register control port write mode (GPCW) in the core control register. This register is updated once every LRCLK frame ($1/f_S$).

Table 35. GPIO Pin Setting Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	MP11	MP10	MP09	MP08	MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	0x0000

Table 36.

Bit Name	Description
MP[11:0]	Setting of multipurpose pin when controlled through SPI or I^2C

2074 TO 2075 (0x081A TO 0x081B)—DATA CAPTURE REGISTERS

The ADAU1401 data capture feature allows the data at any node in the signal processing flow to be sent to one of two readable registers. This feature is useful for monitoring and displaying information about internal signal levels or compressor/limiter activity.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 1023 that corresponds to the program step number where the capture is to occur. The register select field programs one of four registers in the DSP core that transfers this information to the data capture register when the program counter reaches this step.

The captured data is in 5.19, twos complement data format, which comes from the internal 5.23 data-word with the four LSBs truncated.

The data that must be written to set up the data capture is a concatenation of the 10-bit program count index with the 2-bit register select field. The capture count and register select values that correspond to the desired point to be monitored in the signal processing flow can be found in a file output from the program compiler. The capture registers can be accessed by reading from Location 2074 and Location 2075. The format for writing and reading to the data capture registers is shown in Table 28 and Table 29.

Table 44. Safeload Data Registers Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	PC09	PC08	PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00	RS01	RS00	0x0000

Table 45.

Bit Name	Description	
PC[9:0]	10-bit program counter address	
RS[1:0]	Select the register to be transferred to the data capture output	
	RS[1:0]	**Register**
	00	Multiplier X input (Mult_X_input)
	01	Multiplier Y input (Mult_Y_input)
	10	Multiplier-accumulator output (MAC_out)
	11	Accumulator feedback (Accum_fback)

2079 (0x081F)—SERIAL INPUT CONTROL REGISTER

Table 50. Serial Input Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	ILP	IBP	M2	M1	M0	0x00

Table 51.

Bit Name	Description	
ILP	INPUT_LRCLK Polarity. When this bit is set to 0, the left-channel data on the SDATA_INx pins is clocked when INPUT_LRCLK is low and the right-channel data is clocked when INPUT_LRCLK is high. When this bit is set to 1, the clocking of these channels is reversed. In TDM mode when this bit is set to 0, data is clocked in, starting with the next appropriate BCLK edge (set in Bit 3 of this register) after a falling edge on the INPUT_LRCLK pin. When this bit is set to 1 and the device is running in TDM mode, the input data is valid on the BCLK edge after a rising edge on the word clock (INPUT_LRCLK). INPUT_LRCLK can also operate with a pulse input, rather than a clock. In this case, the first edge of the pulse is used by the ADAU1401 to start the data frame. When this polarity bit is set to 0, a low pulse should be used; when the bit it set to 1, a high pulse should be used.	
IBP	INPUT_BCLK Polarity. This bit controls on which edge of the bit clock the input data changes and on which edge it is clocked. Data changes on the falling edge of INPUT_BCLK when this bit is set to 0 and on the rising edge when this bit is set at 1.	
M[2:0]	Serial Input Mode. These two bits control the data format that the input port expects to receive. Bit 3 and Bit 4 of this control register override the settings of Bits[2:0]; therefore, all four bits must be changed together for proper operation in some modes. The clock diagrams for these modes are shown in Figure 32, Figure 33, and Figure 34. Note that for left-justified and right-justified modes, the LRCLK polarity is high and then low, which is the opposite of the default setting for ILP. When these bits are set to accept a TDM input, the ADAU1401 data starts after the edge defined by ILP. The ADAU1401 TDM data stream should be input on Pin SDATA_IN0. Figure 35 shows a TDM stream with a high-to-low triggered LRCLK and data changing on the falling edge of the BCLK. The ADAU1401 expects the MSB of each data slot to be delayed by one BCLK from the beginning of the slot, as it would in stereo I²S format. In TDM mode, Channel 0 to Channel 3 are in the first half of the frame, and Channel 4 to Channel 7 are in the second half. Figure 36 shows an example of a TDM stream running with a pulse word clock, which is used to interface to ADI codecs in auxiliary mode. To work in this mode with either the input or output serial ports, set the ADAU1401 to begin the frame on the rising edge of LRCLK, to change data on the falling edge of BCLK, and to delay the MSB position from the start of the word clock by one BCLK.	
	M[2:0]	**Setting**
	000	I²S
	001	Left-justified
	010	TDM
	011	Right-justified, 24 bits
	100	Right-justified, 20 bits
	101	Right-justified, 18 bits
	110	Right- justified, 16 bits
	111	Reserved

MULTIPURPOSE PINS

The ADAU1401 has 12 multipurpose (MP) pins that can be individually programmed to be used as serial data inputs, serial data outputs, digital control inputs/outputs to and from the SigmaDSP core, or inputs to the 4-channel auxiliary ADC. These pins allow the ADAU1401 to be used with external ADCs and DACs. They also use analog or digital inputs to control settings such as volume control, or use output digital signals to drive LED indicators. Every MP pin has an internal 15 kΩ pull-up resistor.

AUXILIARY ADC

The ADAU1401 has a 4-channel, auxiliary, 8-bit ADC that can be used in conjunction with a potentiometer to control volume, tone, or other parameter settings in the DSP program. Each of the four channels is sampled at the audio sampling frequency (f_S). Full-scale input on this ADC is 3.0 V, so the step size is approximately 12 mV (3.0 V/256 steps). The input resistance of the ADC is approximately 30 kΩ. Table 63 indicates which four MP pins are mapped to the four channels of the auxiliary ADC. The auxiliary ADC is enabled for those pins by writing 1111 to the appropriate portion of the multipurpose pin configuration registers.

The auxiliary ADC is turned on by setting the AAEN bit of the auxiliary ADC enable register (see Table 58).

Noise on the ADC input can cause the digital output to constantly change by a few LSBs. If the auxiliary ADC is used to control volume, this constant change causes small gain fluctuations. To avoid this, add a low-pass filter or hysteresis to the auxiliary ADC signal path by enabling either function in the auxiliary ADC and power control register (2082), as described in Table 56. The filter is enabled by default when the auxiliary ADC is enabled. When data is read from the auxiliary ADC registers, two bytes (12 bits of data, plus zero-padded LSBs) are available because of this filtering.

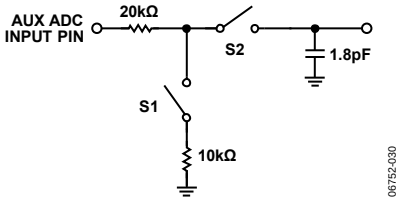

Figure 31. Auxiliary ADC Input Circuit

Figure 31 shows the input circuit for the auxiliary ADC. Switch S1 enables the auxiliary ADC and is set by Bit 15 of the auxiliary ADC enable register. The sampling switch, S2, operates at the audio sampling frequency.

The auxiliary ADC data registers can be written to directly after AACW in the DSP core control register has been set. In this mode, the voltages on the analog inputs are not written into the registers, but rather the data in the registers is written from the control port.

PVDD supplies the 3.3 V power for the auxiliary ADC analog input. The digital core of the auxiliary ADC is powered with the 1.8 V DVDD signal.

Table 63. Multipurpose Pin Auxiliary ADC Mapping

Multipurpose Pin	Function
MP0	N/A
MP1	N/A
MP2	ADC1
MP3	ADC2
MP4	N/A
MP5	N/A
MP6	N/A
MP7	N/A
MP8	ADC3
MP9	ADC0
MP10	N/A
MP11	N/A

GENERAL-PURPOSE INPUT/OUTPUT PINS

The general-purpose input/output (GPIO) pins can be used as either inputs or outputs. These pins are readable and can be set either through the control interface or directly by the SigmaDSP core. When set as inputs, these pins can be used with push-button switches or rotary encoders to control DSP program settings. Digital outputs can be used to drive LEDs or external logic to indicate the status of internal signals and control other devices. Examples of this use include indicating signal overload, signal present, and button press confirmation.

When set as an output, each pin can typically drive 2 mA. This is enough current to directly drive some high efficiency LEDs. Standard LEDs require about 20 mA of current and can be driven from a GPIO output with an external transistor or buffer. Because of issues that could arise from simultaneously driving or sinking a large current on many pins, care should be taken in the application design to avoid connecting high efficiency LEDs directly to many or all of the MPx pins. If many LEDs are required, use an external driver.

When the GPIO pins are set as open-collector outputs, they should be pulled up to a maximum voltage of 3.3 V (the voltage on IOVDD).

SERIAL DATA INPUT/OUTPUT PORTS

The flexible serial data input and output ports of the ADAU1401 can be set to accept or transmit data in 2-channel format or in an 8-channel TDM stream. Data is processed in twos complement, MSB-first format. The left-channel data field always precedes the right-channel data field in the 2-channel streams. In TDM mode, Slot 0 to Slot 3 are in the first half of the audio frame, and Slot 4 to Slot 7 are in the second half of the frame. TDM mode allows fewer multipurpose pins to be used, freeing more pins for other functions. The serial modes are set in the serial output and serial input control registers.

LAYOUT RECOMMENDATIONS

PARTS PLACEMENT

The ADC input voltage-to-current resistors and the ADC current set resistor should be placed as close as possible to the 2, 3, and 4 input pins.

All 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power/ground pair, should be placed as close as possible to the ADAU1401. The 3.3 V and 1.8 V signals on the board should also each be bypassed with a single bulk capacitor (10 µF to 47 µF).

All traces in the crystal oscillator circuit (Figure 14) should be kept as short as possible to minimize stray capacitance. In addition, avoid long board traces connected to any of these components because such traces may affect crystal startup and operation.

GROUNDING

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.

I²C CONTROL

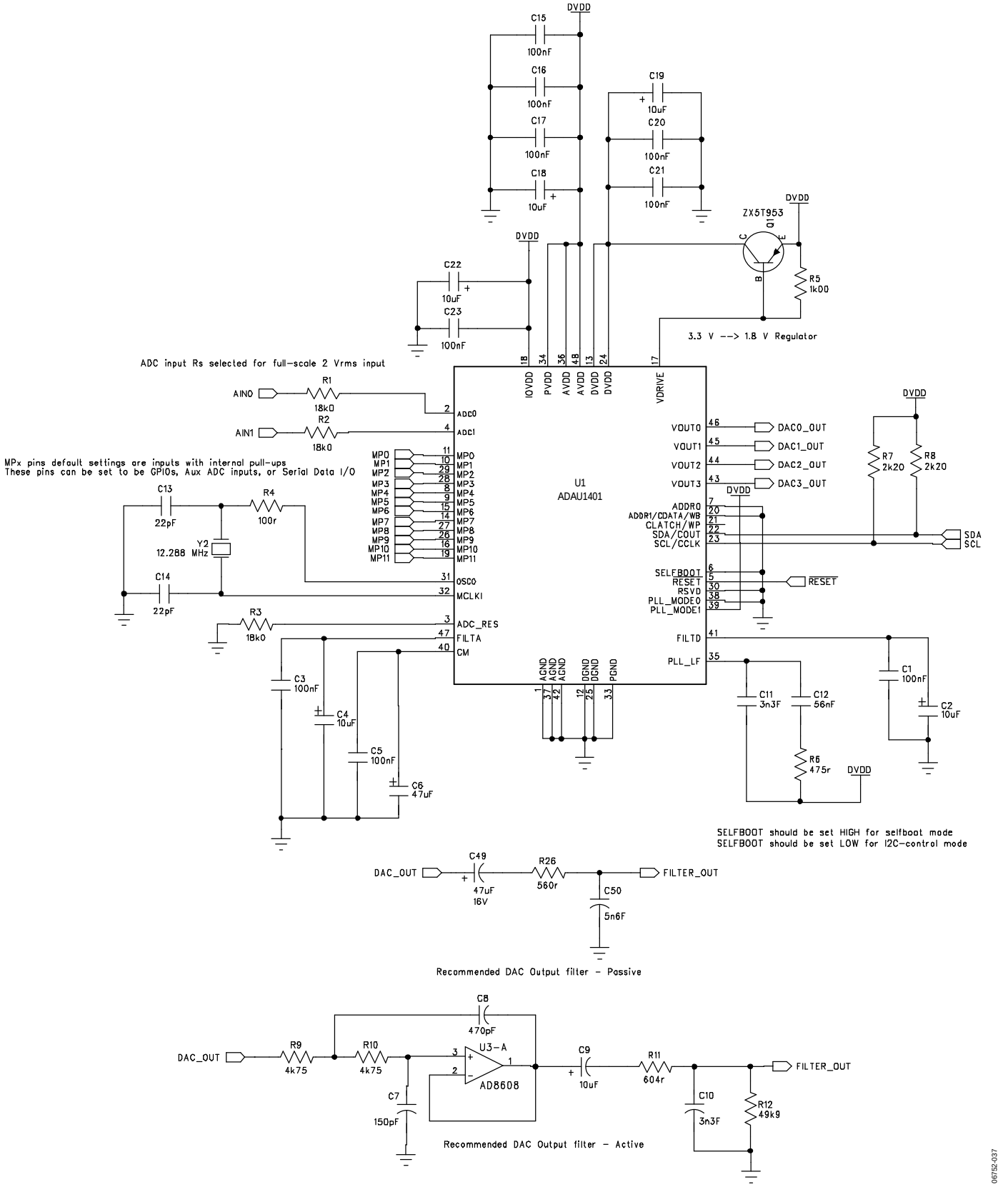

Figure 38. I²C Control Schematic