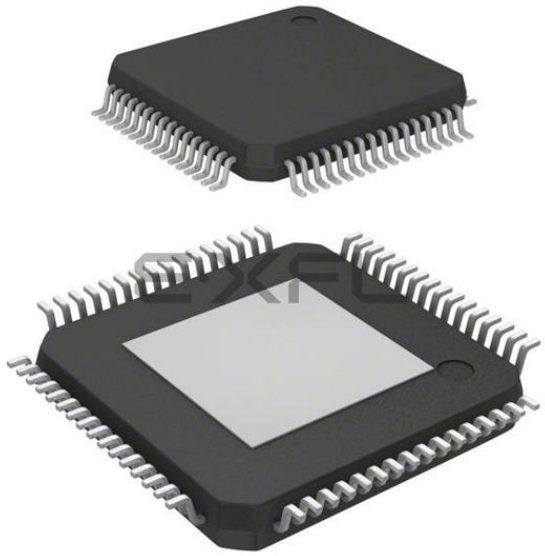

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Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
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Supplier Device Package	64-LQFP (10x10)
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1.7.5 PE[1:0] — Port E I/O signals

PE[1:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull down devices are enabled.

1.7.6 PJ[1:0] — Port J I/O signals

PJ[1:0] are general-purpose input or output signals. These signals can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull-up devices are enabled.

1.7.7 PL[1:0] / KWL[1:0] — Port L input signals

PL[1:0] are the high voltage input signal. These signals can be configured on a per signal basis as interrupt inputs with wake-up capability (KWL[1:0]). These signals can alternatively be used as analog inputs measured by the ADC.

1.7.8 PP[7:0] / KWP[7:0] — Port P I/O signals

PP[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWP[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.9 PS[7:0] / KWS[7:0] — Port S I/O signals

PS[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWS[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull up devices are enabled.

1.7.10 PT[7:0] — Port T I/O signals

PT[7:0] are general-purpose input or output signals. These signals can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.11 AN[15:0] — ADC input signals

AN[15:0] are the analog inputs of the Analog-to-Digital Converters.

1.7.12 ACMP Signals

1.7.12.1 ACMP0_0 / ACMP0_1— Analog Comparator 0 Inputs

ACMP0_0 and ACMP0_1 are the inputs of the analog comparator 0 ACMP0.

1.7.12.2 ACMP1_0 / ACMP1_1 — Analog Comparator 1 Inputs

ACMP1_0 and ACMP1_1 are the inputs of the analog comparator 1 ACMP1.

1.7.16.2 SCK[1:0] signals

This signal is associated with the serial clock SCK functionality of the serial peripheral interface SPI0 and SPI1.

1.7.16.3 MISO[1:0] signals

This signal is associated with the MISO functionality of the serial peripheral interface SPI0 and SPI1. This signal acts as master input during master mode or as slave output during slave mode.

1.7.16.4 MOSI[1:0] signals

This signal is associated with the MOSI functionality of the serial peripheral interface SPI0 and SPI1. This signal acts as master output during master mode or as slave input during slave mode

1.7.17 SCI signals

1.7.17.1 RXD[1:0] signals

These signals are associated with the receive functionality of the serial communication interfaces SCI[1:0].

1.7.17.2 TXD[1:0] signals

These signals are associated with the transmit functionality of the serial communication interfaces SCI[1:0].

1.7.18 Timer IOC[7:0] signals

The signals IOC0[7:0] and IOC1[3:0] are associated with the input capture or output compare functionality of the timer modules TIM0 and TIM1.

1.7.19 PWM[7:0] signals

The signals PWM0[7:0] and PWM1[7:0] are associated with the outputs of the PWM0 and PWM1 modules.

1.7.20 IIC signals

1.7.20.1 SDA signal

This signal is associated with the serial data pin of IIC.

1.7.20.2 SCL signal

This signal is associated with the serial clock pin of IIC.

The MC9S12ZVC-Family supports BDC communication throughout the device Stop mode. During Stop mode, writes to control registers can alter the operation and lead to unexpected results. It is thus recommended not to reconfigure the peripherals during STOP using the debugger.

1.10.3 Low Power Modes

The device has two dynamic-power modes (run and wait) and two static low-power modes (stop and pseudo stop). For a detailed description refer to the CPMU section.

- Dynamic power mode: Run
  - Run mode is the main full performance operating mode with the entire device clocked. The user can configure the device operating speed through selection of the clock source and the phase locked loop (PLL) frequency. To save power, unused peripherals must not be enabled.
- Dynamic power mode: Wait
  - This mode is entered when the CPU executes the WAI instruction. In this mode the CPU does not execute instructions. The internal CPU clock is switched off. All peripherals can be active in system wait mode. For further power consumption the peripherals can individually turn off their local clocks. Asserting $\overline{\text{RESET}}$, $\overline{\text{XIRQ}}$, $\overline{\text{IRQ}}$, or any other interrupt that is not masked, either locally or globally by a CCR bit, ends system wait mode.
- Static power modes:
  Static power (Stop) modes are entered following the CPU STOP instruction unless an NVM command is active. When no NVM commands are active, the Stop request is acknowledged and the device enters either Stop or Pseudo Stop mode.
  - Pseudo-stop: In this mode the system clocks are stopped but the oscillator is still running and the real time interrupt (RTI), watchdog (COP) and Autonomous Periodic Interrupt (API) may be enabled. Other peripherals are turned off. This mode consumes more current than system STOP mode but, as the oscillator continues to run, the full speed wake up time from this mode is significantly shorter.
  - Stop: In this mode the oscillator is stopped and clocks are switched off and the VREG enters reduced performance mode (RPM). The counters and dividers remain frozen. The autonomous periodic interrupt (API) may remain active but has a very low power consumption. The KWx pins and the SCI module can be configured to wake the device, whereby current consumption is negligible.
    If the BDC is enabled, in Stop mode, the VREG remains in full performance mode. With BDC enabled and BDCCIS bit set, then all clocks remain active during Stop mode to allow BDC access to internal peripherals. If the BDC is enabled and BDCCIS is clear, then the BDCSI clock remains active to allow BDC register access, but other clocks (with the exception of the API) are switched off. With the BDC enabled during Stop, the VREG full performance mode and clock activity lead to higher current consumption than with BDC disabled.
    If the BDC is enabled in Stop mode, then the voltage monitoring remains enabled.

NOTE

The U-bit should be cleared and the S-bit (stop enable) should be cleared in the CPU condition code register (CCR) to execute the STOP instruction.Otherwise the STOP instruction is considered as a NOP.

Read: Anytime.

Write: Never

DBGEFR contains flag bits each mapped to events whilst armed. Should an event occur, then the corresponding flag is set. With the exception of TRIGF, the bits can only be set when the ARM bit is set. The TRIGF bit is set if a TRIG event occurs when ARM is already set, or if the TRIG event occurs simultaneous to setting the ARM bit.All other flags can only be cleared by arming the DBG module. Thus the contents are retained after a debug session for evaluation purposes.

A set flag does not inhibit the setting of other flags.

Table 6-13. DBGEFR Field Descriptions

Field	Description
6 TRIGF	**TRIG Flag** — Indicates the occurrence of a TRIG event during the debug session. 0 No TRIG event 1 TRIG event
4 EEVF	**External Event Flag** — Indicates the occurrence of an external event during the debug session. 0 No external event 1 External event
3–0 ME[3:0]	**Match Event[3:0]**— Indicates a comparator match event on the corresponding comparator channel**.**

6.3.2.7 Debug Status Register (DBGSR)

Address: 0x010B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-10. Debug Status Register (DBGSR)

Read: Anytime.

Write: Never.

Table 6-14. DBGSR Field Descriptions

Field	Description
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate the current State Sequencer state. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal event, then the state sequencer returns to State0 and these bits are cleared to indicate that State0 was entered during the session. On arming the module the state sequencer enters State1 and these bits are forced to SSF[2:0] = 001. See Table 6-15**.**

8.3.2.16 Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

The CPMUAPICTL register allows the configuration of the autonomous periodical interrupt features.

Module Base + 0x0012

	7	6	5	4	3	2	1	0
R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-20. Autonomous Periodical Interrupt Control Register (CPMUAPICTL)

Read: Anytime

Write: Anytime

Table 8-18. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous Clock (ACLK) used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure 8-21. See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 8-22). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	**Autonomous Periodical Interrupt Enable Bit** 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1.Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

Table 8-22. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms[1]
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * Bus Clock period
1	0001	4 * Bus Clock period
1	0002	6 * Bus Clock period
1	0003	8 * Bus Clock period
1	0004	10 * Bus Clock period
1	0005	12 * Bus Clock period
1	.....	.....
1	FFFD	131068 * Bus Clock period
1	FFFE	131070 * Bus Clock period
1	FFFF	131072 * Bus Clock period

[1] When f_{ACLK} is trimmed to 20KHz.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Reset	0	0	0	0	0	0	0	0

Figure 11-11. Timer Count Register Low (TCNTL)

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes .

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

11.3.2.6 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-12. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

Table 11-6. TSCR1 Field Descriptions

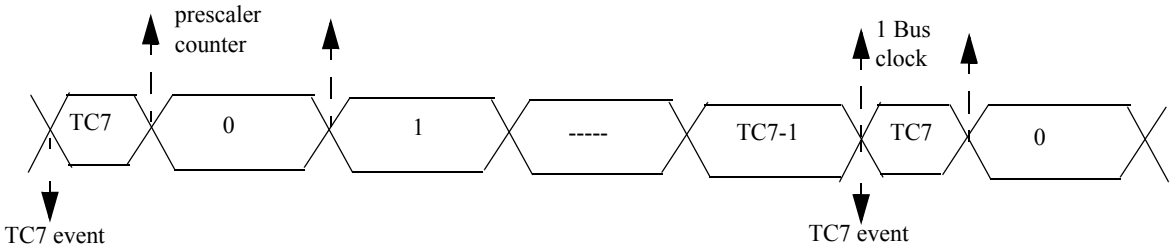
Field	Description
7 TEN	**Timer Enable** 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator because the ÷64 is generated by the timer prescaler.
6 TSWAI	**Timer Module Stops While in Wait** 0 Allows the timer module to continue running during wait. 1 Disables the timer module when the MCU is in the wait mode. Timer interrupts cannot be used to get the MCU out of wait. TSWAI also affects pulse accumulator.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

When TCRE is set and TC7 is not equal to 0, then TCNT will cycle from 0 to TC7. When TCNT reaches TC7 value, it will last only one Bus cycle then reset to 0.

Note: in Figure 11-31,if PR[2:0] is equal to 0, one prescaler counter equal to one Bus clock

Figure 11-31. The TCNT cycle diagram under TCRE=1 condition



11.4.3.1 OC Channel Initialization

The internal register whose output drives OCx can be programmed before the timer drives OCx. The desired state can be programmed to this internal register by writing a one to CFORCx bit with TIOSx, OCPDx and TEN bits set to one.

Set OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=1 and OCPDx=1

Clear OCx: Write a 1 to FOCx while TEN=1, IOSx=1, OMx=1, OLx=0 and OCPDx=1

Setting OCPDx to zero allows the internal register to drive the programmed state to OCx. This allows a glitch free switch over of port from general purpose I/O to timer output once the OCPDx bit is set to zero.

11.4.4 Pulse Accumulator

The pulse accumulator (PACNT) is a 16-bit counter that can operate in two modes:

Event counter mode — Counting edges of selected polarity on the pulse accumulator input pin, PAI.

Gated time accumulation mode — Counting pulses from a divide-by-64 clock. The PAMOD bit selects the mode of operation.

The minimum pulse width for the PAI input is greater than two Bus clocks.

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register.The transmit driver routine may respond to this flag by writing another byte to the Transmitter buffer (SCIDRH/SCIDRL), while the shift register is still shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
   a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is zero. Writing to the SCIBDH has no effect without also writing to SCIBDL.
   b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS,RSRC,M,WAKE,ILT,PE,PT).
   c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE,TCIE,RIE,ILIE,TE,RE,RWU,SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit Procedure for each byte:
   a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to one.
   b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

Chapter 16
Inter-Integrated Circuit (IICV3) Block Description

Table 16-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	28 Jul 2006	16.7.1.7/16-525	- Update flow-chart of interrupt routine for 10-bit address
V01.04	17 Nov 2006	16.3.1.2/16-505	- Revise Table1-5
V01.05	14 Aug 2007	16.3.1.1/16-505	- Backward compatible for IBAD bit name

16.1 Introduction

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

16.1.1 Features

The IIC module has the following key features:

- Compatible with I2C bus standard
- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation

17.5 Functional Description

17.5.1 General

The CAN Physical Layer provides an interface for the SoC-integrated MSCAN controller.

17.5.2 Modes

Figure 17-10 shows the possible mode transitions depending on control bit CPE, device reduced performance mode (“RPM”; refer to “Low Power Modes” section in device overview) and bus error conditions.

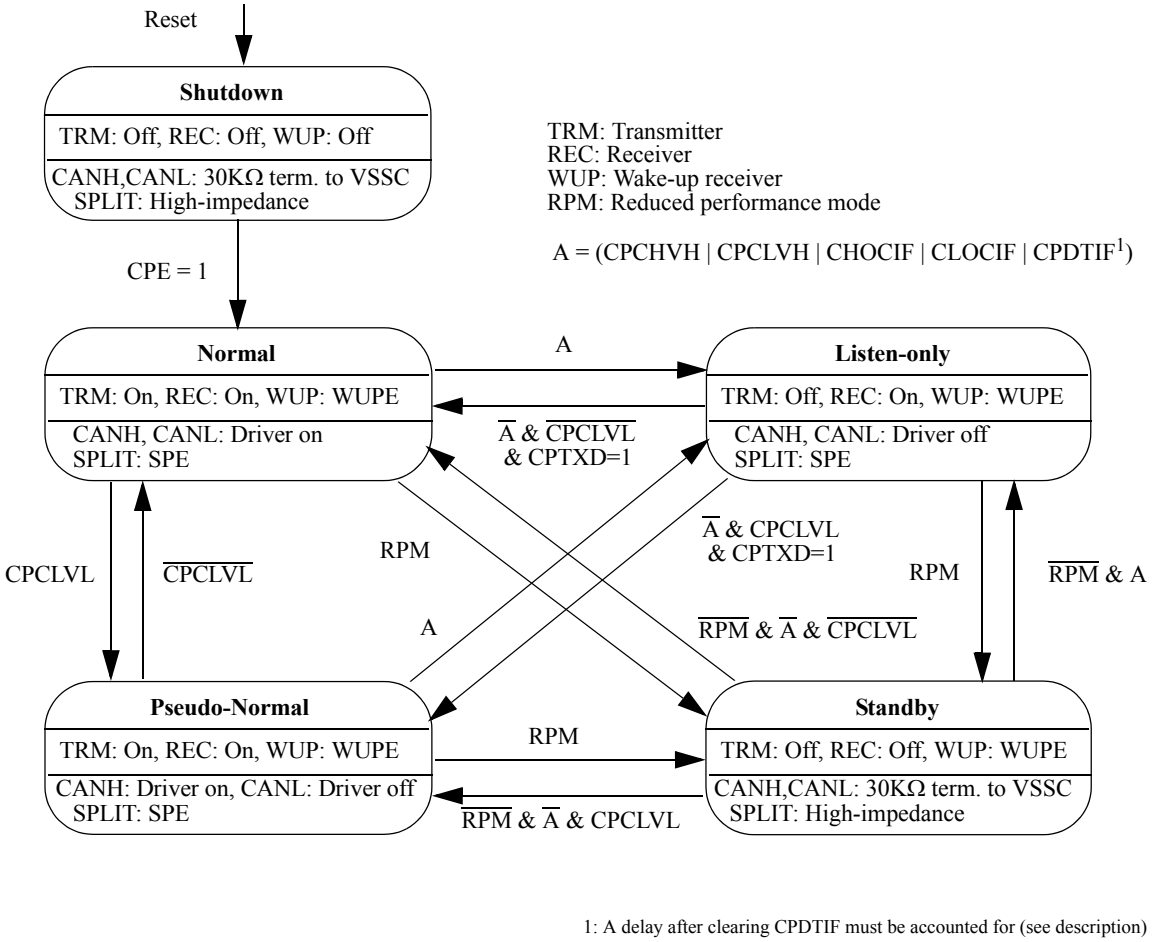


Figure 17-10. CAN Physical Layer Mode Transitions

17.5.2.1 Shutdown Mode

Shutdown mode is a low power mode and entered out of reset. The transceiver, wake-up, bus error diagnostic, dominant timeout and interrupt functionality are disabled. CANH and CANL lines are pulled

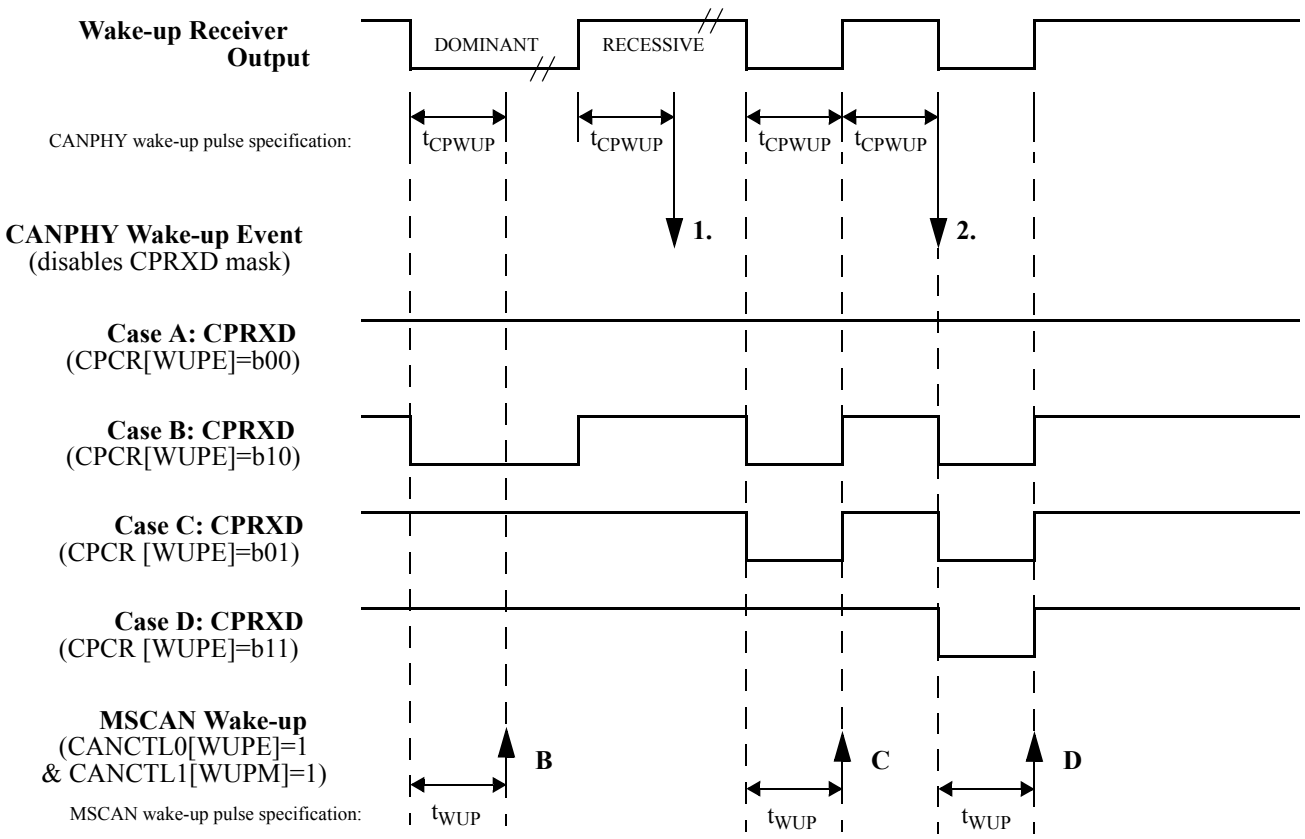


Figure 17-11. Wake-up Event Filtering

17.5.4 Interrupts

This section describes the interrupt generated by the CAN Physical Layer and its individual sources.

Vector addresses and interrupt priorities are defined at MCU level. The module internal interrupt sources are combined (OR-ed) into one module interrupt output CPI with a single local enable bit each for voltage failure and over-current errors.

Table 17-9. CAN Physical Layer Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
CAN Physical Layer Interrupt (CPI)	CANH Voltage Failure High Interrupt (CHVHIF)	CPVFIE = 1
	CANH Voltage Failure Low Interrupt (CHVLIF)	
	CANL Voltage Failure High Interrupt (CLVHIF)	
	CANL Voltage Failure Low Interrupt (CLVLIF)	
	CPTXD-Dominant Timeout Interrupt (CPDTIF)	CPDTIE = 1
	CANH Over-Current Interrupt (CHOCIF)	CPOCIE = 1
	CANL Over-Current Interrupt (CLOCIF)	

Table 18-17. CANIDAC Register Field Descriptions

Field	Description
5-4 IDAM[1:0]	**Identifier Acceptance Mode** — The CPU sets these flags to define the identifier acceptance filter organization (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-18 summarizes the different settings. In filter closed mode, no message is accepted such that the foreground buffer is never reloaded.
2-0 IDHIT[2:0]	Identifier Acceptance Hit Indicator — The MSCAN sets these flags to indicate an identifier acceptance hit (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-19 summarizes the different settings.

Table 18-18. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32-bit acceptance filters
0	1	Four 16-bit acceptance filters
1	0	Eight 8-bit acceptance filters
1	1	Filter closed

Table 18-19. Identifier Acceptance Hit Indication

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit
0	0	0	Filter 0 hit
0	0	1	Filter 1 hit
0	1	0	Filter 2 hit
0	1	1	Filter 3 hit
1	0	0	Filter 4 hit
1	0	1	Filter 5 hit
1	1	0	Filter 6 hit
1	1	1	Filter 7 hit

The IDHITx indicators are always related to the message in the foreground buffer (RxFG). When a message gets shifted into the foreground buffer of the receiver FIFO the indicators are updated as well.

18.3.2.13 MSCAN Reserved Register

This register is reserved for factory testing of the MSCAN module and is not available in normal system operating modes.

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

18.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 18.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

19.4.2.2 Analog Output Voltage Level Register (DACVOL)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	VOLTAGE[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 19-4. Analog Output Voltage Level Register (DACVOL)

1 Read: Anytime
Write: Anytime

Table 19-4. DACVOL Field Description

Field	Description
7:0 VOLTAGE[7:0]	**VOLTAGE** — This register defines (together with the FVR bit) the analog output voltage. For more detail see Equation 19-1 and Equation 19-2.

19.4.2.3 Reserved Register

Module Base + 0x0007 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
W								
Reset	0	0	0	0	0	0	0	0

Figure 19-5. Reserved Registerfv_dac_8b5v_RESERVED

1 Read: Anytime
Write: Only in special mode

NOTE

This reserved register bits are designed for factory test purposes only and are not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

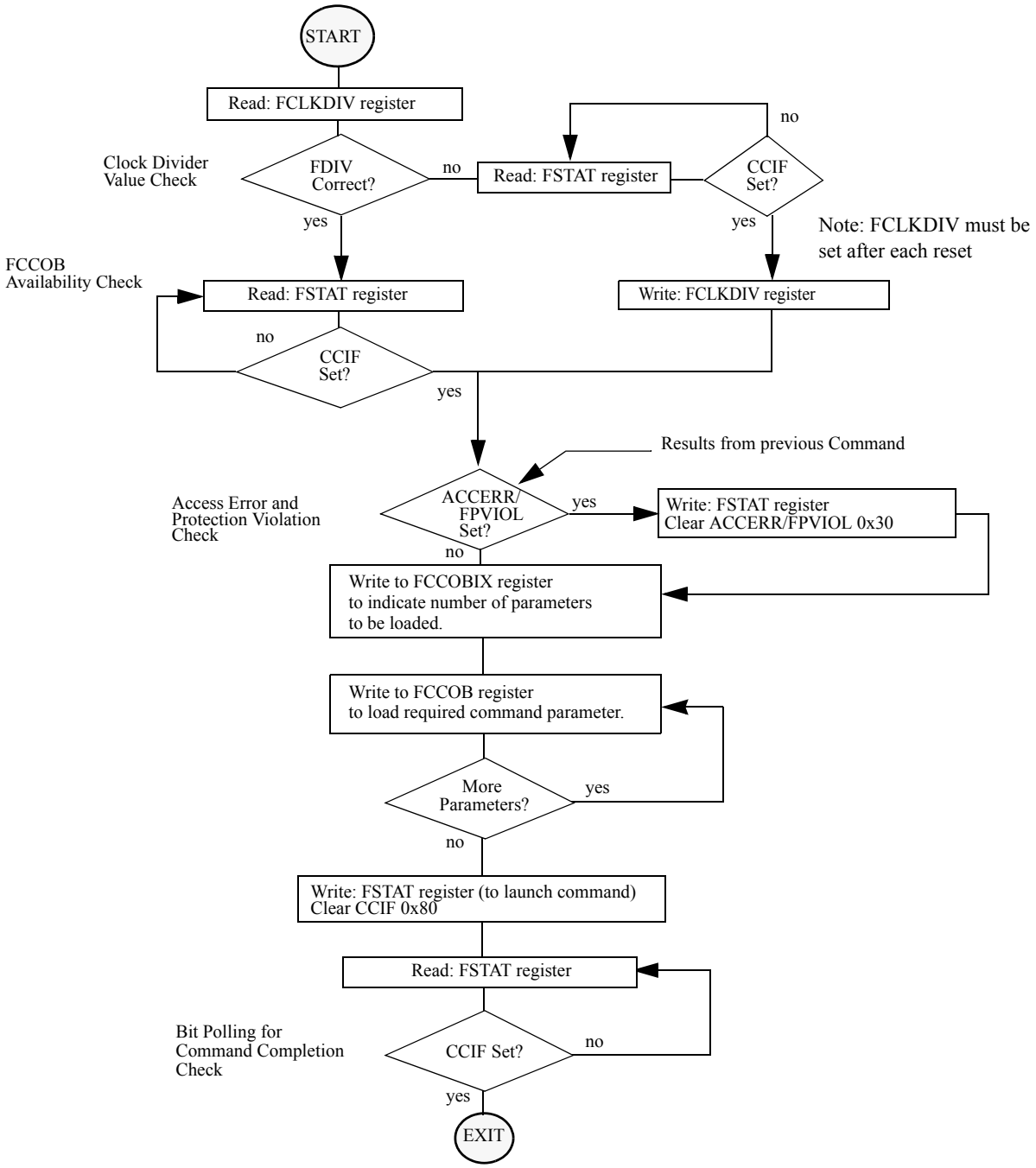


Figure 22-30. Generic Flash Command Write Sequence Flowchart

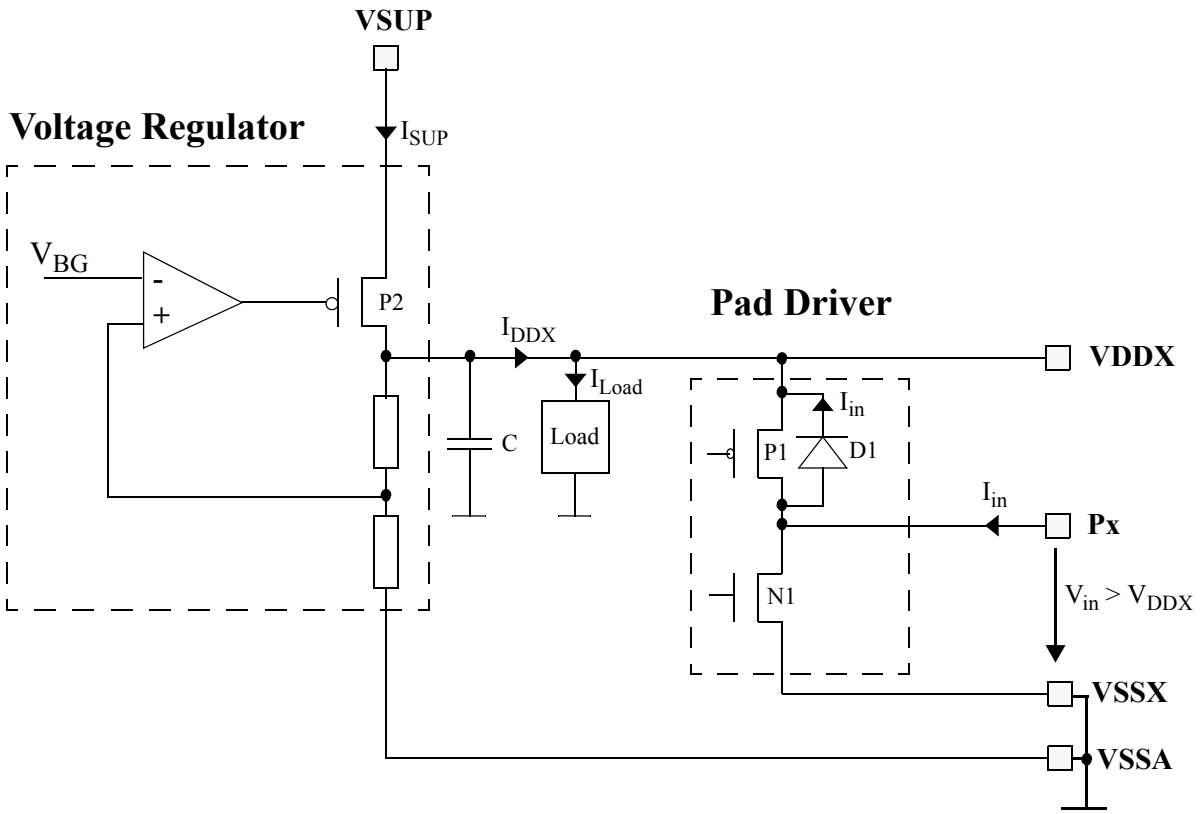
A.1.2.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

A.1.3 Current Injection

Power supply must maintain regulation within operating V_{DDX} or V_{DD} range during instantaneous and operating maximum current conditions. **Figure A-1.** shows a 5 V GPIO pad driver and the on chip voltage regulator with VDDX output. It shows also the power and ground pins VSUP, VDDX, VSSX and VSSA. Px represents any 5 V GPIO pin. Assume Px is configured as an input. The pad driver transistors P1 and N1 are switched off (high impedance). If the voltage V_{in} on Px is greater than V_{DDX} a positive injection current I_{in} will flow through diode D1 into VDDX node. If this injection current I_{in} is greater than I_{Load}, the internal power supply VDDX may go out of regulation. Ensure the external V_{DDX} load will shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Figure A-1. Current Injection on GPIO Port if $V_{in} > V_{DDX}$



A.1.4 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation outside these ranges is not guaranteed. Stress beyond these limits may affect the reliability or cause permanent damage of the device.

Appendix K
NVM Electrical Parameters

K.1 NVM Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

The device bus frequency, below which the flash wait states can be disabled, is specified in the device operating condition table in Table A-5.

The following sections provide equations which can be used to determine the time required to execute specific flash commands. All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in Table K.

K.2 NVM Reliability Parameters

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The data retention and program/erase cycling failure rates are specified at the operating conditions noted. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table K-1. NVM Clock Timing Characteristics

Num	Rating	Symbol	Min	Typ	Max	Unit
1	Bus frequency	f_{NVMBUS}	1	32	32	MHz
2	Operating frequency	f_{NVMOP}	0.8	1.0	1.05	MHz

Table K-2. NVM Timing Characteristics 32 MHz (Junction Temperature From –40°C To +175°C)

Num	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Erase Verify All Blocks[5,6]	0	51101	t_{RD1ALL}	1.60	1.60	3.19	102.20	ms
2	Erase Verify Block (Pflash)[5]	0	49894	t_{RD1BLK_P}	1.56	1.56	3.12	99.79	ms
3	Erase Verify Block (EEPROM)[6]	0	1608	t_{RD1BLK_D}	0.05	0.05	0.10	3.22	ms
4	Erase Verify P-Flash Section	0	624	t_{RD1SEC}	0.02	0.02	0.04	1.25	ms
5	Read Once	0	512	t_{RDONCE}	16.00	16.00	16.00	512.00	us

N.17 0x06F0-0x06F7 BATS

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06F0	BATE	R	0	BVHS	BVLS[1:0]		BSUAE	BSUSE	0	0
		W								
0x06F1	BATSR	R	0	0	0	0	0	0	BVHC	BVLC
		W								
0x06F2	BATIE	R	0	0	0	0	0	0	BVHIE	BVLIE
		W								
0x06F3	BATIF	R	0	0	0	0	0	0	BVHIF	BVLIF
		W								
0x06F4 - 0x06F5	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x06F6 - 0x06F7	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								

N.18 0x0700-0x0707 SCI0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0700	SCI0BDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0701	SCI0BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x0702	SCI0CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0700	SCI0ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0701	SCI0ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x0702	SCI0ACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x0703	SCI0CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x0704	SCI0SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x0705	SCI0SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								