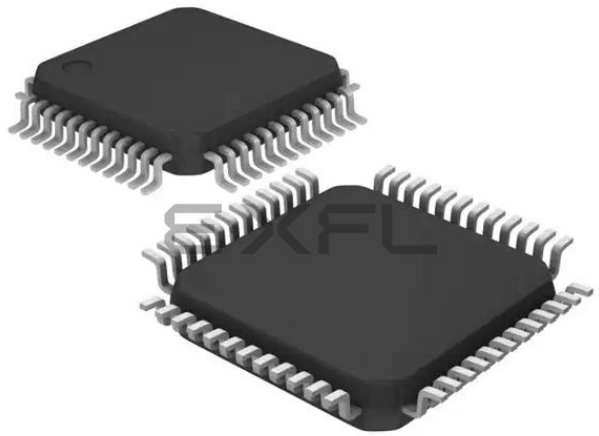

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Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc12f0mlfr

1.7.5 PE[1:0] — Port E I/O signals

PE[1:0] are general-purpose input or output signals. They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull down devices are enabled.

1.7.6 PJ[1:0] — Port J I/O signals

PJ[1:0] are general-purpose input or output signals. These signals can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull-up devices are enabled.

1.7.7 PL[1:0] / KWL[1:0] — Port L input signals

PL[1:0] are the high voltage input signal. These signals can be configured on a per signal basis as interrupt inputs with wake-up capability (KWL[1:0]). These signals can alternatively be used as analog inputs measured by the ADC.

1.7.8 PP[7:0] / KWP[7:0] — Port P I/O signals

PP[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWP[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.9 PS[7:0] / KWS[7:0] — Port S I/O signals

PS[7:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWS[7:0]). They can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull up devices are enabled.

1.7.10 PT[7:0] — Port T I/O signals

PT[7:0] are general-purpose input or output signals. These signals can have a pull-up or pull-down device selected and enabled on per signal basis. Out of reset the pull devices are disabled.

1.7.11 AN[15:0] — ADC input signals

AN[15:0] are the analog inputs of the Analog-to-Digital Converters.

1.7.12 ACMP Signals

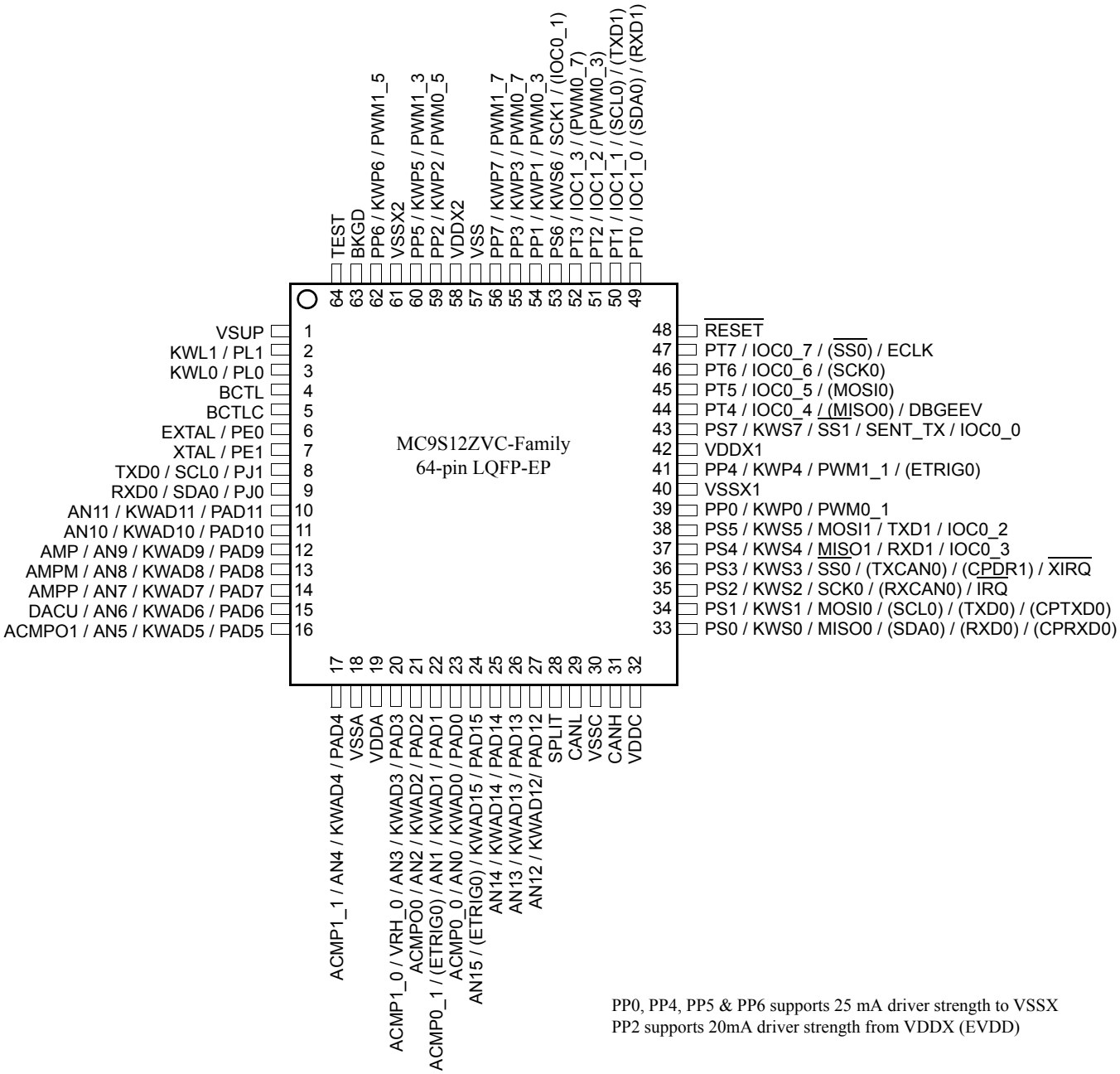
1.7.12.1 ACMP0_0 / ACMP0_1— Analog Comparator 0 Inputs

ACMP0_0 and ACMP0_1 are the inputs of the analog comparator 0 ACMP0.

1.7.12.2 ACMP1_0 / ACMP1_1 — Analog Comparator 1 Inputs

ACMP1_0 and ACMP1_1 are the inputs of the analog comparator 1 ACMP1.

Figure 1-4. Pinout MC9S12ZVC-Family 64-pin LQFP-EP[1]



1.The exposed pad on the package bottom must be connected to a ground pad on the PCB.

Table 1-6. MC9S12ZVC-Family Pin Summary

LQFP			Function					Power Supply	Internal Pull Resistor	
64	48	Pin	1st Func.	2nd Func.	3rd Func.	4th Func.	5th Func.		CTRL	Reset State
44	34	PT4	IOC0_4	(MISO0)	DBGEEV		—	V_{DDX}	PERT/ PPST	Off
45	—	PT5	IOC0_5	(MOSI0)		—	—	V_{DDX}	PERT/ PPST	Off
46	—	PT6	IOC0_6	(SCK0)	—	—	—	V_{DDX}	PERT/ PPST	Off
47	35	PT7	IOC0_7	($\overline{SS0}$)	ECLK	—	—	V_{DDX}	PERT/ PPST	Off
48	36	$\overline{RESET}$	—	—	—	—	—	V_{DDX}	TEST pin	Up
49	37	PT0	IOC1_0	(SDA0)	(RXD1)			V_{DDX}	PERT/ PPST	Off
50	38	PT1	IOC1_1	(SCL0)	(TXD1)			V_{DDX}	PERT/ PPST	Off
51	39	PT2	IOC1_2	(PWM0_3)				V_{DDX}	PERT/ PPST	Off
52	40	PT3	IOC1_3	(PWM0_7)				V_{DDX}	PERT/ PPST	Off
53		PS6	KWS6	SCK1	(IOC0_1)			V_{DDX}	PERS/ PPSS	Up
54	—	PP1	KWP1	PWM0_3	—	—	—	V_{DDX}	PERP/ PPSP	Off
55	—	PP3	KWP3	PWM0_7	—	—	—	V_{DDX}	PERP/ PPSP	Off
56	—	PP7	KWP7	PWM1_7	—	—	—	V_{DDX}	PERP/ PPSP	Off
57	41	VSS	—	—	—	—	—			
58	42	VDDX2	—	—	—	—	—	V_{DDX}		
59	43	PP2	KWP2	PWM0_5	—	—	—	V_{DDX}	PERP/ PPSP	Off
60	44	PP5	KWP5	PWM1_3	—	—	—	V_{DDX}	PERP/ PPSP	Off
61	45	VSSX2	—	—	—	—	—	V_{DDX}		
62	46	PP6	KWP6	PWM1_5	—	—	—	V_{DDX}	PERP/ PPSP	Off
63	47	BKGD	MODC	—	—	—	—	V_{DDX}		Up
64	48	TEST	—	—	—	—	—	—	$\overline{RESET}$	Down

[1]Input capture routed to PS7 by default. Output compare feature always on PS6.
[2]Input capture routed to PS7 by default. Output compare feature always on PS6

2.3.3.2 Port Input Register

Address 0x0262 PTIE
0x0282 PTIADH
0x0283 PTIADL
0x02C1 PTIT
0x02D1 PTIS
0x02F1 PTIP
0x0311 PTIJ
0x0331 PTIL

Access: User read only[1]

	7	6	5	4	3	2	1	0
R	PTIx7	PTIx6	PTIx5	PTIx4	PTIx3	PTIx2	PTIx1	PTIx0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-11. Port Input Register

[1] Read: Anytime
Write:Never

This is a generic description of the standard port input registers. Refer to Table 2-33 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-12. Port Input Register Field Descriptions

Field	Description
7-0 PTIx7-0	**Port Input** — Data input A read always returns the buffered input state of the associated pin. It can be used to detect overload or short circuit conditions on output pins.

2.3.3.3 Data Direction Register

Address 0x0264 DDRE
0x0284 DDRADH
0x0285 DDRADL
0x02C2 DDRT
0x02D2 DDRS
0x02F2 DDRP
0x0312 DDRJ

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	DDRx7	DDRx6	DDRx5	DDRx4	DDRx3	DDRx2	DDRx1	DDRx0
Reset	0	0	0	0	0	0	0	0

Figure 2-12. Data Direction Register

[1] Read: Anytime
Write: Anytime

This is a generic description of the standard data direction registers. Refer to Table 2-33 to determine the implemented bits in the respective register. Unimplemented bits read zero.

2.3.4.12 Port L Test Enable Register (PTTEL)

Address 0x033F Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTTEL1	PTTEL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-32. Port L Test Enable Register (PTTEL)

[1] Read: Anytime
Write: Anytime

Table 2-32. PTTEL Register Field Descriptions

Field	Description
1-0 PTTEL1-0	**Port L Test Enable** — This bit forces the input buffer of the HVI pin active while using the analog function to support open input detection in run mode. Refer to Section 2.5.5, "Open Input Detection on PL[1:0] (HVI)"). In stop mode this bit has no effect. **Note:** In direct mode (PTADIRL=1) the digital input buffer is not enabled. 1 Input buffer enabled when used with analog function and not in direct mode (PTADIRL=0) 0 Input buffer disabled when used with analog function

2.4 Functional Description

2.4.1 General

Each pin except BKGD can act as general-purpose I/O. In addition each pin can act as an output or input of a peripheral module.

2.4.2 Registers

Table 2-33 lists the implemented configuration bits which are available on each port. These registers except the pin input registers can be written at any time, however a specific configuration might not become active. For example a pullup device does not become active while the port is used as a push-pull output.

Unimplemented bits read zero.

drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

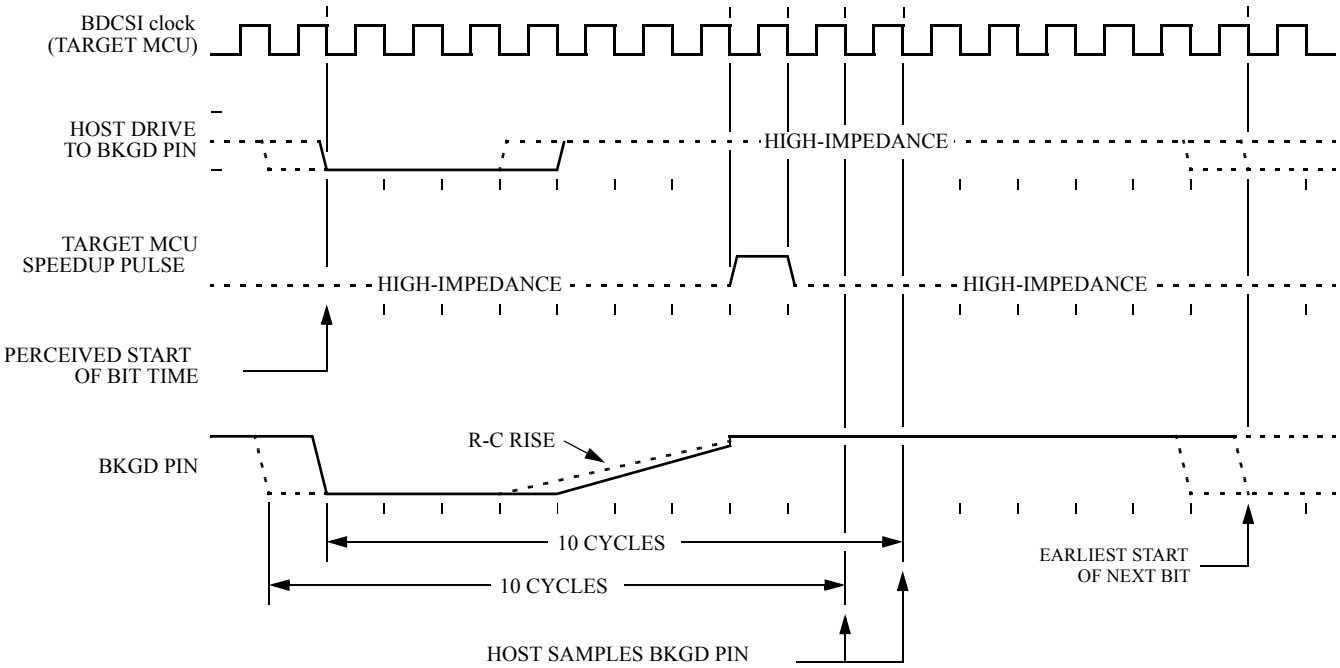


Figure 3-7. BDC Target-to-Host Serial Bit Timing (Logic 1)

Figure 3-8 shows the host receiving a logic 0 from the target. The host initiates the bit time but the target finishes it. Since the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

6.3.2.14 Debug Comparator D Control Register (DBGDCTL)

Address: 0x0140

	7	6	5	4	3	2	1	0
R	0	0	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-17. Debug Comparator D Control Register

Read: Anytime.

Write: If DBG not armed.

Table 6-24. DBGDCTL Field Descriptions

Field[1]	Description
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

1 If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 6-25 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 6-25. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

Table 6-31. Event Priorities

Priority	Source	Action
Highest	TRIG	Force immediately to final state
	DBGEEV	Force to next state as defined by state control registers (EEVE=2'b10)
	Match3	Force to next state as defined by state control registers
	Match1	Force to next state as defined by state control registers
Lowest	Match0	Force to next state as defined by state control registers

6.4.4 State Sequence Control

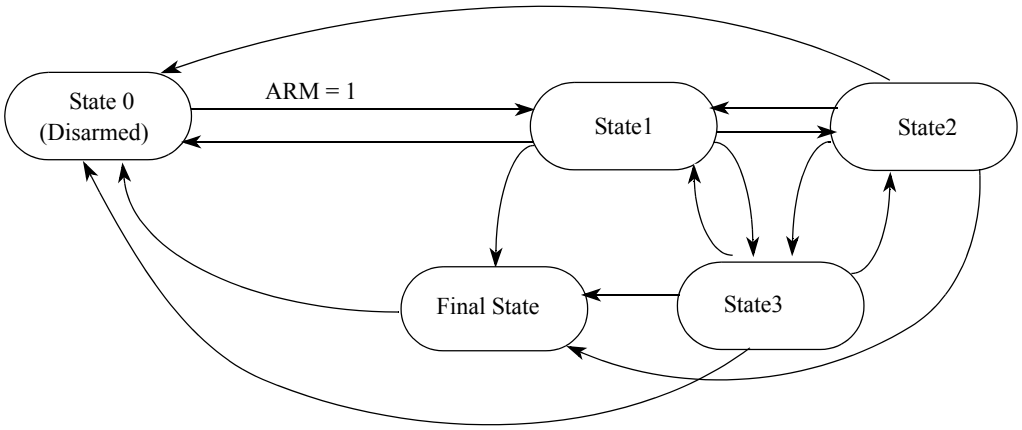


Figure 6-19. State Sequencer Diagram

The state sequencer allows a defined sequence of events to provide a breakpoint. When the DBG module is armed by setting the ARM bit in the DBGC1 register, the state sequencer enters State1. Further transitions between the states are controlled by the state control registers and depend upon event occurrences (see Section 6.4.3, "Events). From Final State the only permitted transition is back to the disarmed State0. Transition between the states 1 to 3 is not restricted. Each transition updates the SSF[2:0] flags in DBGSR accordingly to indicate the current state. If breakpoints are enabled, then an event based transition to State0 generates the breakpoint request. A transition to State0 resulting from writing "0" to the ARM bit does not generate a breakpoint request.

6.4.4.1 Final State

When the Final State is reached the state sequencer returns to State0 immediately and the debug module is disarmed.If breakpoints are enabled, a breakpoint request is generated on transitions to State0.

6.4.5 Breakpoints

Breakpoints can be generated by state sequencer transitions to State0. Transitions to State0 are forced by the following events

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ADCEOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0011	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	Reserved	Reserved					0	0
		W								
0x0014	ADCCMD_0	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0015	ADCCMD_1	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0016	ADCCMD_2	R	SMP[4:0]					0	0	Reserved
		W								
0x0017	ADCCMD_3	R	Reserved	Reserved	Reserved					
		W								
0x0018	Reserved	R	Reserved							
		W								
0x0019	Reserved	R	Reserved							
		W								
0x001A	Reserved	R	Reserved							
		W								
0x001B	Reserved	R	Reserved							
		W								
0x001C	ADCCIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x001D	ADCCBP_0	R	CMD_PTR[23:16]							
		W								
0x001E	ADCCBP_1	R	CMD_PTR[15:8]							
		W								
0x001F	ADCCBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0020	ADCRIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0021	ADCRBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0022	ADCRBP_1	R	RES_PTR[15:8]							
		W								
0x0023	ADCRBP_2	R	RES_PTR[7:2]						0	0
		W								
0x0024	ADCCROFF0	R	0	CMDRES_OFF0[6:0]						
		W								
0x0025	ADCCROFF1	R	0	CMDRES_OFF1[6:0]						
		W								
0x0026	Reserved	R	0	0	0	0	Reserved			
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 2 of 3)

9.8 Use Cases and Application Information

9.8.1 List Usage — CSL single buffer mode and RVL single buffer mode

In this use case both list types are configured for single buffer mode (CSL_BMOD=1’b0 and RVL_BMOD=1’b0, CSL_SEL and RVL_SEL are forced to 1’b0). The index register for the CSL and RVL are cleared to start from the top of the list with next conversion command and result storage in the following cases:

- The conversion flow reaches the command containing the “End-of-List” command type identifier
- A Restart Request occurs at a sequence boundary
- After an aborted conversion or conversion sequence

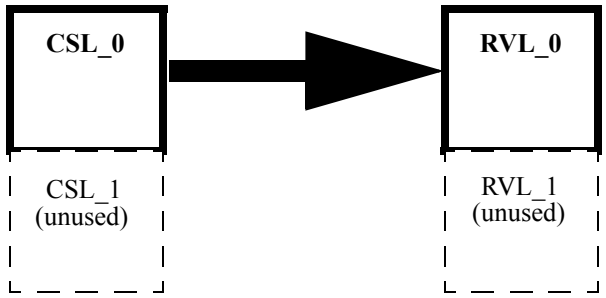


Figure 9-35. CSL Single Buffer Mode — RVL Single Buffer Mode Diagram

9.8.2 List Usage — CSL single buffer mode and RVL double buffer mode

In this use case the CSL is configured for single buffer mode (CSL_BMOD=1’b0) and the RVL is configured for double buffer mode (RVL_BMOD=1’b1). In this buffer configuration only the result list RVL is switched when the first conversion result of a CSL is stored after a CSL was successfully finished or a CSL got aborted.

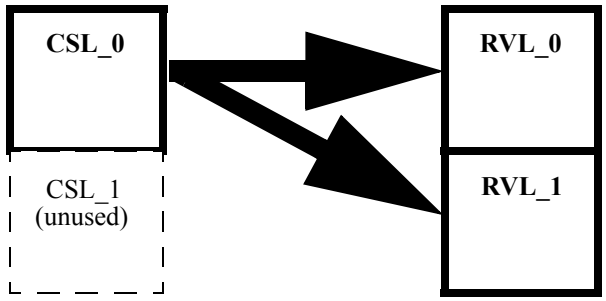


Figure 9-36. CSL Single Buffer Mode — RVL Single Buffer Mode Diagram

The last entirely filled RVL (an RVL where the corresponding CSL has been executed including the “End Of List “ command type) is shown by register ADCEOLRI.

The CSL is used in single buffer mode and bit CSL_SEL is forced to 1’b0.

NOTE

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

11.3.2.12 Main Timer Interrupt Flag 1 (TFLG1)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write: Used in the clearing mechanism (set bits cause corresponding bits to be cleared). Writing a zero will not affect current status of the bit.

Table 11-16. TRLG1 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 C[7:0]F	**Input Capture/Output Compare Channel "x" Flag** — These flags are set when an input capture or output compare event occurs. Clearing requires writing a one to the corresponding flag bit while TEN or PAEN is set to one. **Note:** When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel (0x0010–0x001F) will cause the corresponding channel flag CxF to be cleared.

11.3.2.13 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-21. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 or PAEN bit of PACTL is set to one.

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

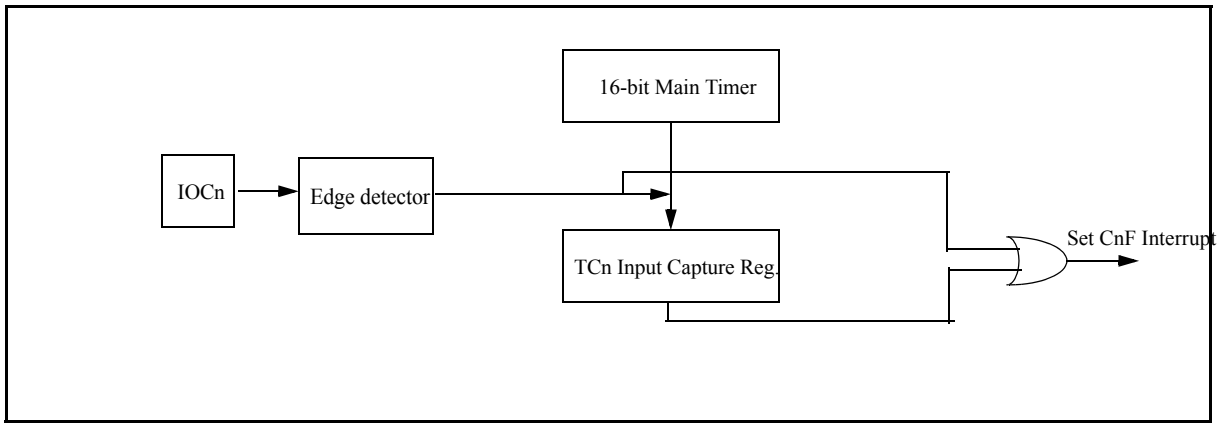


Figure 12-2. Interrupt Flag Setting

12.2 External Signal Description

The TIM16B4CV3 module has a selected number of external pins. Refer to device specification for exact number.

12.2.1 IOC3 - IOC0 — Input Capture and Output Compare Channel 3-0

Those pins serve as input capture or output compare for TIM16B4CV3 channel .

NOTE

For the description of interrupts see Section 12.6, “Interrupts”.

12.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

12.3.1 Module Memory Map

The memory map for the TIM16B4CV3 module is given below in Figure 12-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B4CV3 module and the address offset for each register.

12.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

13.2.1 PWM7 - PWM0 — PWM Channel 7 - 0

Those pins serve as waveform output of PWM channel 7 - 0.

13.3 Memory Map and Register Definition

13.3.1 Module Memory Map

This section describes the content of the registers in the scalable PWM module. The base address of the scalable PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated with the scalable PWM and their relative offset from the base address. The register detail description follows the order they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

13.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the scalable PWM module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PWME[1]	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
	W								
0x0001 PWMPOL[1]	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
	W								
0x0002 PWMCLK[1]	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
	W								
0x0003 PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
0x0004 PWMCAE[1]	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
	W								
0x0005 PWMCTL[1]	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
	W								

= Unimplemented or Reserved

Figure 13-2. The scalable PWM Register Summary (Sheet 1 of 4)

13.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8-bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Shown below in Figure 13-16 is the block diagram for the PWM timer.

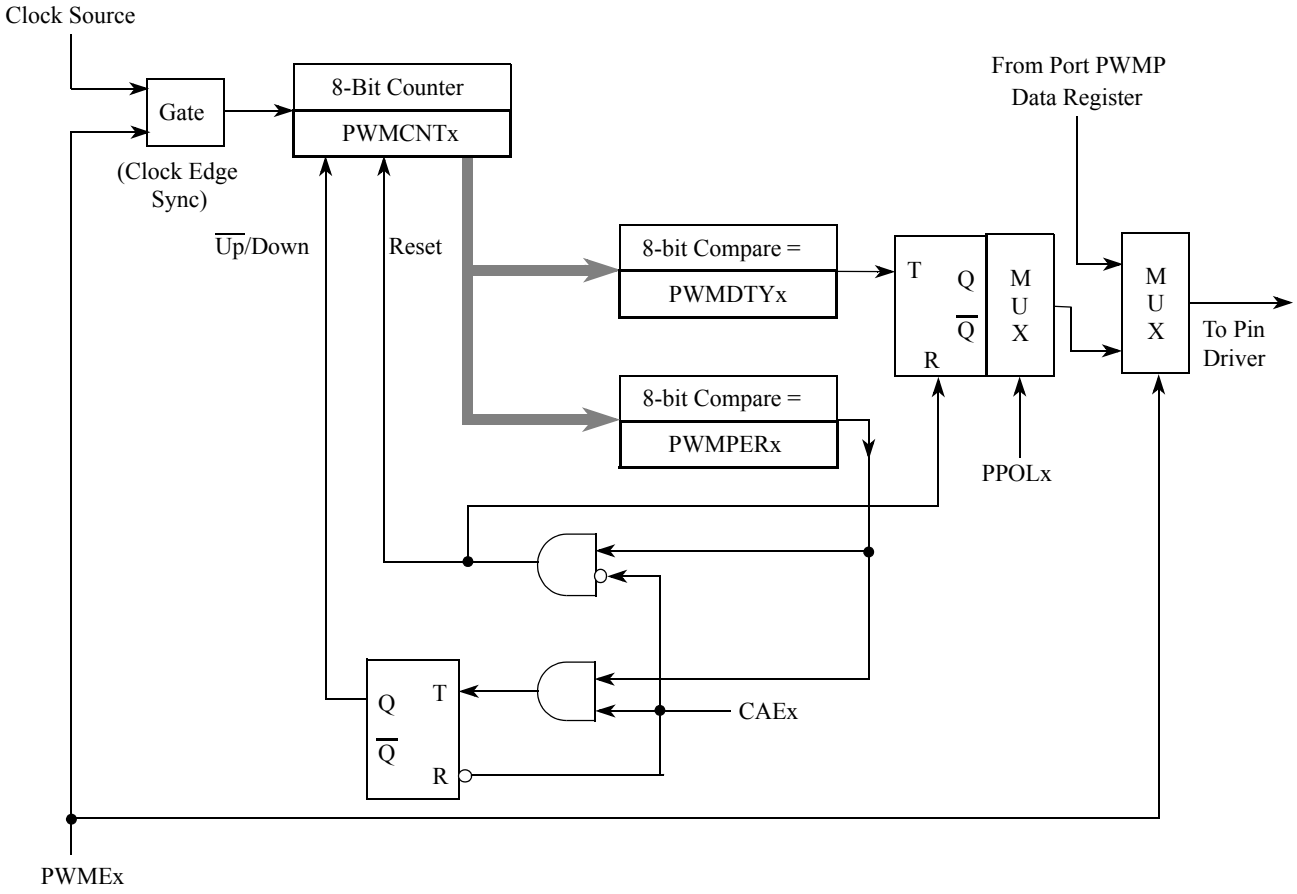


Figure 13-16. PWM Timer Channel Block Diagram

13.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 13.4.2.7, “PWM 16-Bit Functions” for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register.The transmit driver routine may respond to this flag by writing another byte to the Transmitter buffer (SCIDRH/SCIDRL), while the shift register is still shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
   a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is zero. Writing to the SCIBDH has no effect without also writing to SCIBDL.
   b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS,RSRC,M,WAKE,ILT,PE,PT).
   c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE,TCIE,RIE,ILIE,TE,RE,RWU,SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit Procedure for each byte:
   a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to one.
   b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

17.5 Functional Description

17.5.1 General

The CAN Physical Layer provides an interface for the SoC-integrated MSCAN controller.

17.5.2 Modes

Figure 17-10 shows the possible mode transitions depending on control bit CPE, device reduced performance mode (“RPM”; refer to “Low Power Modes” section in device overview) and bus error conditions.

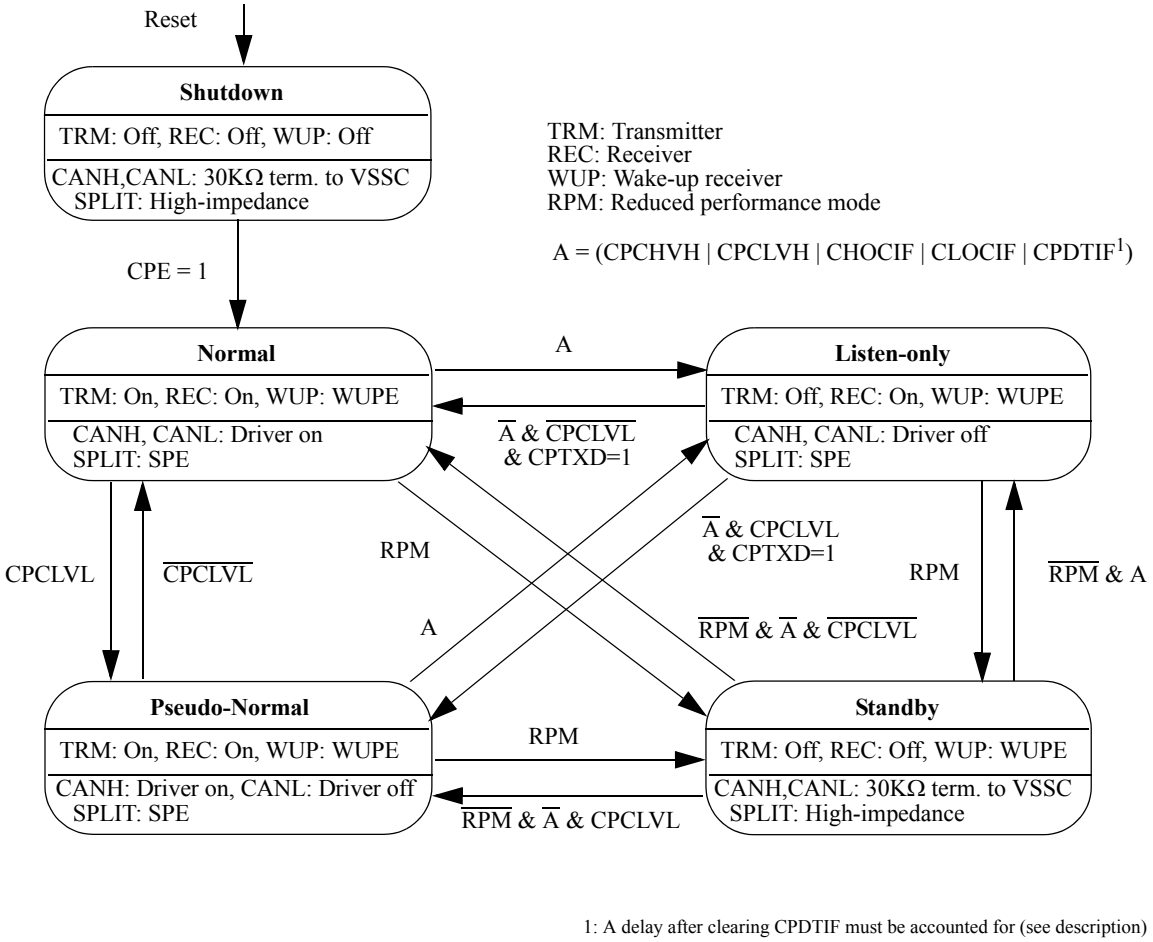


Figure 17-10. CAN Physical Layer Mode Transitions

17.5.2.1 Shutdown Mode

Shutdown mode is a low power mode and entered out of reset. The transceiver, wake-up, bus error diagnostic, dominant timeout and interrupt functionality are disabled. CANH and CANL lines are pulled

Table 18-17. CANIDAC Register Field Descriptions

Field	Description
5-4 IDAM[1:0]	**Identifier Acceptance Mode** — The CPU sets these flags to define the identifier acceptance filter organization (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-18 summarizes the different settings. In filter closed mode, no message is accepted such that the foreground buffer is never reloaded.
2-0 IDHIT[2:0]	Identifier Acceptance Hit Indicator — The MSCAN sets these flags to indicate an identifier acceptance hit (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-19 summarizes the different settings.

Table 18-18. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32-bit acceptance filters
0	1	Four 16-bit acceptance filters
1	0	Eight 8-bit acceptance filters
1	1	Filter closed

Table 18-19. Identifier Acceptance Hit Indication

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit
0	0	0	Filter 0 hit
0	0	1	Filter 1 hit
0	1	0	Filter 2 hit
0	1	1	Filter 3 hit
1	0	0	Filter 4 hit
1	0	1	Filter 5 hit
1	1	0	Filter 6 hit
1	1	1	Filter 7 hit

The IDHITx indicators are always related to the message in the foreground buffer (RxFG). When a message gets shifted into the foreground buffer of the receiver FIFO the indicators are updated as well.

18.3.2.13 MSCAN Reserved Register

This register is reserved for factory testing of the MSCAN module and is not available in normal system operating modes.

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0315–0x031E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x031F	WOMJ	R	0	0	0	0	0	0	WOMJ1	WOMJ0
		W								
0x0320–0x032F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0330	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0331	PTIL	R	0	0	0	0	0	0	PTIL1	PTIL0
		W								
0x0332	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0333	PTPSL	R	0	0	0	0	0	0	PTPSL1	PTPSL0
		W								
0x0334	PPSL	R	0	0	0	0	0	0	PPSL1	PPSL0
		W								
0x0335	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0336	PIEL	R	0	0	0	0	0	0	PIEL1	PIEL0
		W								
0x0337	PIFL	R	0	0	0	0	0	0	PIFL1	PIFL0
		W								
0x0338–0x0339	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x033A	PTABYPL	R	0	0	0	0	0	0	PTABYPL1	PTABYPL0
		W								
0x033B	PTADIRL	R	0	0	0	0	0	0	PTADIRL1	PTADIRL0
		W								
0x033C	DIENL	R	0	0	0	0	0	0	DIENL1	DIENL0
		W								
0x033D	PTAENL	R	0	0	0	0	0	0	PTAENL1	PTAENL0
		W								