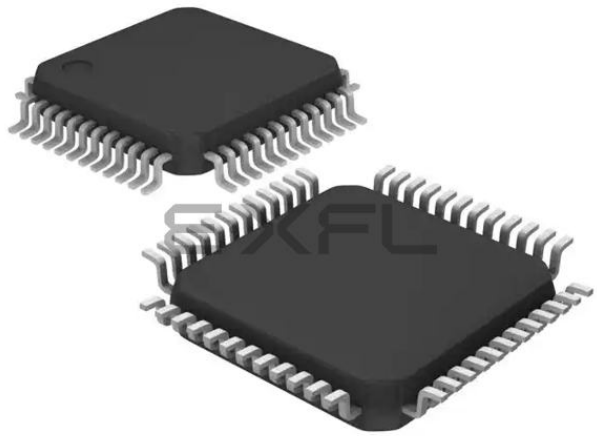

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc12f0vlf

Chapter 1
Device Overview MC9S12ZVC-Family

1.9.5 TIM0 and TIM1 IOC Channel Connectivity

Table 1-9 shows a summary of TIM0 and TIM1channel connections.

Table 1-9. TIM0 and TIM1 Connections

IOC Channel	TIM0	TIM1 (fast)
IOC0	SENTTX	PT0
IOC1	SENTTX	PT1
IOC2	ACLK / ADC Trigger	PT2 / ACMP0 output
IOC3	RXD0 / RXD1	PT3 / ACMP1 output
IOC4	PT4	
IOC5	PT5	
IOC6	PT6	
IOC7	PT7	

1.9.6 PWM0 and PWM1 Clock Source Connectivity

The clock for PWM1, PWM Clock , is mapped to device core clock, generated in the CPMU module. (maximum core clock is 64MHz)

The clock for PWM0 , PWM Clock , is mapped to device bus clock, generated in the CPMU module. (maximum bus clock is 32MHz)

1.9.7 BDC Clock Source Connectivity

The BDC clock, BDCCLK, is mapped to the IRCCLK generated in the CPMU module.

The BDC clock, BDCFCLK is mapped to the device bus clock, generated in the CPMU module.

1.9.8 FTMRZ Connectivity

The soc_erase_all_req input to the flash module is driven directly by a BDC erase flash request resulting from the BDC ERASE_FLASH command.

1.9.9 CPMU Connectivity

The API clock generated in the CPMU is not mapped to a device pin in the MC9S12ZVC-Family.

Table 2-19. Reduced Drive Register Field Descriptions

Field	Description
7-0 RDRx7-0	**Reduced Drive Register** — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/10 of the full drive strength) 0 Full drive strength enabled

2.3.3.10 Wired-Or Mode Register

Address 0x02DF WOMS
0x031F WOMJ

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	WOMx7	WOMx6	WOMx5	WOMx4	WOMx3	WOMx2	WOMx1	WOMx0
Reset	0	0	0	0	0	0	0	0

Figure 2-19. Wired-Or Mode Register

[1] Read: Anytime
Write: Anytime

This is a generic description of the standard wired-or registers. Refer to Table 2-33 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-20. Wired-Or Mode Register Field Descriptions

Field	Description
7-0 WOMx7-0	**Wired-Or Mode** — Enable open-drain output This bit configures the output buffer as wired-or. If enabled the output is driven active low only (open-drain) while the active high drive is turned off. This allows a multipoint connection of several serial modules. These bits have no influence on pins used as inputs. 1 Output buffers operate as open-drain outputs 0 Output buffers operate as push-pull outputs

2.3.3.11 PIM Reserved Register

Address (any reserved)

Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-20. PIM Reserved Register

[1] Read: Always reads 0x00
Write: Unimplemented

2.3.4.4 Port L Input Register (PTIL)

Address 0x0331 Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTIL1	PTIL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-24. Port L Input Register (PTIL)

[1] Read: Anytime
Write: No Write

Table 2-24. PTIL - Register Field Descriptions

Field	Description
1-0 PTIL1-0	**Port Input Data Register Port L —** A read returns the synchronized input state if the associated HVI pin is used in digital mode, that is the related DIENL bit is set to 1 and the pin is not used in analog mode (PTAENL=0). See Section 2.3.4.10, “Port L ADC Connection Enable Register (PTAENL)”. A one is read in any other case[1].

[1] Refer to PTTEL bit description in Section 2.3.4.12, “Port L Test Enable Register (PTTEL) for an override condition.

2.3.4.5 Port L Pull Select Register (PTPSL)

Address 0x0333 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTPSL1	PTPSL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-25. Port L Pull Select Register (PTPSL)

[1] Read: Anytime
Write: Anytime

Table 2-25. PTPSL Register Field Descriptions

Field	Description
1-0 PTPSL1-0	**Port L Pull Select —** This bit selects a pull device on the HVI pin in analog mode for open input detection. By default a pulldown device is active as part of the input voltage divider. If this bit set to 1 and PTTEL=1 and not in stop mode a pullup to a level close to V_{DDX} takes effect and overrides the weak pulldown device. Refer to Section 2.5.5, “Open Input Detection on PL[1:0] (HVI)”). 1 Pullup enabled 0 Pulldown enabled

accesses to mask out individual data bus bits and to use R/W access qualification in the comparison. Comparators can be configured to monitor a range of addresses.

When configured for data access comparisons, the match is generated if the address (and optionally data) of a data access matches the comparator value.

Configured for monitoring opcode addresses, the match is generated when the associated opcode reaches the execution stage of the instruction queue, but before execution of that opcode.

When a match with a comparator register value occurs, the associated control logic can force the state sequencer to another state (see Figure 6-19).

The state sequencer can transition freely between the states 1, 2 and 3. On transition to Final State, a breakpoint can be generated and the state sequencer returns to state0, disarming the DBG.

Independent of the comparators, state sequencer transitions can be forced by the external event input or by writing to the TRIG bit in the DBGC1 control register.

6.4.2 Comparator Modes

The DBG contains three comparators, A, B, and D. Each comparator compares the address stored in DBGXAH, DBGXAM, and DBGXAL with the PC (opcode addresses) or selected address bus (data accesses). Furthermore, comparator A can compare the data buses to values stored in DBGXD3-0 and allow data bit masking.

The comparators can monitor the buses for an exact address or an address range. The comparator configuration is controlled by the control register contents and the range control by the DBGC2 contents.

The comparator control register also allows the type of data access to be included in the comparison through the use of the RWE and RW bits. The RWE bit controls whether the access type is compared for the associated comparator and the RW bit selects either a read or write access for a valid match.

The INST bit in each comparator control register is used to determine the matching condition. By setting INST, the comparator matches opcode addresses, whereby the databus, data mask, RW and RWE bits are ignored. The comparator register must be loaded with the exact opcode address.

The comparator can be configured to match memory access addresses by clearing the INST bit.

Each comparator match can force a transition to another state sequencer state (see Section 6.4.3, “Events”).

Once a successful comparator match has occurred, the condition that caused the original match is not verified again on subsequent matches. Thus if a particular data value is matched at a given address, this address may not contain that data value when a subsequent match occurs.

Match[0, 1, 3] map directly to Comparators [A, B, D] respectively, except in range modes (see Section 6.3.2.2, “Debug Control Register2 (DBGC2)”). Comparator priority rules are described in the event priority section (Section 6.4.3.4, “Event Priorities”).

8.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V7.

8.3.1 Module Memory Map

The S12CPMU_UHV_V7 registers are shown in Figure 8-3.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPMU RESERVED00	R	0	0	0	0	0	0	0	0
		W								
0x0001	CPMU RESERVED01	R	0	0	0	0	0	0	0	0
		W								
0x0002	CPMU RESERVED02	R	0	0	0	0	0	0	0	0
		W								
0x0003	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x0004	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0005	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0006	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0007	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x0008	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0009	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x000A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x000B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x000C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x000D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x000E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 8-3. CPMU Register Summary

8.3.2.20 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV_V7 temperature sense.

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 8-26. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 8-24. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 8-25 for trimming effects.

Table 8-25. Trimming Effect of HTTR

Bit	Trimming Effect
HTTR[3]	Increases V_{HT} twice of HTTR[2]
HTTR[2]	Increases V_{HT} twice of HTTR[1]
HTTR[1]	Increases V_{HT} twice of HTTR[0]
HTTR[0]	Increases V_{HT} (to compensate Temperature Offset)

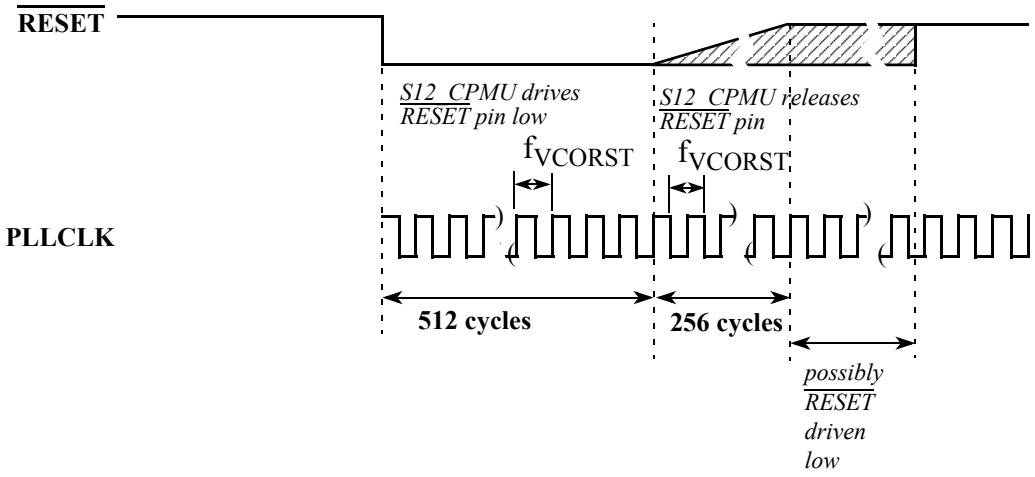
8.5.2 Description of Reset Operation

Upon detection of any reset of Table 8-33, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the $\overline{\text{RESET}}$ pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence.In case the $\overline{\text{RESET}}$ pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

NOTE

While System Reset is asserted the PLLCLK runs with the frequency f_{VCORST}.

Figure 8-40. RESET Timing



8.5.3 Oscillator Clock Monitor Reset

If the external oscillator is enabled (OSCE=1)and the oscillator clock monitor reset is enabled (OMRE=1), then in case of loss of oscillation or the oscillator frequency drops below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V7 generates an Oscillator Clock Monitor Reset. In Full Stop Mode the external oscillator and the oscillator clock monitor are disabled.

8.5.4 PLL Clock Monitor Reset

In case of loss of PLL clock oscillation or the PLL clock frequency is below the failure assert frequency f_{PMFA} (see device electrical characteristics for values), the S12CPMU_UHV_V7 generates a PLL Clock Monitor Reset[. In Full Stop Mode the PLL and the PLL clock monitor are disabled.

If signal Restart is asserted before signal LoadOK is set the conversion starts from top of currently active CSL at the next Trigger Event (no exchange of CSL list).
If signal Restart is asserted after or simultaneously with signal LoadOK the conversion starts from top of the other CSL at the next Trigger Event (CSL is switched) if CSL is configured for double buffer mode.

- **Sequence Abort Event**
  Internal Interface Signal: Seq_Abort
  Corresponding Bit Name: SEQA
  - *Function:*
    Abort any possible ongoing conversion at next conversion boundary and abort current conversion sequence and active CSL
  - *Requested by:*
    - Positive edge of internal interface signal Seq_Abort
    - Write Access via data bus to set control bit SEQA
  - *When finished:*
    This bit gets cleared when an ongoing conversion is finished and the result is stored and/or an ongoing conversion sequence is aborted and current active CSL is aborted (ADC idle, RVL done)
  - *Mandatory Requirement:*
    - In all ADC conversion flow control modes bit SEQA can only be set if:
    * ADC not idle (a conversion or conversion sequence is ongoing)
    * ADC idle but RVL done condition not reached
    The RVL done condition is not reached if:
    * An “End Of List” command type has not been executed
    * A Sequence Abort Event has not been executed (bit SEQA not already set)
    - In all ADC conversion flow control modes a Sequence Abort Event can be issued at any time
    - In ADC conversion flow control mode “Restart Mode” after a conversion sequence abort request has been executed it is mandatory to set bit RSTA. If a Trigger Event occurs before a Restart Event is executed (bit RSTA set and cleared by hardware), bit TRIG is set, error flag TRIG_EIF is set, and the ADC can only be continued by a Soft-Reset. After the Restart Event the ADC accepts new Trigger Events (bit TRIG set) and begins conversion from top of the currently active CSL.
    - In ADC conversion flow control mode “Restart Mode” after a Sequence Abort Event has been executed, a Restart Event causes only the RSTA bit being set. The ADC executes a Restart Event only.
  - In both conversion flow control modes (“Restart Mode” and “Trigger Mode”) when conversion flow control bit RSTA gets set automatically bit SEQA gets set when the ADC has not reached one of the following scenarios:
    * An “End Of List” command type has been executed or is about to be executed
    * A Sequence Abort request is about to be executed or has been executed.
    In case bit SEQA is set automatically the Restart error flag RSTA_EIF is set to indicate an unexpected Restart Request.

Table 13-10. PWMCTL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 CON67	**Concatenate Channels 6 and 7** 0 Channels 6 and 7 are separate 8-bit PWMs. 1 Channels 6 and 7 are concatenated to create one 16-bit PWM channel. Channel 6 becomes the high order byte and channel 7 becomes the low order byte. Channel 7 output pin is used as the output for this 16-bit PWM (bit 7 of port PWMP). Channel 7 clock select control-bit determines the clock source, channel 7 polarity bit determines the polarity, channel 7 enable bit enables the output and channel 7 center aligned enable bit determines the output mode.
6 CON45	**Concatenate Channels 4 and 5** 0 Channels 4 and 5 are separate 8-bit PWMs. 1 Channels 4 and 5 are concatenated to create one 16-bit PWM channel. Channel 4 becomes the high order byte and channel 5 becomes the low order byte. Channel 5 output pin is used as the output for this 16-bit PWM (bit 5 of port PWMP). Channel 5 clock select control-bit determines the clock source, channel 5 polarity bit determines the polarity, channel 5 enable bit enables the output and channel 5 center aligned enable bit determines the output mode.
5 CON23	**Concatenate Channels 2 and 3** 0 Channels 2 and 3 are separate 8-bit PWMs. 1 Channels 2 and 3 are concatenated to create one 16-bit PWM channel. Channel 2 becomes the high order byte and channel 3 becomes the low order byte. Channel 3 output pin is used as the output for this 16-bit PWM (bit 3 of port PWMP). Channel 3 clock select control-bit determines the clock source, channel 3 polarity bit determines the polarity, channel 3 enable bit enables the output and channel 3 center aligned enable bit determines the output mode.
4 CON01	**Concatenate Channels 0 and 1** 0 Channels 0 and 1 are separate 8-bit PWMs. 1 Channels 0 and 1 are concatenated to create one 16-bit PWM channel. Channel 0 becomes the high order byte and channel 1 becomes the low order byte. Channel 1 output pin is used as the output for this 16-bit PWM (bit 1 of port PWMP). Channel 1 clock select control-bit determines the clock source, channel 1 polarity bit determines the polarity, channel 1 enable bit enables the output and channel 1 center aligned enable bit determines the output mode.
3 PSWAI	**PWM Stops in Wait Mode —** Enabling this bit allows for lower power consumption in wait mode by disabling the input clock to the prescaler. 0 Allow the clock to the prescaler to continue while in wait mode. 1 Stop the input clock to the prescaler whenever the MCU is in wait mode.
2 PFRZ	**PWM Counters Stop in Freeze Mode** — In freeze mode, there is an option to disable the input clock to the prescaler by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode, the input clock to the prescaler is disabled. This feature is useful during emulation as it allows the PWM function to be suspended. In this way, the counters of the PWM can be stopped while in freeze mode so that once normal program flow is continued, the counters are re-enabled to simulate real-time operations. Since the registers can still be accessed in this mode, to re-enable the prescaler clock, either disable the PFRZ bit or exit freeze mode. 0 Allow PWM to continue while in freeze mode. 1 Disable PWM input clock to the prescaler whenever the part is in freeze mode. This is useful for emulation.

13.3.2.7 PWM Clock A/B Select Register (PWMCLKAB)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

15.4.7.5.2 SPIF

SPIF occurs when new data has been received and copied to the SPI data register. After SPIF is set, it does not clear until it is serviced. SPIF has an automatic clearing process, which is described in Section 15.3.2.4, “SPI Status Register (SPISR)”.

15.4.7.5.3 SPTEF

SPTEF occurs when the SPI data register is ready to accept new data. After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process, which is described in Section 15.3.2.4, “SPI Status Register (SPISR)”.

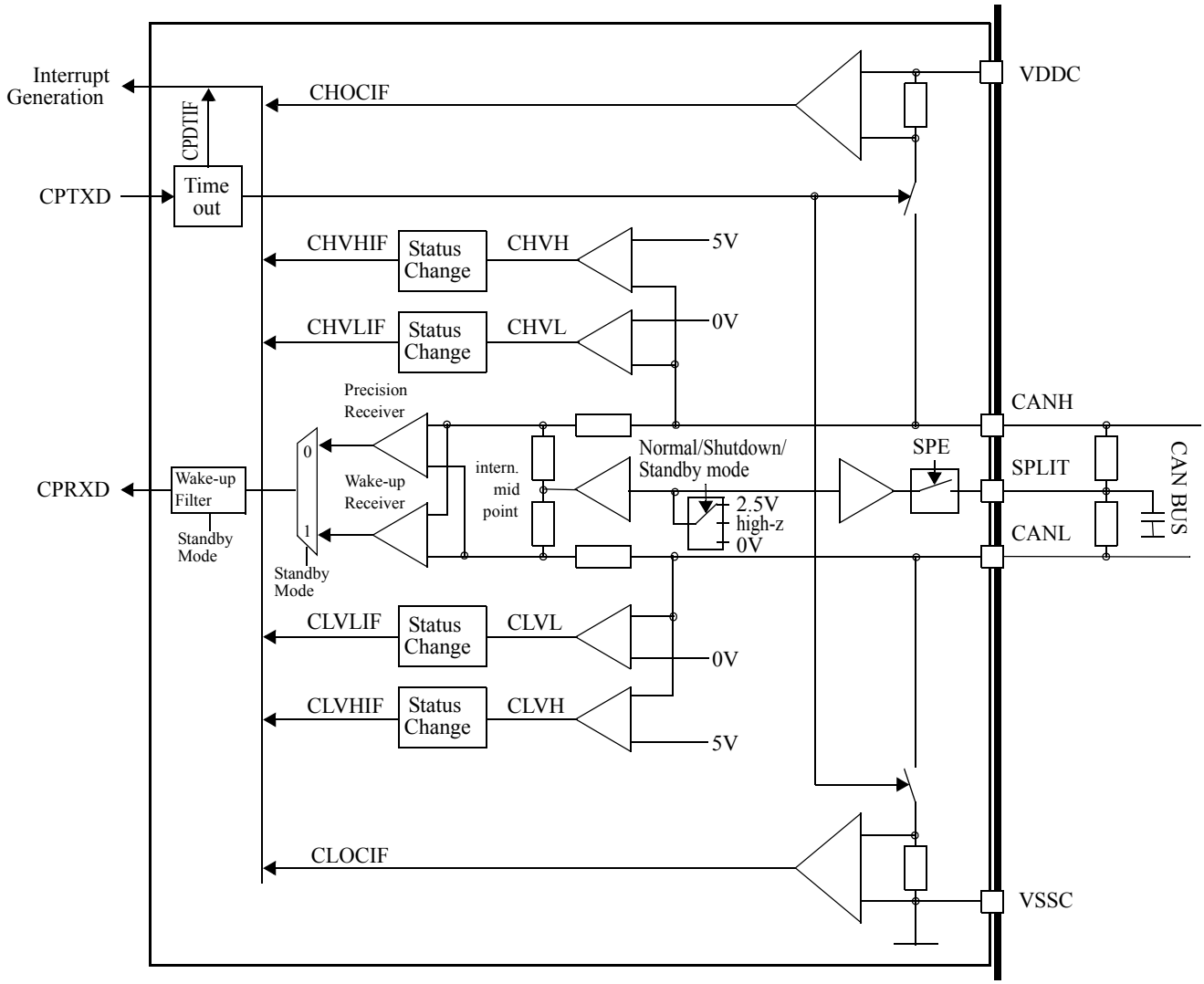


Figure 17-1. CAN Physical Layer Block Diagram

17.2 External Signal Description

Table 17-2 shows the external pins associated with the CAN Physical Layer.

Table 17-2. CAN Physical Layer Signal Properties

Name	Function
CANH	CAN Bus High Pin
SPLIT	2.5 V Termination Pin
CANL	CAN Bus Low Pin
VDDC	Supply Pin for CAN Physical Layer
VSSC	Ground Pin for CAN Physical Layer

17.4 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the CAN Physical Layer.

17.4.1 Module Memory Map

A summary of the registers associated with the CAN Physical Layer sub-block is shown in Table 17-3. Detailed descriptions of the registers and bits are given in the following sections.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPDR	R	CPDR7	0	0	0	0	0	CPDR1	CPDR0
		W								
0x0001	CPCR	R	CPE	SPE	WUPE1-0		0	SLR2-0		
		W								
0x0002	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0003	CPSR	R	CPCHVH	CPCHVL	CPCLVH	CPCLVL	CPDT	0	0	0
		W								
0x0004	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0005	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0006	CPIE	R	0	0	0	CPVFIE	CPDTIE	0	0	CPOCIE
		W								
0x0007	CPIF	R	CHVHIF	CHVLIF	CLVHIF	CLVLIF	CPDTIF	0	CHOCIF	CLOCIF
		W								

= Unimplemented or Reserved

Table 17-3. CAN Physical Layer Register Summary

[1] Read: Anytime
Write: Anytime when out of initialization mode; exceptions are read-only RXACT and SYNCH, RXFRM (which is set by the module only), and INITRQ (which is also writable in initialization mode)

NOTE

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 18-2. CANCTL0 Register Field Descriptions

Field	Description
7 RXFRM	**Received Frame Flag** — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode. 0 No valid message was received since last clearing this flag 1 A valid message was received since last clearing of this flag
6 RXACT	**Receiver Active Status** — This read-only flag indicates the MSCAN is receiving a message[1]. The flag is controlled by the receiver front end. This bit is not valid in loopback mode. 0 MSCAN is transmitting or idle 1 MSCAN is receiving a message (including when arbitration is lost)
5 CSWAI[2]	**CAN Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module. 0 The module is not affected during wait mode 1 The module ceases to be clocked during wait mode
4 SYNCH	**Synchronized Status** — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN. 0 MSCAN is not synchronized to the CAN bus 1 MSCAN is synchronized to the CAN bus
3 TIME	**Timer Enable** — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. Right after the EOF of a valid message on the CAN bus, the time stamp is written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 18.3.3, “Programmer’s Model of Message Storage”). In loopback mode no receive timestamp is generated. The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode. 0 Disable internal MSCAN timer 1 Enable internal MSCAN timer
2 WUPE[3]	**Wake-Up Enable** — This configuration bit allows the MSCAN to restart from sleep mode or from power down mode (entered from sleep) when traffic on CAN is detected (see Section 18.4.5.5, “MSCAN Sleep Mode”). This bit must be configured before sleep mode entry for the selected function to take effect. 0 Wake-up disabled — The MSCAN ignores traffic on CAN 1 Wake-up enabled — The MSCAN is able to restart

An option exists to also include the status and serial communication nibble into the automatic CRC calculation (CONFIG[CRCSCN]=1).

21.8.2 Transmitter States

- Init State

  After system reset the SENTTX module starts up in Init State, which means the transmitter is initially disabled with all configuration registers (e.g. TICKRATE, PPULSE, CONFIG) writeable. Additionally, all interrupt flags are held in their respective reset states.

  The Init State can be left by clearing the CONFIG[TXINIT] bit with CONFIG[TXEN] being set (clearing CONFIG[TXINIT] and setting CONFIG[TXEN] to leave Init State can be done in the same write access).

- Idle State

  After leaving Init State, the SENTTX module enters Idle State. In this state, the registers TICKRATE, PPULSE and CONFIG (except CONFIG[TXINIT]) are read-only.

  The module waits for software to clear INTFLG[TBE] which announces valid data in the transmit buffer (TXBUF). Clearing INTFLG[TBE] causes the module to enter Transmit State.

- Transmit State

  In Transmit State the SENTTX module transmits the data written by software into the TXBUF register. As long as there is data available in TXBUF the SENTTX module remains in Transmit State. If single-shot mode is active (CONFIG[SINGLE]=1) the module enters Idle State after transmission completes and no new data is available in TXBUF. Otherwise, when not in single-shot mode and no new data is available at the end of the calibration pulse period of a new message, the SENTTX module aborts the transmission, sets the Transmitter Under-run flag bit and enters Error State. The SENT_TX_OUT signal remains at idle level in case of a Transmitter Under-run condition.

  If the system enters Stop mode while the SENTTX module is in Transmit State, the module aborts the current transmission, resets interrupt flags INTFLG[PPRE,CS,TC,TBE] and enters Idle State. The SENT_TX_OUT signal switches to idle level in this case.

- Error State

  In this state transmission of messages is disabled. The module waits for the Transmitter Under-run flag bit to be cleared.

  When software clears the Transmitter Under-run error flag bit, the module resets interrupt flags INTFLG[PPRE,CS,TC,TBE] and enters Idle State again.

Whenever software sets the CONFIG[TXINIT] bit, the SENTTX aborts any ongoing transmission, and resets interrupt flags INTFLG[PPRE,CS,TC,TBE]. The SENT_TX_OUT signal switches to idle level in this case. If the transmitter under-run error flag is set (INTFLG[TU]=1) when software sets the CONFIG[TXINIT] bit, the transmitter remains in Error State; else transmitter enters Init State.

region), and the remaining addresses in the Flash memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 22-3.

Table 22-3. Flash Configuration Field

Global Address	Size (Bytes)	Description
0xFF_FE00-0xFF_FE07	8	Backdoor Comparison Key Refer to Section 22.4.7.11, "Verify Backdoor Access Key Command," and Section 22.5.1, "Unsecuring the MCU using Backdoor Key Access"
0xFF_FE08-0xFF_FE09[1]	2	Protection Override Comparison Key. Refer to Section 22.4.7.17, "Protection Override Command"
0xFF_FE0A-0xFF_FE0B[1]	2	Reserved
0xFF_FE0C[1]	1	P-Flash Protection byte. Refer to Section 22.3.2.9, "P-Flash Protection Register (FPROT)"
0xFF_FE0D[1]	1	EEPROM Protection byte. Refer to Section 22.3.2.10, "EEPROM Protection Register (DFPROT)"
0xFF_FE0E[1]	1	Flash Nonvolatile byte Refer to Section 22.3.2.11, "Flash Option Register (FOPT)"
0xFF_FE0F[1]	1	Flash Security byte Refer to Section 22.3.2.2, "Flash Security Register (FSEC)"

1 0xFF_FE08-0xFF_FE0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0xFF_FE0A - 0xFF_FE0B reserved field should be programmed to 0xFF.

Table E-1. Voltage Regulator Electrical Characteristics (Junction Temperature From –40°C To +175°C)

VDDA and VDDX must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
11	Trimmed ACLK output frequency[4]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock $\Delta f / f_{nominal}$ [4]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage T_J=150°C untrimmed	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[5] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	Bandgap output voltage V_{SUP} dependency T_J =150°C, 3.5V < V_{SUP}<18V	Δ_{VBGV}	-5	—	5	mV
19	Bandgap output voltage temperature dependency V_{SUP}<18V, -40°C < T_J < 150°C	Δ_{VBGT}	-20	—	20	mV
20	Max. Base Current For External PNP (VDDX)[6] -40°C < T_J < 150°C	$I_{BCTLMAX}$	2.3	—	—	mA
21	Max. Base Current For External PNP (VDDX) 150°C < T_J < 175°C	$I_{BCTLMAX}$	1.5	—	—	mA
22	Max. Base Current For External PNP (VDDC) -40°C < T_J < 150°C	$I_{BCTLCMAX}$	2.3	—	—	mA
23	Max. Base Current For External PNP (VDDC) 150°C < T_J < 175°C	$I_{BCTLCMAX}$	1.5	—	—	mA
24	Recovery time from STOP	t_{STP_REC}	—	23	—	µs

[1] Please note that the core current is derived from VDDX

[2] LVI is monitored on the VDDA supply domain

[3] LVRX is monitored on the VDDX supply domain only active during full performance mode. During reduced performance mode (stop mode) voltage supervision is solely performed by the POR block monitoring core VDD.

[4] Nominal condition is T_a=25°C and VDDA=VDDX=5V

[5] VREGHTTR=0x88

[6] This is the minimum base current that can be guaranteed when the external PNP is delivering maximum current.

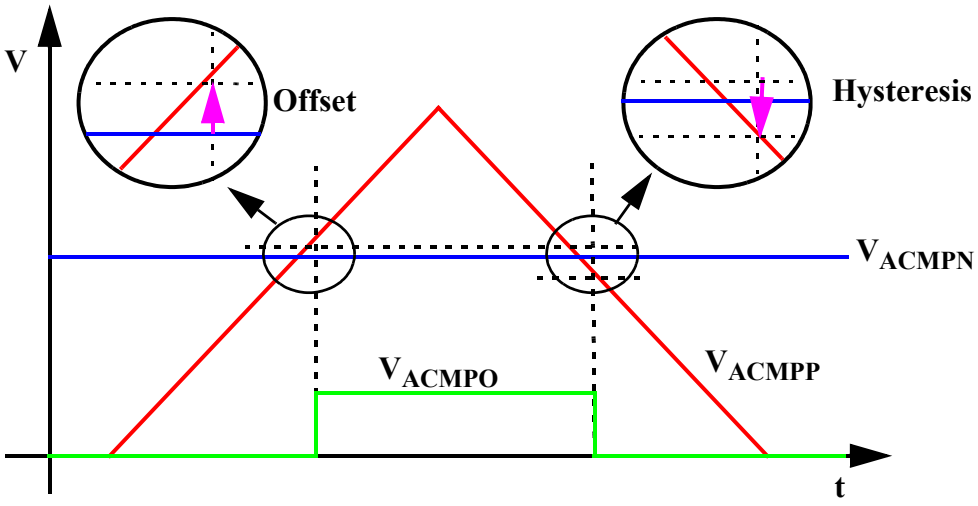
E.2 IRC and OSC Electrical Specifications

Table E-2. IRC electrical characteristics

Num	Rating	Symbol	Min	Typ	Max	Unit
1a	Internal Reference Frequency, factory trimmed -40°C < T_J < 150°C	f_{IRC1M_TRIM}	0.9895	1.002	1.0145	MHz
1b	Internal Reference Frequency, factory trimmed 150°C < T_J < 175°C	f_{IRC1M_TRIM}	0.9855		1.0145	MHz

[2] T_A: Ambient Temperature

Input Offset and Hysteresis



N.5 0x0200-0x037F S12ZVCPIM

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0200	MODRR0	R	IIC0RR1-0		SCI1RR	SCI0RR	SPI0RR	M0C0RR2-0		
		W								
0x0201	MODRR1	R	T1IC3RR	T1IC2RR	0	0	0	TRIG0NEG	TRIG0RR1-0	
		W								
0x0202	MODRR2	R	P0C7RR	0	0	0	P0C3RR	0	0	0
		W								
0x0203	MODRR3	R	0	0	0	T0IC3RR1	T0IC3RR0	T0IC2RR	T0IC1RR	0
		W								
0x0204–0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	ECLKCTL	R	NECLK	0	0	0	0	0	0	0
		W								
0x0209	IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								
0x020A–0x020D	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x020E	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x020F	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0210–0x025F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0260	PTE	R	0	0	0	0	0	0	PTE1	PTE0
		W								
0x0261	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0262	PTIE	R	0	0	0	0	0	0	PTIE1	PTIE0
		W								
0x0263	Reserved	R	0	0	0	0	0	0	0	0
		W								

N.10 0x0500-0x052F PWM1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x050C	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050D	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050E	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050F	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0510	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0511	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0512	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0513	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0514	PWMPER0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0515	PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0516	PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0517	PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0518	PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0519	PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x051A	PWMPER6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x051B	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x051C	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0