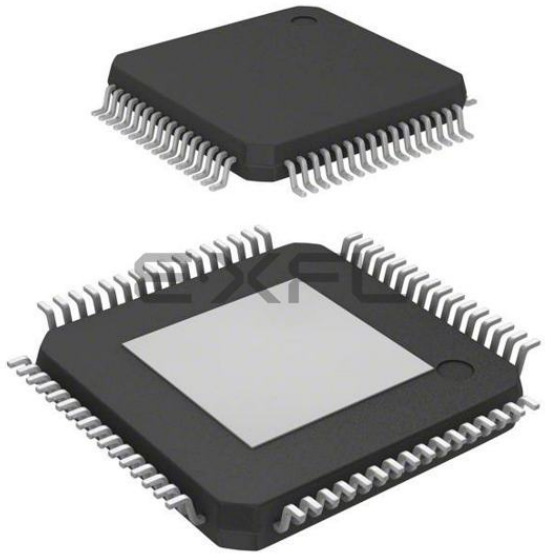

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Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 16x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc19f0mkhr

2.2.1 Internal Routing Options

The following table summarizes the internal routing options.

Table 2-3. Internal Routing Options

Internal Signal	Connects to	Routing Bits
ACMP0 out	TIM1 IC2	T1IC2RR
ACMP1 out	TIM1 IC3	T1IC3RR
ACLK	TIM0 IC2	T0IC2RR
RXD0, RXD1	TIM0 IC3	T0IC3RR1-0
TIM0 OC2	ADC0 Trigger	TRIG0RR1-0, TRIG0NEG

2.3 Memory Map and Register Definition

This section provides a detailed description of all port integration module registers.

Similarly the STEP1 command issued from a WAI instruction cannot be completed by the CPU until the CPU leaves wait mode due to an interrupt. The first STEP1 into wait mode sets the BDCCSR WAIT bit.

If the part is still in Wait mode and a further STEP1 is carried out then the NORESP and ILLCMD bits are set because the device is no longer in active BDM for the duration of WAI execution.

3.1.4 Block Diagram

A block diagram of the BDC is shown in Figure 3-1.

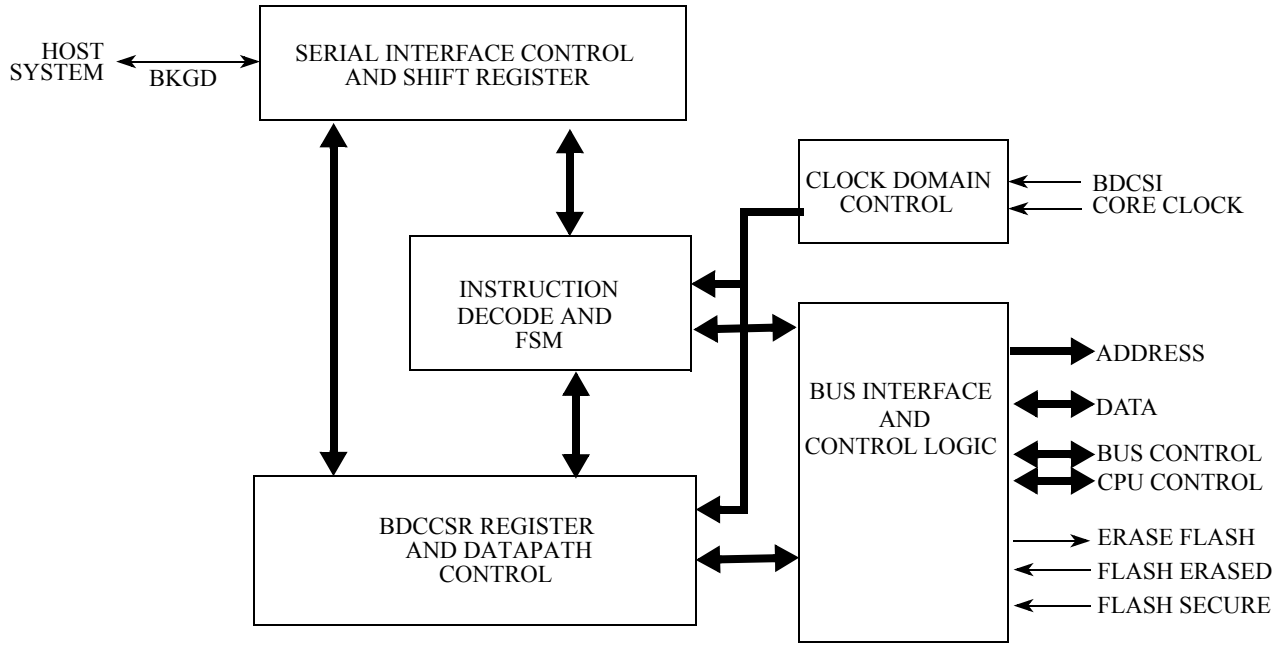


Figure 3-1. BDC Block Diagram

3.2 External Signal Description

A single-wire interface pin (BKGD) is used to communicate with the BDC system. During reset, this pin is a device mode select input. After reset, this pin becomes the dedicated serial interface pin for the BDC.

BKGD is a pseudo-open-drain pin with an on-chip pull-up. Unlike typical open-drain pins, the external RC time constant on this pin due to external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speed-up pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to Section 3.4.6, “BDC Serial Interface” for more details.

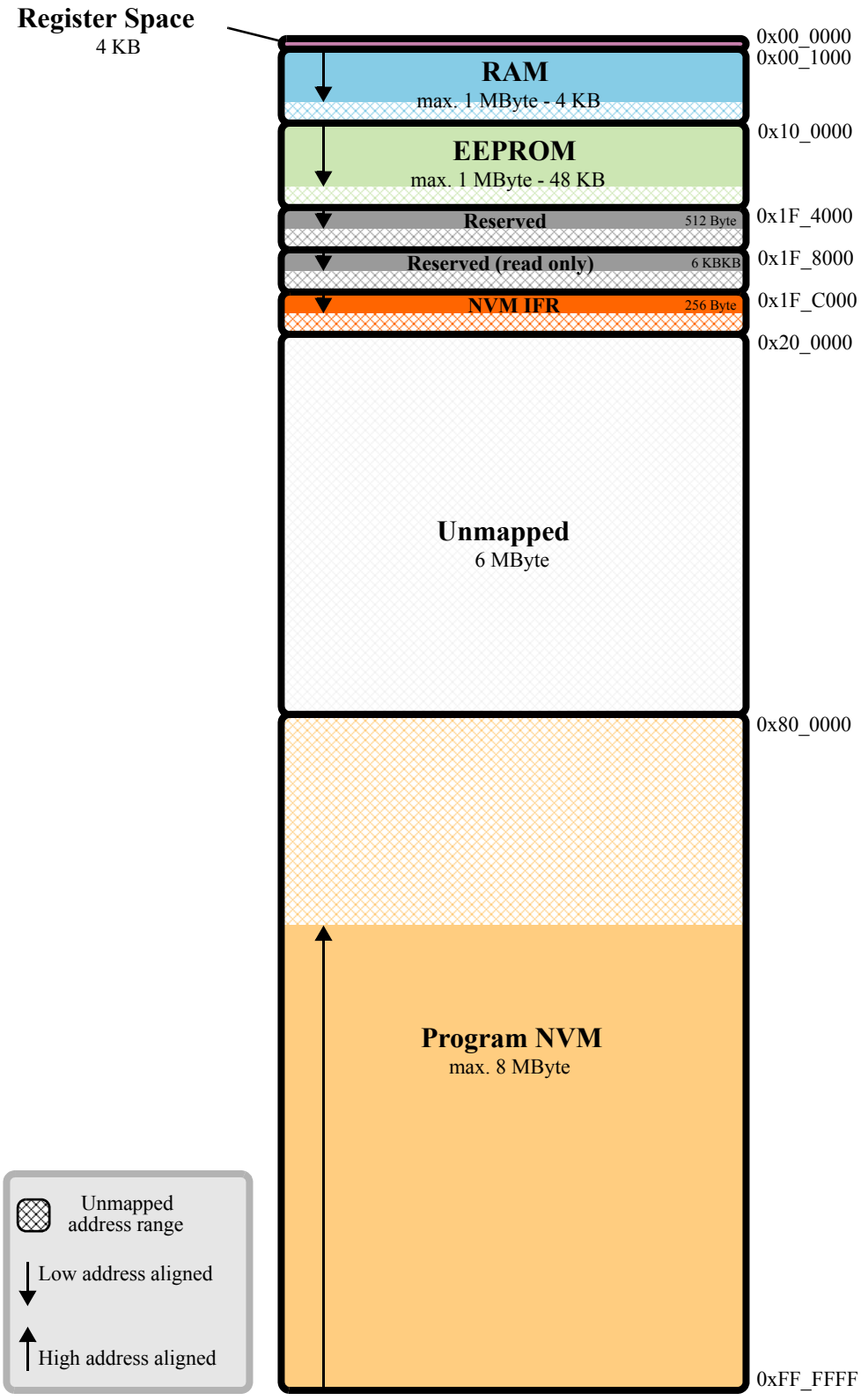


Figure 4-8. Global Memory Map

Chapter 6
S12Z DebugLite (S12ZDBGV3) Module

Table 6-1. Revision History Table

Revision Number	Revision Date	Sections Affected	Description Of Changes
3.00	23.MAY.2012	General	Updated for DBGV3 using conditional text
3.01	27.JUN.2012	General	Added Lite to module name. Corrected DBGEFR register format issue
3.02	05.JUL.2012	Section 6.3.2.6, “Debug Event Flag Register (DBGEFR)	Removed ME2 flag from DBGEFR
3.03	16.NOV.2012	Section 6.5.1, “Avoiding Unintended Breakpoint Re-triggering	Modified step over breakpoint information
3.04	19.DEC.2012	General	Formatting corrections
3.05	19.APR.2013	General	Specified DBGC1[0] reserved bit as read only
3.06	15.JUL.2013	Section 6.3.2, “Register Descriptions	Added explicit names to state control register bit fields

6.1 Introduction

The DBG module provides on-chip breakpoints with flexible triggering capability to allow non-intrusive debug of application software. The DBG module is optimized for the S12Z architecture and allows debugging of CPU module operations.

Typically the DBG module is used in conjunction with the BDC module, whereby the user configures the DBG module for a debugging session over the BDC interface. Once configured the DBG module is armed and the device leaves active BDM returning control to the user program, which is then monitored by the DBG module. Alternatively the DBG module can be configured over a serial interface using SWI routines.

Chapter 8
S12 Clock, Reset and Power Management Unit (S12CPMU_UHV_V7)

Revision History

Rev. No. (Item No)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V07.00	6 March 2013		• copied from V5 • adapted for Hearst: added VDDC, added EXTCON Bit
V07.01	13 June 2013		• EXTCON register Bit: correct reset value to 1 • PMRF register Bit: corrected description
V07.02	21 Aug. 2013		• correct bit numbering for CSAD Bit • f_{PLLRST} changed to f_{VCORST} • changed frequency upper limit of external Pierce Oscillator (XOSCLCP) from 16MHz to 20MHz • corrected typo in heading of CPMUOSC2 Field Description • Memory Map, CPMUAPIRH register: corrected address typo

8.1 Introduction

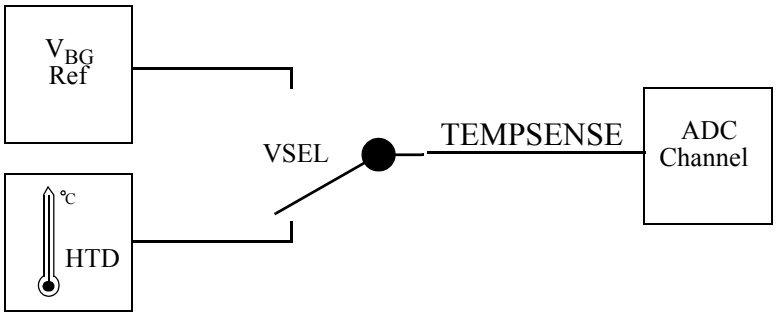
This specification describes the function of the Clock, Reset and Power Management Unit (S12CPMU_UHV_V7).

- The Pierce oscillator (XOSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators.
- The Voltage regulator (VREGAUTO) operates from the range 6V to 18V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.
- The Internal Reference Clock (IRC1M) provides a 1MHz internal clock.

Table 8-16. CPMUHTCTL Field Descriptions

Field	Description
5 VSEL	**Voltage Access Select Bit** — If set, the bandgap reference voltage V_{BG} can be accessed internally (i.e. multiplexed to an internal Analog to Digital Converter channel). If not set, the die temperature proportional voltage V_{HT} of the temperature sensor can be accessed internally. See device level specification for connectivity. For any of these access the HTE bit must be set. 0 An internal temperature proportional voltage V_{HT} can be accessed internally. 1 Bandgap reference voltage V_{BG} can be accessed internally.
3 HTE	**High Temperature Sensor/Bandgap Voltage Enable Bit** — This bit enables the high temperature sensor and bandgap voltage amplifier. 0 The temperature sensor and bandgap voltage amplifier is disabled. 1 The temperature sensor and bandgap voltage amplifier is enabled.
2 HTDS	**High Temperature Detect Status Bit** — This read-only status bit reflects the temperature status. Writes have no effect. 0 Junction Temperature is below level T_{HTID} or RPM. 1 Junction Temperature is above level T_{HTIA} and FPM.
1 HTIE	**High Temperature Interrupt Enable Bit** 0 Interrupt request is disabled. 1 Interrupt will be requested whenever HTIF is set.
0 HTIF	**High Temperature Interrupt Flag** — HTIF is set to 1 when HTDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (HTIE=1), HTIF causes an interrupt request. 0 No change in HTDS bit. 1 HTDS bit has changed.

Figure 8-18. Voltage Access Select



8.3.2.21 S12CPMU_UHV_V7 IRC1M Trim Registers (CPMUIRCTRIMH / CPMUIRCTRIML)

Module Base + 0x0018

	15	14	13	12	11	10	9	8
R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
W								
Reset	F	F	F	F	F	0	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-27. S12CPMU_UHV_V7 IRC1M Trim High Register (CPMUIRCTRIMH)

Module Base + 0x0019

	7	6	5	4	3	2	1	0
R	IRCTRIM[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Figure 8-28. S12CPMU_UHV_V7 IRC1M Trim Low Register (CPMUIRCTRIML)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register). Else write has no effect

NOTE

Writes to these registers while PLLSEL=1 clears the LOCK and UPOSC status bits.

Table 8-26. CPMUIRCTRIMH/L Field Descriptions

Field	Description
15-11 TCTRIM[4:0]	**IRC1M temperature coefficient Trim Bits** Trim bits for the Temperature Coefficient (TC) of the IRC1M frequency. Table 8-27 shows the influence of the bits TCTRIM[4:0] on the relationship between frequency and temperature. Figure 8-30 shows an approximate TC variation, relative to the nominal TC of the IRC1M (i.e. for TCTRIM[4:0]=0x00000 or 0x10000).
9-0 IRCTRIM[9:0]	**IRC1M Frequency Trim Bits** — Trim bits for Internal Reference Clock After System Reset the factory programmed trim value is automatically loaded into these registers, resulting in a Internal Reference Frequency f_{IRC1M_TRIM}.See device electrical characteristics for value of f_{IRC1M_TRIM}. The frequency trimming consists of two different trimming methods: A rough trimming controlled by bits IRCTRIM[9:6] can be done with frequency leaps of about 6% in average. A fine trimming controlled by bits IRCTRIM[5:0] can be done with frequency leaps of about 0.3% (this trimming determines the precision of the frequency setting of 0.15%, i.e. 0.3% is the distance between two trimming values). Figure 8-29 shows the relationship between the trim bits and the resulting IRC1M frequency.

- **MCU Wait Mode**
  Depending on the ADC Wait Mode configuration bit SWAI, the ADC either continues conversion in MCU Wait Mode or freezes conversion at the next conversion boundary before MCU Wait Mode is entered.

  ADC behavior for configuration SWAI =1'b0:
  The ADC continues conversion during Wait Mode according to the conversion flow control sequence. It is assumed that the conversion flow control sequence is continued (conversion flow control bits TRIG, RSTA, SEQA, and LDOK are serviced accordingly).

  ADC behavior for configuration SWAI = 1'b1:
  At MCU Wait Mode request the ADC should be idle (no conversion or conversion sequence or Command Sequence List ongoing).
  If a conversion, conversion sequence, or CSL is in progress when an MCU Wait Mode request is issued, a Sequence Abort Event occurs automatically and any ongoing conversion finish. After the Sequence Abort Event finishes, if the STR_SEQA bit is set (STR_SEQA=1), then the conversion result is stored and the corresponding flags are set. If the STR_SEQA bit is cleared (STR_SEQA=0), then the conversion result is not stored and the corresponding flags are not set.
  Alternatively the Sequence Abort Event can be issued by software before MCU Wait Mode request. As soon as flag SEQAD_IF is set, the MCU Wait Mode request can be issued.
  With the occurrence of the MCU Wait Mode request until exit from Wait Mode all flow control signals (RSTA, SEQA, LDOK, TRIG) are cleared.
  After exiting MCU Wait Mode, the following happens in the order given with expected event(s) depending on the conversion flow control mode:
  — In ADC conversion flow control mode "Trigger Mode", a Restart Event is expected to occur. This simultaneously sets bit TRIG and RSTA causing the ADC to execute the Restart Event (CMD_IDX and RVL_IDX cleared) followed by the Trigger Event. The Restart Event can be generated automatically after exit from MCU Wait Mode if bit AUT_RSTA is set.
  — In ADC conversion flow control mode "Restart Mode", a Restart Event is expected to set bit RSTA only (ADC already aborted at MCU Wait Mode entry hence bit SEQA must not be set simultaneously) causing the ADC to execute the Restart Event (CDM_IDX and RVL_IDX cleared). The Restart Event can be generated automatically after exit from MCU Wait Mode if bit AUT_RSTA is set.
  — The RVL buffer select (RVL_SEL) is not changed if a CSL is in process at MCU Wait Mode request. Hence the same RVL buffer will be used after exit from Wait Mode that was used when Wait Mode request occurred.

Table 9-10. Summary of Conversion Flow Control Bit Scenarios

RSTA	TRIG	SEQA	LDOK	Conversion Flow Control Mode	Conversion Flow Control Scenario
0	0	0	0	Both Modes	Valid
0	0	0	1	Both Modes	Can Not Occur
0	0	1	0	Both Modes	Valid[5]
0	0	1	1	Both Modes	Can Not Occur
0	1	0	0	Both Modes	Valid[2]
0	1	0	1	Both Modes	Can Not Occur
0	1	1	0	Both Modes	Can Not Occur
0	1	1	1	Both Modes	Can Not Occur
1	0	0	0	Both Modes	Valid[4]
1	0	0	1	Both Modes	Valid[1 4]
1	0	1	0	Both Modes	Valid[3 4 5]
1	0	1	1	Both Modes	Valid[1 3 4 5]
1	1	0	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2 4 6]
1	1	0	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[1 2 4 6]
1	1	1	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2 3 4 5 6]
1	1	1	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[1 2 3 4 5 6]

1 Swap CSL buffer

2 Start conversion sequence

3 Prevent RSTA_EIF and LDOK_EIF

4 Load conversion command from top of CSL

5 Abort any ongoing conversion, conversion sequence and CSL

6 Bit TRIG set automatically in Trigger Mode

For a detailed description of all conversion flow control bit scenarios please see also Section 9.5.3.2.4, “The two conversion flow control Mode Configurations, Section 9.5.3.2.5, “The four ADC conversion flow control bits and Section 9.5.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios

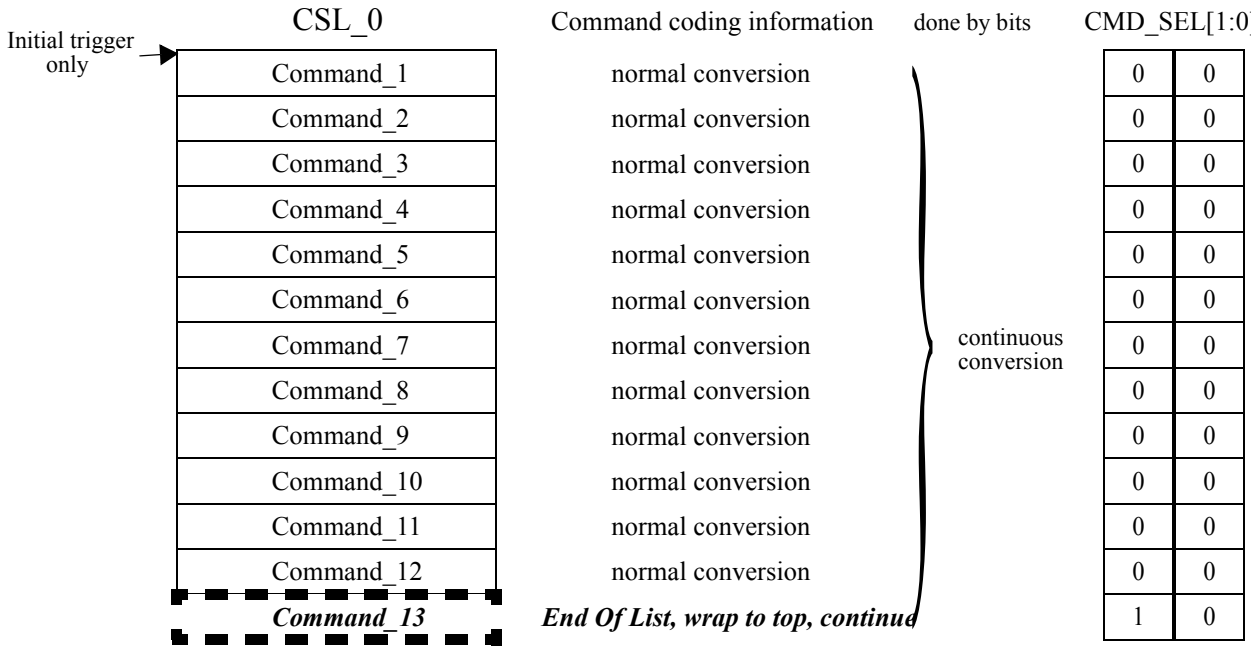


Figure 9-30. Example CSL for continues conversion

9.7.3 ADC Error and Conversion Flow Control Issue Interrupt

The ADC provides one error interrupt for four error classes related to conversion interrupt overflow, command validness, DMA access status and Conversion Flow Control issues, and CSL failure. The following error interrupt flags belong to the group of severe issues which cause an error interrupt if enabled and cease ADC operation:

- IA_EIF
- CMD_EIF
- EOL_EIF
- TRIG_EIF

In order to make the ADC operational again, an ADC Soft-Reset must be issued which clears the above listed error interrupt flags.

NOTE

It is important to note that if flag DBECC_ERR is set, the ADC ceases operation as well, but does not cause an ADC error interrupt. Instead, a machine exception is issued. In order to make the ADC operational again an ADC Soft-Reset must be issued.

Remaining error interrupt flags cause an error interrupt if enabled, but ADC continues operation. The related interrupt flags are:

- RSTAR_EIF
- LDOK_EIF
- CONIF_OIF

9.8.7 Conversion flow control application information

The ADC12B_LBA provides various conversion control scenarios to the user accomplished by the following features.

The ADC conversion flow control can be realized via the data bus only, the internal interface only, or by both access methods. The method used is software configurable via bits ACC_CFG[1:0].

The conversion flow is controlled via the four conversion flow control bits: SEQA, TRIG, RSTA, and LDOK.

Two different conversion flow control modes can be configured: Trigger Mode or Restart Mode

Single or double buffer configuration of CSL and RVL.

9.8.7.1 Initial Start of a Command Sequence List

At the initial start of a Command Sequence List after device reset all entries for at least one of the two CSL must have been completed and data must be valid. Depending on if the CSL_0 or the CSL_1 should be executed at the initial start of a Command Sequence List the following conversion control sequence must be applied:

If CSL_0 should be executed at the initial conversion start after device reset:
A Restart Event and a Trigger Event must occur (depending to the selected conversion flow control mode the events must occur one after the other or simultaneously) which causes the ADC to start conversion with commands loaded from CSL_0.

If CSL_1 should be executed at the initial conversion start after device reset:
Bit LDOK must be set simultaneously with the Restart Event followed by a Trigger Event (depending on the selected conversion flow control mode the Trigger events must occur simultaneously or after the Restart Event is finished). As soon as the Trigger Event gets executed the ADC starts conversion with commands loaded from CSL_1.

As soon as a new valid Restart Event occurs the flow for ADC register load at conversion sequence start as described in Section 9.5.3.3, “ADC List Usage and Conversion/Conversion Sequence Flow Description applies.

9.8.7.2 Restart CSL execution with currently active CSL

To restart a Command Sequence List execution it is mandatory that the ADC is idle (no conversion or conversion sequence is ongoing).

If necessary, a possible ongoing conversion sequence can be aborted by the Sequence Abort Event (setting bit SEQA). As soon as bit SEQA is cleared by the ADC, the current conversion sequence has been aborted and the ADC is idle (no conversion sequence or conversion ongoing).

After a conversion sequence abort is executed it is mandatory to request a Restart Event (bit RSTA set). After the Restart Event is finished (bit RSTA is cleared), the ADC accepts a new Trigger Event (bit TRIG can be set) and begins conversion from the top of the currently active CSL. In conversion flow control

Chapter 10
Supply Voltage Sensor - (BATSV3)

Table 10-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
V01.00	15 Dec 2010	all	Initial Version
V02.00	16 Mar 2011	10.3.2.1 10.4.2.1	- added BVLS[1] to support four voltage level - moved BVHS to register bit 6
V03.00	26 Apr 2011	all	- removed Vsense
V03.10	04 Oct 2011	10.4.2.1 and 10.4.2.2	- removed BSESE

10.1 Introduction

The BATS module provides the functionality to measure the voltage of the chip supply pin VSUP.

10.1.1 Features

The VSUP pin can be routed via an internal divider to the internal Analog to Digital Converter. Independent of the routing to the Analog to Digital Converter, it is possible to route this voltage to a comparator to generate a low or a high voltage interrupt to alert the MCU.

10.1.2 Modes of Operation

The BATS module behaves as follows in the system power modes:

1. Run mode

   The activation of the VSUP Level Sense Enable (BSUSE=1) or ADC connection Enable (BSUAE=1) closes the path from VSUP pin through the resistor chain to ground and enables the associated features if selected.

2. Stop mode

   During stop mode operation the path from the VSUP pin through the resistor chain to ground is opened and the low and high voltage sense features are disabled.
   The content of the configuration register is unchanged.

NOTE

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

11.3.2.12 Main Timer Interrupt Flag 1 (TFLG1)

Module Base + 0x000E

	7	6	5	4	3	2	1	0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 11-20. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write: Used in the clearing mechanism (set bits cause corresponding bits to be cleared). Writing a zero will not affect current status of the bit.

Table 11-16. TRLG1 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 C[7:0]F	**Input Capture/Output Compare Channel "x" Flag** — These flags are set when an input capture or output compare event occurs. Clearing requires writing a one to the corresponding flag bit while TEN or PAEN is set to one. **Note:** When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel (0x0010–0x001F) will cause the corresponding channel flag CxF to be cleared.

11.3.2.13 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-21. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 or PAEN bit of PACTL is set to one.

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 11-23. PTPSR Field Descriptions

Field	Description
7:0 PTPS[7:0]	**Precision Timer Prescaler Select Bits** — These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 11-24 shows some selection examples in this case. The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

The Prescaler can be calculated as follows depending on logical value of the PTPS[7:0] and PRNT bit:

PRNT = 1 : Prescaler = PTPS[7:0] + 1

Table 11-24. Precision Timer Prescaler Selection Examples when PRNT = 1

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
0	0	0	1	0	0	1	1	20
0	0	0	1	0	1	0	0	21
0	0	0	1	0	1	0	1	22
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	253
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

11.4 Functional Description

This section provides a complete functional description of the timer TIM16B8CV3 block. Please refer to the detailed timer block diagram in Figure 11-30 as necessary.

Table 13-4. PWMCLK Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7-0 PCLK[7:0]	**Pulse Width Channel 7-0 Clock Select** 0 Clock A or B is the clock source for PWM channel 7-0, as shown in Table 13-5 and Table 13-6. 1 Clock SA or SB is the clock source for PWM channel 7-0, as shown in Table 13-5 and Table 13-6.

The clock source of each PWM channel is determined by PCLKx bits in PWMCLK and PCLKABx bits in PWMCLKAB (see Section 13.3.2.7, “PWM Clock A/B Select Register (PWMCLKAB)). For Channel 0, 1, 4, 5, the selection is shown in Table 13-5; For Channel 2, 3, 6, 7, the selection is shown in Table 13-6.

Table 13-5. PWM Channel 0, 1, 4, 5 Clock Source Selection

PCLKAB[0,1,4,5]	PCLK[0,1,4,5]	Clock Source Selection
0	0	Clock A
0	1	Clock SA
1	0	Clock B
1	1	Clock SB

Table 13-6. PWM Channel 2, 3, 6, 7 Clock Source Selection

PCLKAB[2,3,6,7]	PCLK[2,3,6,7]	Clock Source Selection
0	0	Clock B
0	1	Clock SB
1	0	Clock A
1	1	Clock SA

13.3.2.4 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-6. PWM Prescale Clock Select Register (PWMPRCLK)

Read: Anytime

Write: Anytime

NOTE

PCKB2–0 and PCKA2–0 register bits can be written anytime. If the clock pre-scale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

14.1.4 Block Diagram

Figure 14-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

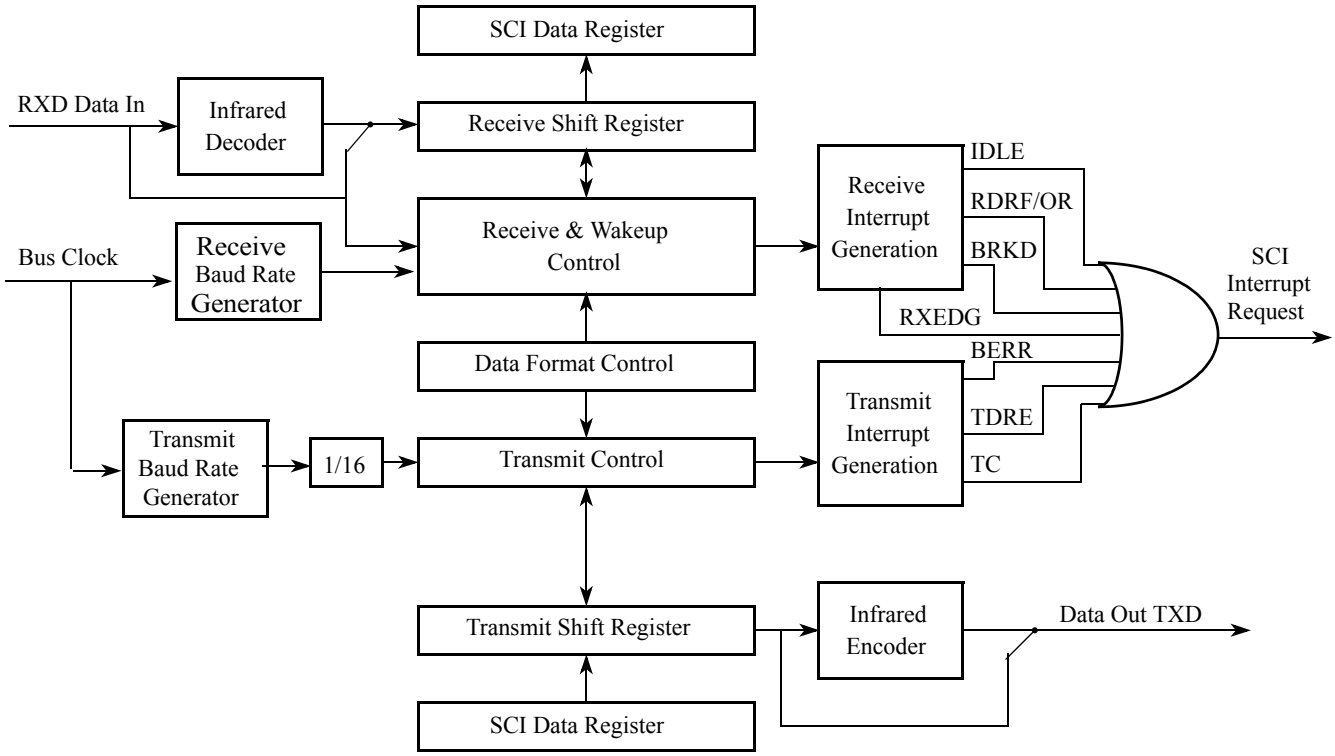


Figure 14-1. SCI Block Diagram

Table 16-8. IBCR Field Descriptions

Field	Description
7 IBEN	**I-Bus Enable** — This bit controls the software reset of the entire IIC bus module. 0 The module is reset and disabled. This is the power-on reset situation. When low the interface is held in reset but registers can be accessed 1 The IIC bus module is enabled.This bit must be set before any other IBCR bits have any effect If the IIC bus module is enabled in the middle of a byte transfer the interface behaves as follows: slave mode ignores the current transfer on the bus and starts operating whenever a subsequent start condition is detected. Master mode will not be aware that the bus is busy, hence if a start cycle is initiated then the current bus cycle may become corrupt. This would ultimately result in either the current bus master or the IIC bus module losing arbitration, after which bus operation would return to normal.
6 IBIE	**I-Bus Interrupt Enable** 0 Interrupts from the IIC bus module are disabled. Note that this does not clear any currently pending interrupt condition 1 Interrupts from the IIC bus module are enabled. An IIC bus interrupt occurs provided the IBIF bit in the status register is also set.
5 MS/SL	**Master/Slave Mode Select Bit** — Upon reset, this bit is cleared. When this bit is changed from 0 to 1, a START signal is generated on the bus, and the master mode is selected. When this bit is changed from 1 to 0, a STOP signal is generated and the operation mode changes from master to slave.A STOP signal should only be generated if the IBIF flag is set. MS/$\overline{SL}$ is cleared without generating a STOP signal when the master loses arbitration. 0 Slave Mode 1 Master Mode
4 Tx/Rx	**Transmit/Receive Mode Select Bit** — This bit selects the direction of master and slave transfers. When addressed as a slave this bit should be set by software according to the SRW bit in the status register. In master mode this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit will always be high. 0 Receive 1 Transmit
3 TXAK	**Transmit Acknowledge Enable** — This bit specifies the value driven onto SDA during data acknowledge cycles for both master and slave receivers. The IIC module will always acknowledge address matches, provided it is enabled, regardless of the value of TXAK. Note that values written to this bit are only used when the IIC bus is a receiver, not a transmitter. 0 An acknowledge signal will be sent out to the bus at the 9th clock bit after receiving one byte data 1 No acknowledge signal response is sent (i.e., acknowledge bit = 1)
2 RSTA	**Repeat Start** — Writing a 1 to this bit will generate a repeated START condition on the bus, provided it is the current bus master. This bit will always be read as a low. Attempting a repeated start at the wrong time, if the bus is owned by another master, will result in loss of arbitration. 1 Generate repeat start cycle
1 RESERVED	**Reserved** — Bit 1 of the IBCR is reserved for future compatibility. This bit will always read 0.
0 IBSWAI	**I Bus Interface Stop in Wait Mode** 0 IIC bus module clock operates normally 1 Halt IIC bus module clock generation in wait mode

Wait mode is entered via execution of a CPU WAI instruction. In the event that the IBSWAI bit is set, all clocks internal to the IIC will be stopped and any transmission currently in progress will halt.If the CPU were woken up by a source other than the IIC module, then clocks would restart and the IIC would resume from where was during the previous transmission. It is not possible for the IIC to wake up the CPU when its internal clocks are stopped.

If it were the case that the IBSWAI bit was cleared when the WAI instruction was executed, the IIC internal clocks and interface would remain alive, continuing the operation which was currently underway. It is also

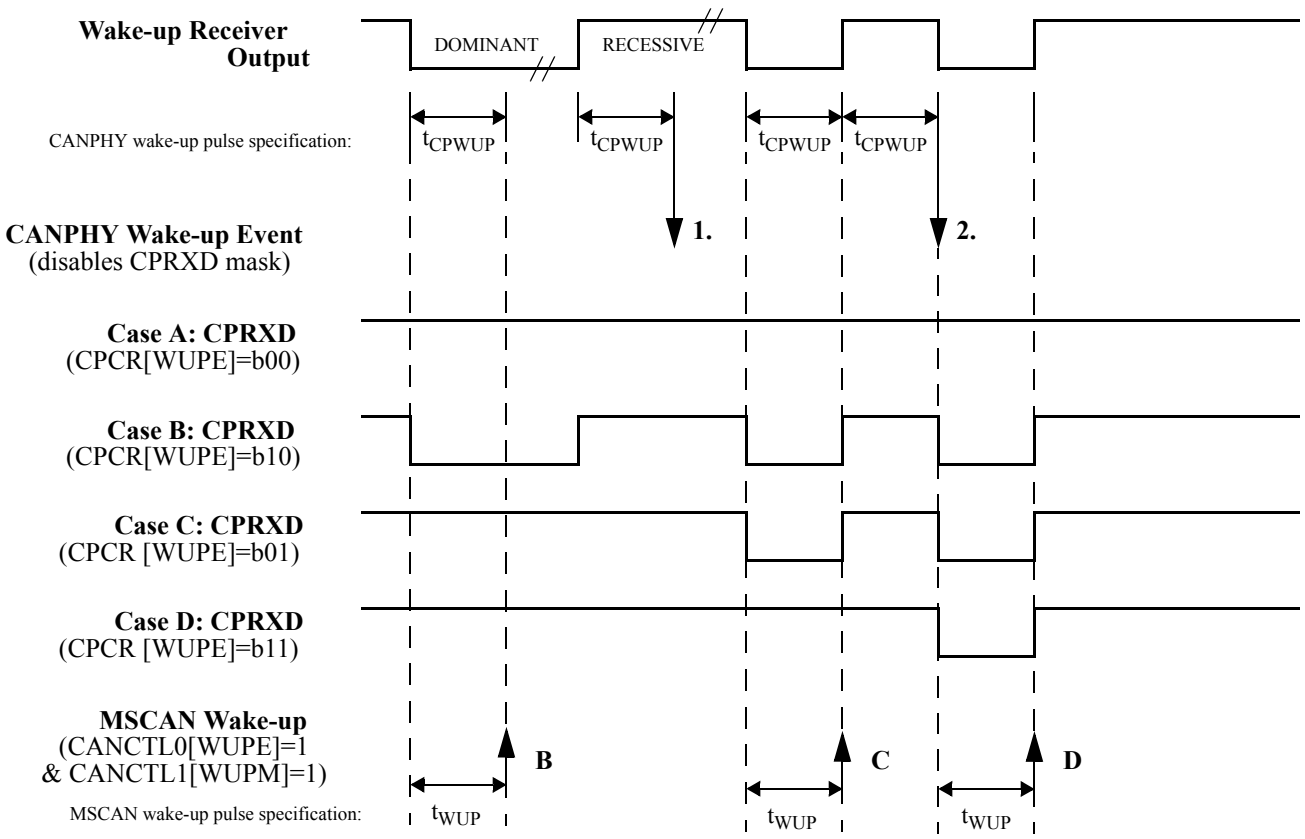


Figure 17-11. Wake-up Event Filtering

17.5.4 Interrupts

This section describes the interrupt generated by the CAN Physical Layer and its individual sources.

Vector addresses and interrupt priorities are defined at MCU level. The module internal interrupt sources are combined (OR-ed) into one module interrupt output CPI with a single local enable bit each for voltage failure and over-current errors.

Table 17-9. CAN Physical Layer Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
CAN Physical Layer Interrupt (CPI)	CANH Voltage Failure High Interrupt (CHVHIF)	CPVFIE = 1
	CANH Voltage Failure Low Interrupt (CHVLIF)	
	CANL Voltage Failure High Interrupt (CLVHIF)	
	CANL Voltage Failure Low Interrupt (CLVLIF)	
	CPTXD-Dominant Timeout Interrupt (CPDTIF)	CPDTIE = 1
	CANH Over-Current Interrupt (CHOCIF)	CPOCIE = 1
	CANL Over-Current Interrupt (CLOCIF)	

Table E-1. Voltage Regulator Electrical Characteristics (Junction Temperature From –40°C To +175°C)

VDDA and VDDX must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
11	Trimmed ACLK output frequency[4]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock $\Delta f / f_{nominal}$ [4]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage T_J=150°C untrimmed	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[5] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	Bandgap output voltage V_{SUP} dependency T_J =150°C, 3.5V < V_{SUP}<18V	Δ_{VBGV}	-5	—	5	mV
19	Bandgap output voltage temperature dependency V_{SUP}<18V, -40°C < T_J < 150°C	Δ_{VBGT}	-20	—	20	mV
20	Max. Base Current For External PNP (VDDX)[6] -40°C < T_J < 150°C	$I_{BCTLMAX}$	2.3	—	—	mA
21	Max. Base Current For External PNP (VDDX) 150°C < T_J < 175°C	$I_{BCTLMAX}$	1.5	—	—	mA
22	Max. Base Current For External PNP (VDDC) -40°C < T_J < 150°C	$I_{BCTLCMAX}$	2.3	—	—	mA
23	Max. Base Current For External PNP (VDDC) 150°C < T_J < 175°C	$I_{BCTLCMAX}$	1.5	—	—	mA
24	Recovery time from STOP	t_{STP_REC}	—	23	—	µs

[1] Please note that the core current is derived from VDDX

[2] LVI is monitored on the VDDA supply domain

[3] LVRX is monitored on the VDDX supply domain only active during full performance mode. During reduced performance mode (stop mode) voltage supervision is solely performed by the POR block monitoring core VDD.

[4] Nominal condition is T_a=25°C and VDDA=VDDX=5V

[5] VREGHTTR=0x88

[6] This is the minimum base current that can be guaranteed when the external PNP is delivering maximum current.

E.2 IRC and OSC Electrical Specifications

Table E-2. IRC electrical characteristics

Num	Rating	Symbol	Min	Typ	Max	Unit
1a	Internal Reference Frequency, factory trimmed -40°C < T_J < 150°C	f_{IRC1M_TRIM}	0.9895	1.002	1.0145	MHz
1b	Internal Reference Frequency, factory trimmed 150°C < T_J < 175°C	f_{IRC1M_TRIM}	0.9855		1.0145	MHz