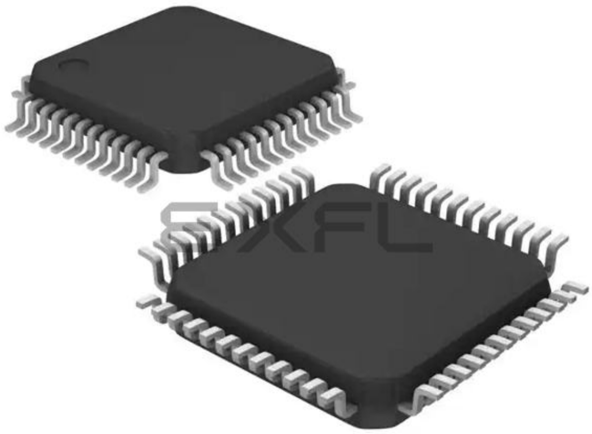

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc19f0mlfr

Chapter 9
Analog-to-Digital Converter (ADC12B_LBA_V1)

Chapter 10
Supply Voltage Sensor - (BATSV3)

1.4.1 S12Z Central Processor Unit (CPU)

The S12Z CPU is a revolutionary high-speed core, with code size and execution efficiencies over the S12X CPU. The S12Z CPU also provides a linear memory map eliminating the inconvenience and performance impact of page swapping.

- Harvard Architecture - parallel data and code access
- 3-stage pipeline
- 32-bit wide instruction and databus
- 32-bit ALU
- 24-bit addressing (16 MB linear address space)
- Instructions and Addressing modes optimized for C-Programming and Compiler
  - MAC unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

1.4.1.1 Background Debug Controller (BDC)

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compare the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus onlyEach comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax

1.7.30 Power Supply Pins

The power and ground pins are described below. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible.

NOTE

All ground pins must be connected together in the application.

1.7.30.1 VDDX1, VDDX2, VSSX1, VSSX2 — Digital I/O power and ground pins

VDDX is the voltage regulator output for the digital I/O drivers. It supplies the VDDX domain pads. The VSSX1 and VSSX2 pin is the ground pin for the digital I/O drivers.

Bypass capacitor requirements on VDDX/VSSX depend on how heavily the MCU pins are loaded.

1.7.30.2 VDDA, VSSA — Power supply pins for ADC

These are the power supply and ground pins for the analog-to-digital converter and the voltage regulator. These pins must be externally connected to the voltage regulator (VDDX, VSSX). A separate bypass capacitor for the ADC supply is recommended.

1.7.30.3 VSUP — Voltage supply pin

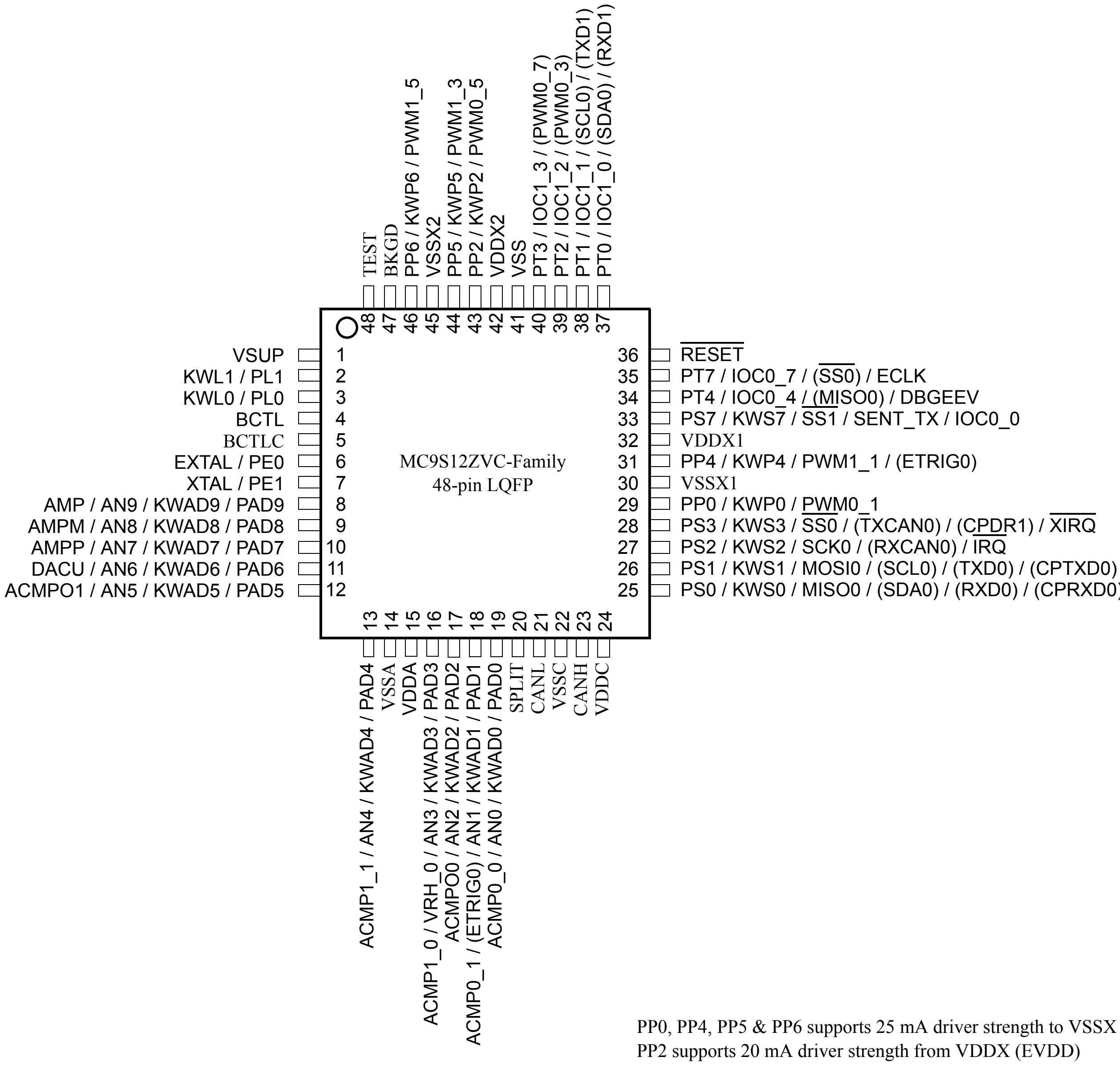
VSUP is the 12V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection.

1.8 Device Pinouts

The MC9S12ZVC-Family will be offered in 48 pin LQFP and 64 pin LQFP-EP packages. The exposed pad on the package bottom of the LQFP-EP package must be connected to a ground pad on the PCB.

:

Figure 1-3. Pinout MC9S12ZVC-Family 48-pin LQFP



NOTE

This document assumes the availability of all features offered in the largest package option. Refer to the package and pinout section in the device overview for functions not available in lower pin count packages.

2.1.2 Features

The PIM includes these distinctive registers:

- Data registers and data direction registers for ports E, AD, T, S, P and J when used as general-purpose I/O
- Control registers to enable pull devices and select pullups/pulldowns on ports E, AD, T, S, P and J
- Control register to enable open-drain (wired-or) mode on port S and J
- Control register to enable digital input buffers on port AD and L
- Interrupt flag register for pin interrupts and key-wakeup (KWU) on port AD, S, P and L
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Control register to enable ECLK output
- Routing registers to support signal relocation on external pins and control internal routings:
  - 2 PWM1 (fast) channels to alternative pins (1 option each)
  - 4 TIM0 channels to pins (1 option each)
  - IIC0 to alternative pins (2 options)
  - SCI0 to alternative pins (1 option)
  - SCI1 to alternative pins (1 option)
  - SPI0 to alternative pins (1 option)
  - ADC0 trigger input with edge select from internal TIM output compare channel link (OC0_2) or external pins (3 options)
  - Various MSCAN0-CANPHY0 routing options for standalone use and conformance testing
  - MSCAN0 to alternative pins (1 option)
  - Internal RXD0 and RXD1 link to TIM input capture channel (IC0_3) for baud rate detection
  - Internal ACLK link to TIM input capture channel (IC0_2) for calibration and clock monitoring purposes
  - SENT_TX pin link to 2 TIM0 input capture channels (IC0_0 and IC0_1)
  - Internal ACMP0 link to TIM1 (fast) input capture channel (IC1_2)
  - Internal ACMP1 link to TIM1 (fast) input capture channel (IC1_3)

A standard port pin has the following minimum features:

- Input/output selection
- 5V output drive
- 5V digital and analog input
- Input with selectable pullup or pulldown device

2.4.4.3 Over-Current Interrupt and Protection

In case of an over-current condition on PP2 (EVDD1) or PP[6-4,0] (see Section 2.5.3, “Over-Current Protection on PP2 (EVDD1)”” and 2.5.4, “Over-Current Protection on PP[6-4,0]””) the related over-current interrupt flag OCIFP[OCIFP] asserts. This flag generates an interrupt if the enable bit OCIEP[OCIEP] is set.

An asserted flag immediately forces the related output independent of its driving source (peripheral output or port register bit) to its disabled level to protect the device. The flag must be cleared to re-enable the driver.

2.4.5 High-Voltage Input

A high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to V_{HVI}
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wakeup from stop (pin interrupts in run mode not available). Open input detection.

Figure 2-35 shows a block diagram of the HVI.

NOTE

The term stop mode (STOP) is limited to voltage regulator operating in reduced performance mode (RPM). Refer to “Low Power Modes” section in device overview.

- Normal modes, secure device
  BDC disabled. No BDC access possible.
- Special single chip mode, unsecure
  BDM active out of reset. All BDC commands are available.
- Special single chip mode, secure
  BDM active out of reset. Restricted command set available.

When operating in secure mode, BDC operation is restricted to allow checking and clearing security by mass erasing the on-chip flash memory. Secure operation prevents BDC access to on-chip memory other than mass erase. The BDC command set is restricted to those commands classified as Always-available.

3.1.3.3 Low-Power Modes

3.1.3.3.1 Stop Mode

The execution of the CPU STOP instruction leads to stop mode only when all bus masters (CPU, or others, depending on the device) have finished processing. The operation during stop mode depends on the ENBDC and BDCCIS bit settings as summarized in Table 3-3

Table 3-3. BDC STOP Operation Dependencies

ENBDC	BDCCIS	Description Of Operation
0	0	BDC has no effect on STOP mode.
0	1	BDC has no effect on STOP mode.
1	0	Only BDCSI clock continues
1	1	All clocks continue

A disabled BDC has no influence on stop mode operation. In this case the BDCSI clock is disabled in stop mode thus it is not possible to enable the BDC from within stop mode.

STOP Mode With BDC Enabled And BDCCIS Clear

If the BDC is enabled and BDCCIS is clear, then the BDC prevents the BDCCLK clock (Figure 3-5) from being disabled in stop mode. This allows BDC communication to continue throughout stop mode in order to access the BDCCSR register. All other device level clock signals are disabled on entering stop mode.

NOTE

This is intended for application debugging, not for fast flash programming.
Thus the CLKSW bit must be clear to map the BDCSI to BDCCLK.

With the BDC enabled, an internal acknowledge delays stop mode entry and exit by 2 BDCSI clock + 2 bus clock cycles. If no other module delays stop mode entry and exit, then these additional clock cycles represent a difference between the debug and not debug cases. Furthermore if a BDC internal access is being executed when the device is entering stop mode, then the stop mode entry is delayed until the internal access is complete (typically for 1 bus clock cycle).

Address: 0x000019

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1[1]

= Unimplemented or Reserved

Figure 5-6. Interrupt Request Configuration Data Register 1 (INT_CFDATA1)

1 Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1[1]

= Unimplemented or Reserved

Figure 5-7. Interrupt Request Configuration Data Register 2 (INT_CFDATA2)

1 Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1[1]

= Unimplemented or Reserved

Figure 5-8. Interrupt Request Configuration Data Register 3 (INT_CFDATA3)

1 Please refer to the notes following the PRIOLVL[2:0] description below.

Address: 0x00001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PRIOLVL[2:0]		
W								
Reset	0	0	0	0	0	0	0	1[1]

= Unimplemented or Reserved

Figure 5-9. Interrupt Request Configuration Data Register 4 (INT_CFDATA4)

1 Please refer to the notes following the PRIOLVL[2:0] description below.

8.1.1 Features

The Pierce Oscillator (XOSCLCP) contains circuitry to dynamically control current gain in the output amplitude. This ensures a signal with low harmonic distortion, low power and good noise immunity.

- Supports crystals or resonators from 4MHz to 20MHz.
- High noise immunity due to input hysteresis and spike filtering.
- Low RF emissions with peak-to-peak swing limited dynamically
- Transconductance (gm) sized for optimum start-up margin for typical crystals
- Dynamic gain control eliminates the need for external current limiting resistor
- Integrated resistor eliminates the need for external bias resistor
- Low power consumption: Operates from internal 1.8V (nominal) supply, Amplitude control limits power
- Optional oscillator clock monitor reset
- Optional full swing mode for higher immunity against noise injection on the cost of higher power consumption and increased emission

The Voltage Regulator (VREGAUTO) has the following features:

- Input voltage range from 6 to 18V (nominal operating range)
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR)
- Low-voltage reset (LVR)
- On Chip Temperature Sensor and Bandgap Voltage measurement via internal ADC channel.
- Voltage Regulator providing Full Performance Mode (FPM) and Reduced Performance Mode (RPM)
- External ballast device support to reduce internal power dissipation
- Capable of supplying both the MCU internally plus external components
- Over-temperature interrupt

The Phase Locked Loop (PLL) has the following features:

- Highly accurate and phase locked frequency multiplier
- Configurable internal filter for best stability and lock time
- Frequency modulation for defined jitter and reduced emission
- Automatic frequency lock detector
- Interrupt request on entry or exit from locked condition
- PLL clock monitor reset
- Reference clock either external (crystal) or internal square wave (1MHz IRC1M) based.
- PLL stability is sufficient for LIN communication in slave mode, even if using IRC1M as reference clock

The Internal Reference Clock (IRC1M) has the following features:

frequency as shown in Table 8-2. Setting the VCOFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 8-2. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32MHz <= f_{VCO} <= 48MHz	00
48MHz < f_{VCO} <= 64MHz	01
Reserved	10
Reserved	11

8.3.2.3 S12CPMU_UHV_V7 Reference Divider Register (CPMUREFDIV)

The CPMUREFDIV register provides a finer granularity for the PLL multiplier steps when using the external oscillator as reference.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
W								
Reset	0	0	0	0	1	1	1	1

Figure 8-6. S12CPMU_UHV_V7 Reference Divider Register (CPMUREFDIV)

Read: Anytime

Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

If XOSCLCP is enabled (OSCE=1)

$$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If XOSCLCP is disabled (OSCE=0)

$$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 8-3.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1MHz <= f_{REF} <= 2MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

8.3.2.24 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV_V7's functionality.

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

(Shaded W cells of bits 5–1) = Unimplemented or Reserved

Figure 8-33. Reserved Register CPMUTEST2

Read: Anytime

Write: Only in Special Mode

Several examples of PLL divider settings are shown in Table 8-32. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 8-32. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.
- Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.

In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

Please see also the detailed conversion flow control bit mandatory requirements and execution information for bit RSTA and SEQA described in Section 9.5.3.2.5, “The four ADC conversion flow control bits.

9.8.8 Continuous Conversion

Applications that only need to continuously convert a list of channels, without the need for timing control or the ability to perform different sequences of conversions (grouped number of different channels to convert) can make use of the following simple setup:

- “Trigger Mode” configuration
- Single buffer CSL
- Depending on data transfer rate either use single or double buffer RVL configuration
- Define a list of conversion commands which only contains the “End Of List” command with automatic wrap to top of CSL

After finishing the configuration and enabling the ADC an initial Restart Event is sufficient to launch the continuous conversion until next device reset or low power mode.

In case a Low Power Mode is used:
If bit AUT_RSTA is set before Low Power Mode is entered the conversion continues automatically as soon as a low power mode (Stop Mode or Wait Mode with bit SWAI set) is exited.

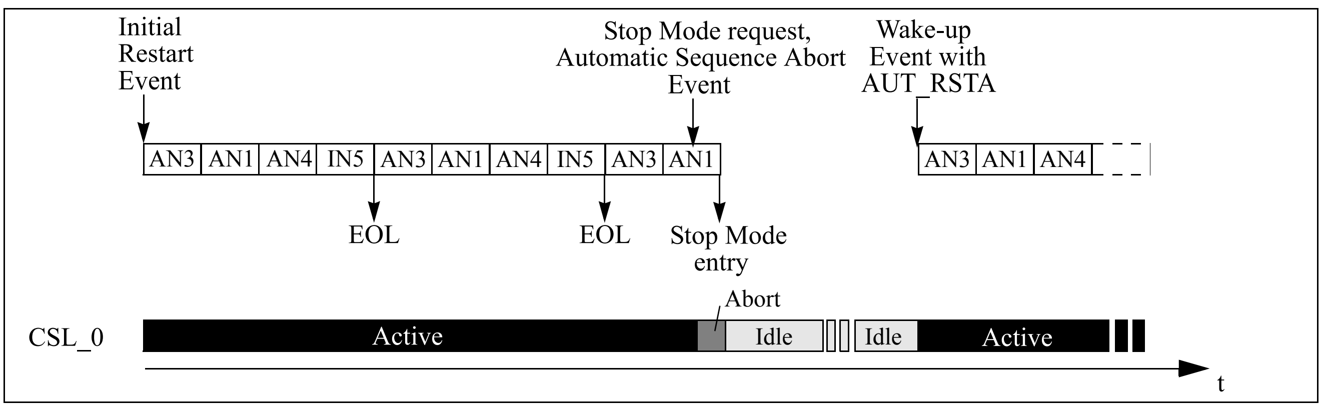


Figure 9-41. Conversion Flow Control Diagram — Continuous Conversion (with Stop Mode)

10.3.2.1 BATS Module Enable Register (BATE)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	BVHS	BVLS[1:0]		BSUAE	BSUSE	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-3. BATS Module Enable Register (BATE)

[1] Read: Anytime
Write: Anytime

Table 10-2. BATE Field Description

Field	Description
6 BVHS	**BATS Voltage High Select** — This bit selects the trigger level for the Voltage Level High Condition (BVHC). 0 Voltage level V_{HBI1} is selected 1 Voltage level V_{HBI2} is selected
5:4 BVLS[1:0]	**BATS Voltage Low Select** — This bit selects the trigger level for the Voltage Level Low Condition (BVLC). 00 Voltage level V_{LBI1} is selected 01 Voltage level V_{LBI2} is selected 10 Voltage level V_{LBI3} is selected 11 Voltage level V_{LBI4} is selected
3 BSUAE	**BATS VSUP ADC Connection Enable** — This bit connects the VSUP pin through the resistor chain to ground and connects the ADC channel to the divided down voltage. 0 ADC Channel is disconnected 1 ADC Channel is connected
2 BSUSE	**BATS VSUP Level Sense Enable** — This bit connects the VSUP pin through the resistor chain to ground and enables the Voltage Level Sense features measuring BVLC and BVHC. 0 Level Sense features disabled 1 Level Sense features enabled

NOTE

When opening the resistors path to ground by changing BSUSE or BSUAE then for a time T_{EN_UNC} + two bus cycles the measured value is invalid. This is to let internal nodes be charged to correct value. BVHIE, BVLIE might be cleared for this time period to avoid false interrupts.

14.3.2.3 SCI Alternative Status Register 1 (SCIASR1)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-6. SCI Alternative Status Register 1 (SCIASR1)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 14-5. SCIASR1 Field Descriptions

Field	Description
7 RXEDGIF	**Receive Input Active Edge Interrupt Flag** — RXEDGIF is asserted, if an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD input occurs. RXEDGIF bit is cleared by writing a “1” to it. 0 No active receive on the receive input has occurred 1 An active edge on the receive input has occurred
2 BERRV	**Bit Error Value** — BERRV reflects the state of the RXD input when the bit error detect circuitry is enabled and a mismatch to the expected value happened. The value is only meaningful, if BERRIF = 1. 0 A low input was sampled, when a high was expected 1 A high input reassembled, when a low was expected
1 BERRIF	**Bit Error Interrupt Flag** — BERRIF is asserted, when the bit error detect circuitry is enabled and if the value sampled at the RXD input does not match the transmitted value. If the BERRIE interrupt enable bit is set an interrupt will be generated. The BERRIF bit is cleared by writing a “1” to it. 0 No mismatch detected 1 A mismatch has occurred
0 BKDIF	**Break Detect Interrupt Flag** — BKDIF is asserted, if the break detect circuitry is enabled and a break signal is received. If the BKDIE interrupt enable bit is set an interrupt will be generated. The BKDIF bit is cleared by writing a “1” to it. 0 No break signal was received 1 A break signal was received

Chapter 16
Inter-Integrated Circuit (IICV3) Block Description

Table 16-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	28 Jul 2006	16.7.1.7/16-525	- Update flow-chart of interrupt routine for 10-bit address
V01.04	17 Nov 2006	16.3.1.2/16-505	- Revise Table1-5
V01.05	14 Aug 2007	16.3.1.1/16-505	- Backward compatible for IBAD bit name

16.1 Introduction

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

16.1.1 Features

The IIC module has the following key features:

- Compatible with I2C bus standard
- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation

18.4 Functional Description

18.4.1 General

This section provides a complete functional description of the MSCAN.

18.4.2 Message Storage

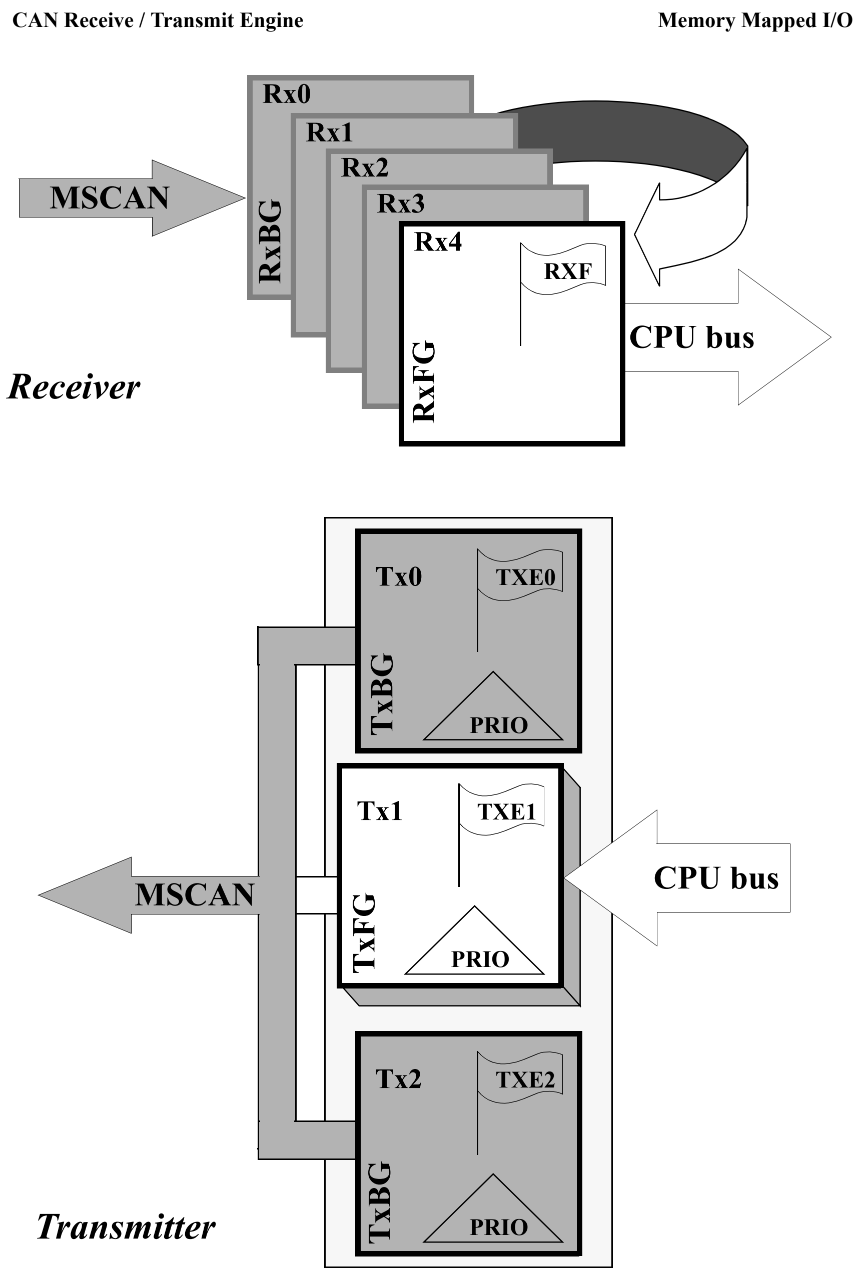


Figure 18-39. User Model for Message Buffer Organization

Field	Description
1 TC	**SENTTX Transmission Complete Flag** — If set, this bit indicates the current transmission has completed. It is set after the CRC nibble has been sent. Write a one to this bit to clear. 1 - Transmission has completed 0 - Transmission has not completed
0 TBE	**SENTTX Transmit-Buffer Empty Flag** — If set, this bit indicates the transmit-buffer is empty and can be written to. It is set by transferring the data from the transmit buffer to the transmit register. Write a one to this bit to clear. Clearing this bit declares the transmit buffer as full. 1 - Transmit-Buffer is empty 0 - Transmit-Buffer is full

21.7.2.6 SENT Transmit Buffer (TXBUF)

Module Base + 0x0008 — Access: User read/write[1]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	STATCONF[3:0]				CRC[3:0]				DATA0[3:0]				DATA1[3:0]			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Module Base + 0x000A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	DATA2[3:0]				DATA3[3:0]				DATA4[3:0]				DATA5[3:0]			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1 Read: Anytime.
Write: Anytime. While the Transmit-Buffer Empty bit in the INTFLG register is zero (INTFLG[TBE]=0) the data in the transmit buffer (TXBUF) should not be changed to avoid transmission of inconsistent data.

Table 21-9. SENT Transmit Buffer (TXBUF) Field Descriptions

Field	Description
31–28 STATCONF [3:0]	**SENTTX Status and Configuration Nibble** — These bits represent data which is sent as the SENT protocol status- and configuration-nibble.
27–24 CRC[3:0]	**SENTTX CRC Nibble** — These bits represent data which is sent as the SENT protocol CRC nibble, if the CRC bypass option bit in the SENTTX CONFIG register (CONFIG[CRCBYP]) is set. Otherwise these bits are ignored.
23–20 DATA0[3:0]	**SENTTX Data Nibble 0** — These bits represent data which is sent as the first SENT protocol data nibble.
19–16 DATA1[3:0]	**SENTTX Data Nibble 1** — These bits represent data which is sent as the second SENT protocol data nibble, if enabled by the data nibble count bits in the SENTTX CONFIG register (CONFIG[DNIBBLECOUNT]>=2).
15–12 DATA2[3:0]	**SENTTX Data Nibble 2** — These bits represent data which is sent as the third SENT protocol data nibble, if enabled by the data nibble count bits in the SENTTX CONFIG register (CONFIG[DNIBBLECOUNT]>=3).
11–8 DATA3[3:0]	**SENTTX Data Nibble 3** — These bits represent data which is sent as the fourth SENT protocol data nibble, if enabled by the data nibble count bits in the SENTTX CONFIG register (CONFIG[DNIBBLECOUNT]>=4).

Appendix J
DAC8B5V Electrical Specifications

Table J-1. Static Electrical Characteristics - DAC8B5V

Characteristics noted under conditions 4.75V <= VDDA <= 5.25V>, -40°C < T_j < 175°C , VRH=VDDA, VRL=VSSA unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Num	Ratings	Symbol	Min	Typ	Max	Unit
1	Supply Current of DAC8B5V buffer disabled buffer enabled FVR=0 DRIVE=1 buffer enabled FVR=1 DRIVE=0	I_{buf}	- - -	- 365 215	5 800 800	µA
2	Reference current (–40°C <T_J< +150°C) reference disabled reference enabled	I_{ref}	-	- 50	1 150	µA
3	Resolution		8			bit
4	Relative Accuracy measured at AMP	INL	-0.5		+0.5	LSB
5	Differential Nonlinearity measured at AMP	DNL	-0.5		+0.5	LSB
6	Relative Accuracy measured at AMP 150°C < T_j < 175°C	INL	-0.75		+0.75	LSB
7	Differential Nonlinearity measured at AMP 150°C < T_j < 175°C	DNL	-0.75		+0.75	LSB
8	DAC Range A (FVR bit = 1)	V_{out}	0...255/256(VRH-VRL)+VRL			V
9	DAC Range B (FVR bit = 0)	V_{out}	32...287/320(VRH-VRL)+VRL			V
10	Output Voltage unbuffered range A or B (load >= 50MΩ)	V_{out}	full DAC Range A or B			V
11	Output Voltage (DRIVE bit = 0) *) buffered range A (load >= 100KΩ to VSSA) buffered range A (load >= 100KΩ to VDDA)	V_{out}	0 0.15	- -	VDDA-0.15 VDDA	V
	buffered range B (load >= 100KΩ to VSSA) buffered range B (load >= 100KΩ to VDDA)		full DAC Range B			
12	Output Voltage (DRIVE bit = 1) **) buffered range B with 6.4KΩ load into resistor divider of 800Ω /6.56KΩ between VDDA and VSSA. (equivalent load is >= 65KΩ to VSSA) or (equivalent load is >= 7.5KΩ to VDDA)	V_{out}	full DAC Range B			V

Appendix L
Package Information

Figure L-1. 64 LQFP Exposed Pad Package