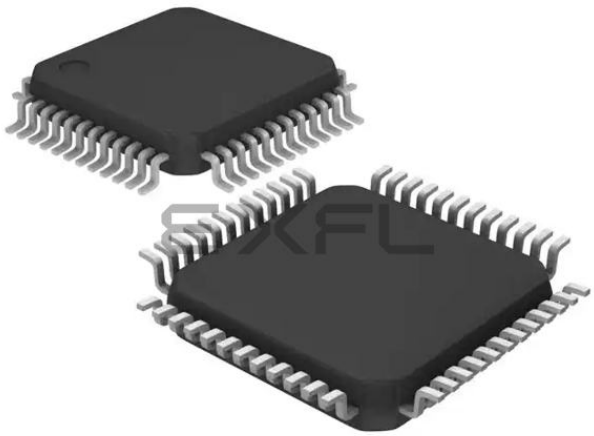

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
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Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc19f0vlf

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Supply Voltage Sensor - (BATSV3)

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1.6 Family Memory Map

Table 1-2.shows the MC9S12ZVC-Family register memory map.

Table 1-2. Device Register Memory Map

Address	Module	Size (Bytes)
0x0000–0x0003	ID Register	4
0x0004–0x000F	Reserved	12
0x0010–0x001F	INT	16
0x0020–0x006F	Reserved	80
0x0070–0x008F	MMC	32
0x0090–0x00FF	MMC Reserved	112
0x0100–0x017F	DBG	128
0x0180–0x01FF	Reserved	128
0x0200–0x037F	PIM	380
0x0380–0x039F	FTMRZ	32
0x03A0–0x03BF	Reserved	32
0x03C0–0x03CF	RAM ECC	16
0x03D0–0x03FF	Reserved	48
0x0400–0x042F	TIM1	48
0x0430–0x047F	Reserved	48
0x0480–0x04AF	PWM0	48
0x04B0–0x04FF	Reserved	80
0x0500–0x052F	PWM1	48
0x0530–0x05BF	Reserved	144
0x05C0–0x05EF	TIM0	48
0x05F0–0x05FF	Reserved	16
0x0600–0x063F	ADC0	64
0x0640–0x067F	Reserved	64
0x0680–0x0687	DAC	8
0x0688–0x068F	Reserved	128
0x0690–0x0697	ACMP0	8
0x0698–0x069F	ACMP1	8
0x06A0–0x06BF	Reserved	32
0x06C0–0x06DF	CPMU	32
0x06E0–0x06EF	Reserved	16
0x06F0–0x06F7	BATS	8
0x06F8–0x06FF	Reserved	8
0x0700–0x0707	SCI0	8
0x0708–0x070F	Reserved	8
0x0710–0x0717	SCI1	8

The POR circuit monitors the VDD and VDDA domains, ensuring a reset assertion until an adequate voltage level is attained. The LVR circuit monitors the VDD, VDDF and VDDX domains, generating a reset when the voltage in any of these domains drops below the specified assert level. The VDDX LVR monitor is disabled when the VREG is in reduced power mode. A low voltage interrupt circuit monitors the VDDA domain.

Table 2-33. Bit Indices of Implemented Register Bits per Port

	Port Data Register	Port Input Register	Data Direction Register	Pull Device Enable Register	Polarity Select Register	Port Interrupt Enable Register	Port Interrupt Flag Register	Digital Input Enable Register	Reduced Drive Register	Wired-Or Mode Register
Port	**PT**	**PTI**	**DDR**	**PER**	**PPS**	**PIE**	**PIF**	**DIE**	**RDR**	**WOM**
E	1-0	1-0	1-0	1-0	1-0	-	-	-	-	-
ADH	7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
ADL	7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
T	7-0	7-0	7-0	7-0	7-0	-	-	-	-	-
S	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-	7-0
P	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	6-4,2,0	-
J	1-0	1-0	1-0	1-0	1-0	-	-	-	-	1-0
L	-	1-0	-	-	1-0	1-0	1-0	1-0	-	-

Table 2-34 shows the effect of enabled peripheral features on I/O state and enabled pull devices.

Table 2-34. Effect of Enabled Features

Enabled Feature[1]	Related Signal(s)	Effect on I/O state	Effect on enabled pull device
CPMU OSC	EXTAL, XTAL	CPMU takes control	Forced off
TIMx output compare y	IOCx_y	Forced output	Forced off, pulldown forced off if open-drain
TIMx input capture y	IOCx_y	None[2]	None[3]
SPIx	MISOx, MOSx, SCKx, $\overline{\text{SSx}}$	SPI takes control	Forced off if output, pulldown forced off if open-drain
SCIx transmitter	TXDx	Forced output	Forced off, pulldown forced off if open-drain
SCIx receiver	RXDx	Forced input	None[3]
IICx	SDAx, SCLx	Forced open-drain	Pulldown forced off
S12ZDBG	DBGEEV	None[2]	None[3]
PWMx channel y	PWMx_y	Forced output	Forced off
ADCx	ANy	None[2 4]	None[3]
	VRH		
ACMPx	ACMPx_0, ACMPx_1	None[2 4]	None[3]
	ACMPOx	Forced output	Forced off
DACx	AMPPx, AMPMx	None[2 4]	None[3]
	DACUx, AMPx	Digital output forced off	Forced off

Read: Anytime.

Write: Never

DBGEFR contains flag bits each mapped to events whilst armed. Should an event occur, then the corresponding flag is set. With the exception of TRIGF, the bits can only be set when the ARM bit is set. The TRIGF bit is set if a TRIG event occurs when ARM is already set, or if the TRIG event occurs simultaneous to setting the ARM bit.All other flags can only be cleared by arming the DBG module. Thus the contents are retained after a debug session for evaluation purposes.

A set flag does not inhibit the setting of other flags.

Table 6-13. DBGEFR Field Descriptions

Field	Description
6 TRIGF	**TRIG Flag** — Indicates the occurrence of a TRIG event during the debug session. 0 No TRIG event 1 TRIG event
4 EEVF	**External Event Flag** — Indicates the occurrence of an external event during the debug session. 0 No external event 1 External event
3–0 ME[3:0]	**Match Event[3:0]**— Indicates a comparator match event on the corresponding comparator channel**.**

6.3.2.7 Debug Status Register (DBGSR)

Address: 0x010B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-10. Debug Status Register (DBGSR)

Read: Anytime.

Write: Never.

Table 6-14. DBGSR Field Descriptions

Field	Description
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate the current State Sequencer state. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal event, then the state sequencer returns to State0 and these bits are cleared to indicate that State0 was entered during the session. On arming the module the state sequencer enters State1 and these bits are forced to SSF[2:0] = 001. See Table 6-15**.**

Table 9-2. ADCCTL_0 Field Descriptions (continued)

Field	Description
11-10 ACC_CFG[1:0]	**ADCFLWCTL Register Access Configuration** — These bits define if the register ADCFLWCTL is controlled via internal interface only or data bus only or both. See Table 9-3. for more details.
9 STR_SEQA	**Control Of Conversion Result Storage and RSTAR_EIF flag setting at Sequence Abort or Restart Event** — This bit controls conversion result storage and RSTAR_EIF flag setting when a Sequence Abort Event or Restart Event occurs as follows: *If STR_SEQA = 1'b0 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is not stored and the respective conversion complete flag is not set • Restart Event only is issued before the last conversion of a CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware *If STR_SEQA = 1'b1 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is stored and the respective conversion complete flag is set and Intermediate Result Information Register is updated. • Restart Event only occurs during the last conversion of a CSL and no Sequence Abort Event is in process (SEQA clear) does not set the RSTA_EIF error flag • Restart Event only is issued before the CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware
8 MOD_CFG	**(Conversion Flow Control) Mode Configuration** — This bit defines the conversion flow control after a Restart Event and after execution of the "End Of List" command type: - Restart Mode - Trigger Mode (For more details please see also section Section 9.5.3.2, "Introduction of the Programmer's Model and following.) 0 "Restart Mode" selected. 1 "Trigger Mode" selected.

Table 9-3. ADCFLWCTL Register Access Configurations

ACC_CFG[1]	ACC_CFG[0]	ADCFLWCTL Access Mode
0	0	None of the access paths is enabled (default / reset configuration)
0	1	Single Access Mode - Internal Interface (ADCFLWCTL access via internal interface only)
1	0	Single Access Mode - Data Bus (ADCFLWCTL access via data bus only)
1	1	Dual Access Mode (ADCFLWCTL register access via internal interface and data bus)

NOTE

Each conversion flow control bit (SEQA, RSTA, TRIG, LDOK) must be controlled by software or internal interface according to the requirements described in Section 9.5.3.2.4, "The two conversion flow control Mode Configurations and overview summary in Table 9-10.

9.4.2.8 ADC Interrupt Enable Register (ADCIE)

Module Base + 0x0007

	7	6	5	4	3	2	1	0
R	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-11. ADC Interrupt Enable Register (ADCIE)

Read: Anytime

Write: Anytime

Table 9-12. ADCIE Field Descriptions

Field	Description
7 SEQAD_IE	**Conversion Sequence Abort Done Interrupt Enable Bit** — This bit enables the conversion sequence abort event done interrupt. 0 Conversion sequence abort event done interrupt disabled. 1 Conversion sequence abort event done interrupt enabled.
6 CONIF_OIE	**ADCCONIF Register Flags Overrun Interrupt Enable** — This bit enables the flag which indicates if an overrun situation occurred for one of the CON_IF[15:1] flags or for the EOL_IF flag. 0 No ADCCONIF Register Flag overrun occurred. 1 ADCCONIF Register Flag overrun occurred.

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 10-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 10-6. BATS Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
BATS Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

10.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0
$V_{measure} < V_{LBI1_A}$ (falling edge) or $V_{measure} < V_{LBI1_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
$V_{measure} < V_{LBI2_A}$ (falling edge) or $V_{measure} < V_{LBI2_D}$ (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2
$V_{measure} < V_{LBI3_A}$ (falling edge) or $V_{measure} < V_{LBI3_D}$ (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
$V_{measure} < V_{LBI4_A}$ (falling edge) or $V_{measure} < V_{LBI4_D}$ (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state . The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

10.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

11.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

By enabling the PRNT bit of the TSCR1 register, the performance of the timer can be enhanced. In this case, it is possible to set additional prescaler settings for the main timer counter in the present timer by using PTPSR[7:0] bits of PTPSR register generating divide by 1, 2, 3, 4,....20, 21, 22, 23,.....255, or 256.

11.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two Bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module or Pulse Accumulator must stay enabled (TEN bit of TSCR1 or PAEN bit of PACTL register must be set to one) while clearing CxF (writing one to CxF).

11.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x when available as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin if the corresponding OCPDx bit is set to zero. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests. Timer module or Pulse Accumulator must stay enabled (TEN bit of TSCR1 or PAEN bit of PACTL register must be set to one) while clearing CxF (writing one to CxF).

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx results in no output compare action on the output compare channel pin.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

A channel 7 event, which can be a counter overflow when TTOV[7] is set or a successful output compare on channel 7, overrides output compares on all other output compare channels. The output compare 7 mask register masks the bits in the output compare 7 data register. The timer counter reset enable bit, TCRE, enables channel 7 output compares to reset the timer counter. A channel 7 output compare can reset the timer counter even if the IOC7 pin is being used as the pulse accumulator input.

11.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

11.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

11.5 Resets

The reset state of each individual bit is listed within Section 11.3, “Memory Map and Register Definition” which details the registers and their bit fields

11.6 Interrupts

This section describes interrupts originated by the TIM16B8CV3 block. Table 11-25 lists the interrupts generated by the TIM16B8CV3 to communicate with the MCU.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0015 PWMPER1[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0016 PWMPER2[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0017 PWMPER3[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0018 PWMPER4[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0019 PWMPER5[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001A PWMPER6[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001B PWMPER7[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001C PWMDTY0[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001D PWMDTY1[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001E PWMDTY2[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x001F PWMDTY3[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0010 PWMDTY4[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0021 PWMDTY5[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0022 PWMDTY6[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0
0x0023 PWMDTY7[2]	R/W	Bit 7	6	5	4	3	2	1	Bit 0

= Unimplemented or Reserved

Figure 13-2. The scalable PWM Register Summary (Sheet 3 of 4)

14.4.6 Receiver

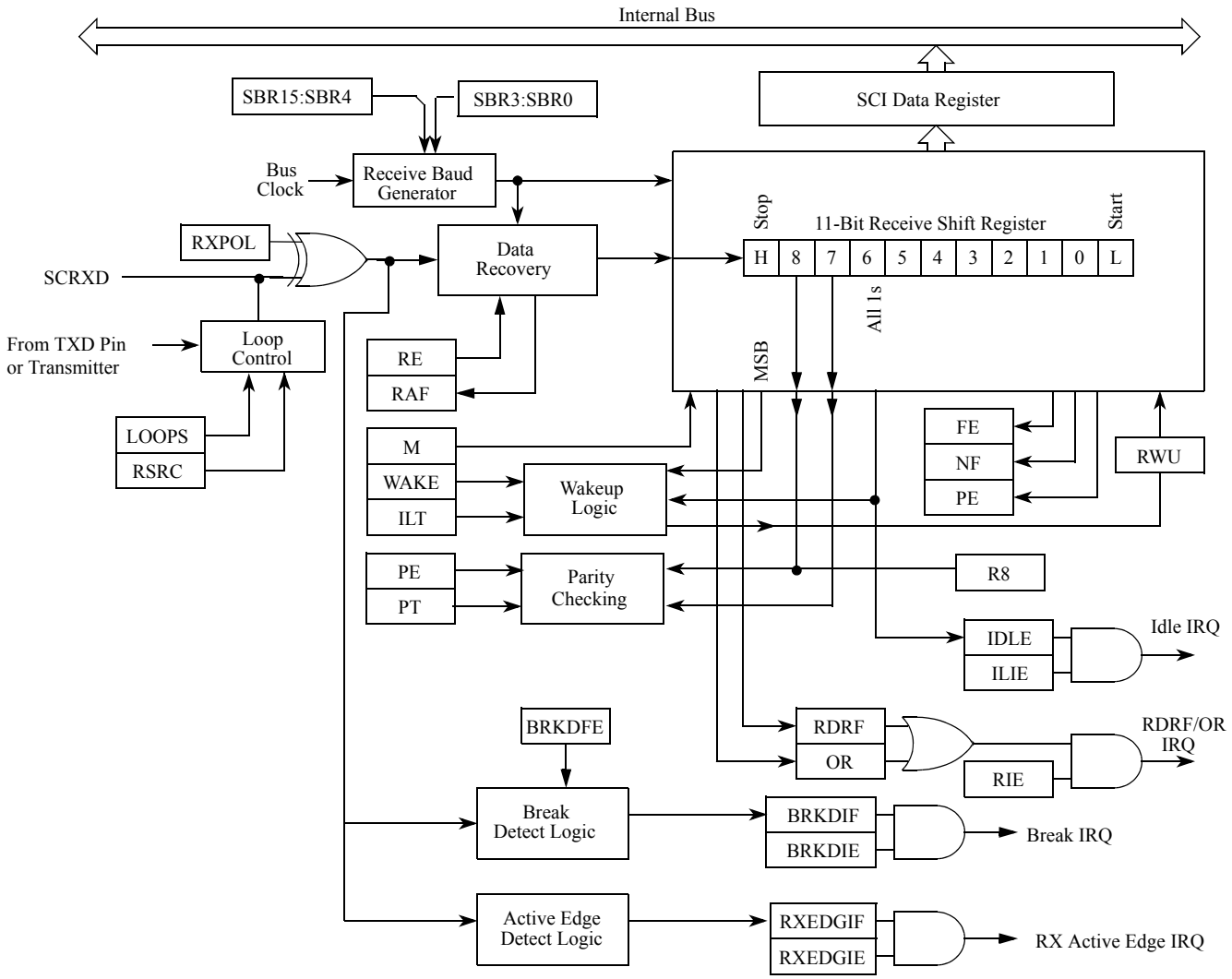


Figure 14-20. SCI Receiver Block Diagram

14.4.6.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

14.4.6.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

Figure 14-26 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

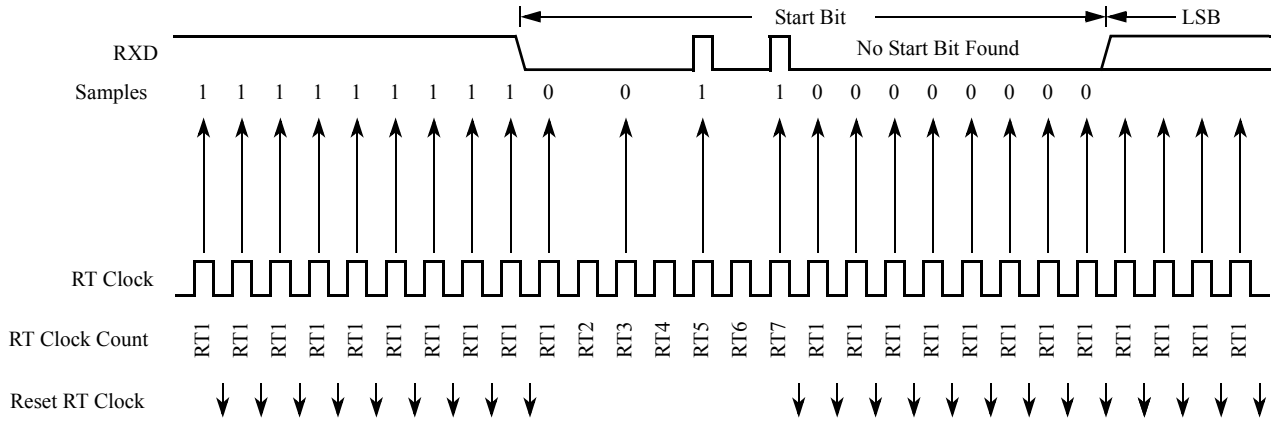


Figure 14-26. Start Bit Search Example 5

In Figure 14-27, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

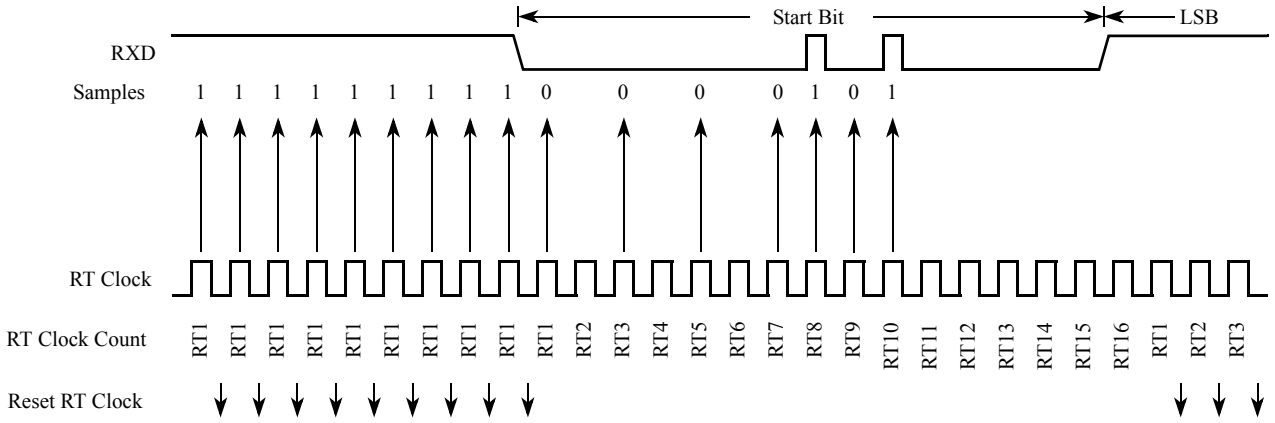


Figure 14-27. Start Bit Search Example 6

14.4.6.4 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming frame, it sets the framing error flag, FE, in SCI status register 1 (SCISR1). A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

- Acknowledge bit generation/detection
- Bus busy detection
- General Call Address detection
- Compliant to ten-bit address

16.3.1.1 IIC Address Register (IBAD)

Module Base +0x0000

	7	6	5	4	3	2	1	0
R W	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-3. IIC Bus Address Register (IBAD)

Read and write anytime

This register contains the address the IIC bus will respond to when addressed as a slave; note that it is not the address sent on the bus during the address transfer.

Table 16-2. IBAD Field Descriptions

Field	Description
7:1 ADR[7:1]	**Slave Address** — Bit 1 to bit 7 contain the specific slave address to be used by the IIC bus module.The default mode of IIC bus is slave mode for an address match on the bus.
0 Reserved	Reserved — Bit 0 of the IBAD is reserved for future compatibility. This bit will always read 0.

16.3.1.2 IIC Frequency Divider Register (IBFD)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-4. IIC Bus Frequency Divider Register (IBFD)

Read and write anytime

Table 16-3. IBFD Field Descriptions

Field	Description
7:0 IBC[7:0]	**I Bus Clock Rate 7:0** — This field is used to prescale the clock for bit rate selection. The bit clock generator is implemented as a prescale divider — IBC7:6, prescaled shift register — IBC5:3 select the prescaler divider and IBC2-0 select the shift register tap point. The IBC bits are decoded to give the tap and prescale values as shown in Table 16-4.

P-Flash memory (see Table 22-3) as indicated by reset condition F in Table 22-24.. To change the EEPROM protection that will be loaded during the reset sequence, the P-Flash sector containing the EEPROM protection byte must be unprotected, then the EEPROM protection byte must be programmed. If a double bit fault is detected while reading the P-Flash phrase containing the EEPROM protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the EEPROM memory fully protected.

Trying to alter data in any protected area in the EEPROM memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the EEPROM memory is not possible if any of the EEPROM sectors are protected.

Table 22-23. DFPROT Field Descriptions

Field	Description
7 DPOPEN	**EEPROM Protection Control** 0 Enables EEPROM memory protection from program and erase with protected address range defined by DPS bits 1 Disables EEPROM memory protection from program and erase
5–0 DPS[5:0]	**EEPROM Protection Size** — The DPS[5:0] bits determine the size of the protected area in the EEPROM memory, this size increase in step of 32 bytes, as shown in Table 22-24. .

Table 22-24. EEPROM Protection Address Range

DPS[5:0]	Global Address Range	Protected Size
000000	0x10_0000 – 0x10_001F	32 bytes
000001	0x10_0000 – 0x10_003F	64 bytes
000010	0x10_0000 – 0x10_005F	96 bytes
000011	0x10_0000 – 0x10_007F	128 bytes
000100	0x10_0000 – 0x10_009F	160 bytes
000101	0x10_0000 – 0x10_00BF	192 bytes
The Protection Size goes on enlarging in step of 32 bytes, for each DPS value increasing of one. . . .		
111111	0x10_0000 – 0x10_07FF	2,048 bytes

22.3.2.11 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

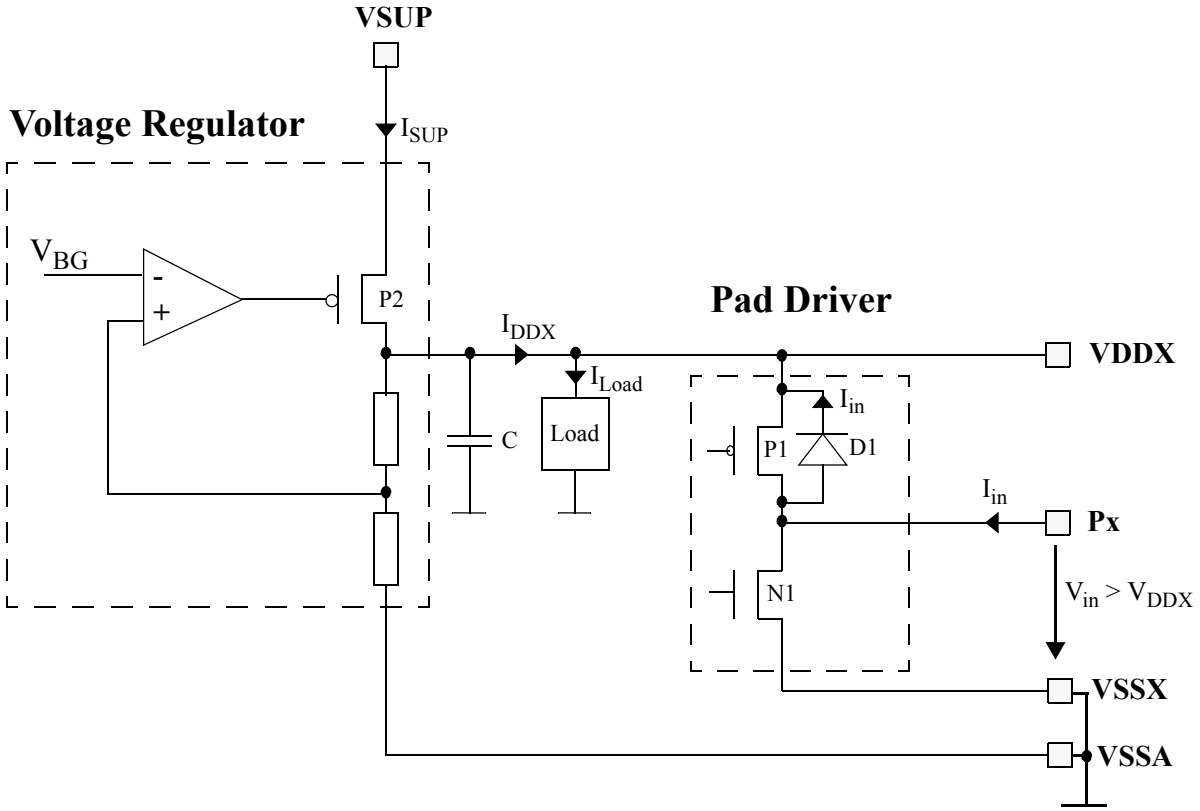
A.1.2.4 TEST

This pin is used for production testing only. The TEST pin must be tied to ground in all applications.

A.1.3 Current Injection

Power supply must maintain regulation within operating V_{DDX} or V_{DD} range during instantaneous and operating maximum current conditions. **Figure A-1.** shows a 5 V GPIO pad driver and the on chip voltage regulator with VDDX output. It shows also the power and ground pins VSUP, VDDX, VSSX and VSSA. Px represents any 5 V GPIO pin. Assume Px is configured as an input. The pad driver transistors P1 and N1 are switched off (high impedance). If the voltage V_{in} on Px is greater than V_{DDX} a positive injection current I_{in} will flow through diode D1 into VDDX node. If this injection current I_{in} is greater than I_{Load}, the internal power supply VDDX may go out of regulation. Ensure the external V_{DDX} load will shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Figure A-1. Current Injection on GPIO Port if $V_{in} > V_{DDX}$



A.1.4 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation outside these ranges is not guaranteed. Stress beyond these limits may affect the reliability or cause permanent damage of the device.

Appendix N
Detailed Register Address Map

Table N-1. Revision History Table

Revision Number	Revision Date	Sections Affected	Description Of Changes
0.01	22-Aug-2013		Initial version
0.02	25-Oct-2013		Added instance suffix to SENTTX register names

The following tables show the detailed register map of the MC9S12ZVC-Family.

NOTE

Smaller derivatives within the MC9S12ZVC-Family feature a subset of the listed modules.

N.1 0x0000–0x0003 Part ID

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PARTID0	R	0	0	0	0	0	0	0	0
		W								
0x0001	PARTID1	R	0	0	0	1	0	1	1	1
		W								
0x0002	PARTID2	R	0	0	0	0	0	0	0	0
		W								
0x0003	PARTID3	R	Revision Dependent							
		W								

N.2 0x0010–0x001F S12ZINT

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	IVBR	R	IVB_ADDR[15:8]							
		W								
0x0011		R	IVB_ADDR[7:1]							0
		W								
0x0016	INT_XGPRIO	R	0	0	0	0	0	XILVL[2:0]		
		W								
0x0017	INT_CFADDR	R	0	INT_CFADDR[6:3]				0	0	0
		W								
0x0018	INT_CFDATA0	R	RQST	0	0	0	0	PRIOLVL[2:0]		
		W								
0x0019	INT_CFDATA1	R	RQST	0	0	0	0	PRIOLVL[2:0]		
		W								