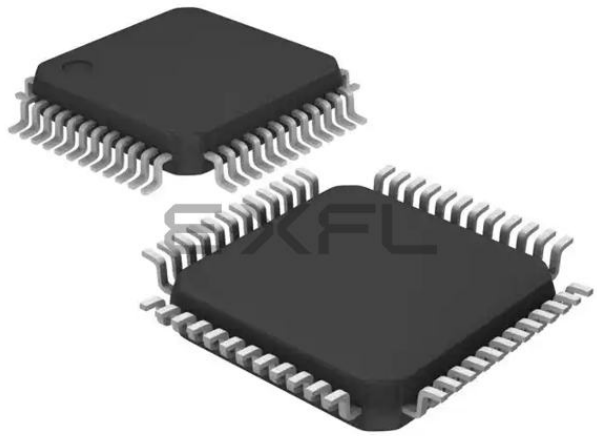

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
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The MC9S12ZVC family of microcontrollers is targeted at use in safety relevant systems and has been developed using an ISO26262 compliant development system under the NXP Safe Assure Program. For more details of the NXP Safe Assure program, refer to : NXP Safe Assure

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A full list of family members and options is included in device overview section.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the S12Z CPU. For S12ZCPU information please refer to the CPU S12Z Reference Manual.

Revision History

Date	Revision Level	Description
22-August-2016	Rev 1.6	Added item 18 and 19 Table E-1 Bandgap voltage and temperature dependency Changed item 5 Table H-2 ACMP input offset Added operating condition for C part to Table A-5
13-October-2016	Rev 1.7	Corrected Table 1-1 Two SCIs for 48pin packages. Corrected typo in table H-2 item 5
2-January-2018	Rev 1.8	Corrected Package Information for 64LQFP Exposed Pad
29-January-2018	Rev 1.9	Corrected Package Information for 64LQFP Exposed Pad
26-March-2018	Rev 2.0	Updated Appendix A MCU Electrical Specifications

1.14 Application Information

1.14.1 ADC Calibration

For applications that do not provide external ADC reference voltages, the VDDA/VSSA supplies can be used as sources for VRH/VRL respectively. Since the VDDA must be connected to VDDX at board level in the application, the accuracy of the VDDA reference is limited by the internal voltage regulator accuracy. In order to compensate for VDDA reference voltage variation in this case, the on chip bandgap reference voltage V_{BG} is measured during production test. V_{BG} has a narrow variation over temperature and external voltage supply. V_{BG} is connected to an internal channel of the ADC module (see Table 1-8). The12-bit left justified ADC conversion result of V_{BG} is stored in the flash IFR for reference, as listed in Table 1-16.

By measuring the voltage V_{BG} in the application environment and comparing the result to the reference value in the IFR, it is possible to determine the current ADC reference voltage V_{RH}:

$$V_{RH} = \frac{StoredReference}{ConvertedReference} \bullet 5V$$

The exact absolute value of an analog conversion can be determined as follows:

$$Result = ConvertedADInput \bullet \frac{StoredReference \bullet 5V}{ConvertedReference \bullet 2^{n}}$$

With:

Converted AD Input:	Result of the analog to digital conversion of the desired pin
Converted Reference:	Result of internal channel conversion
Stored Reference:	Value in IFR location
n:	ADC resolution (12 bit)

NOTE

The ADC reference voltage V_{RH} must remain at a constant level throughout the conversion process.

The reference voltage V_{BG} is measured under the conditions shown in Table 1-17. The value stored in the IFR is the average of 8 consecutive conversions.

Table 2-19. Reduced Drive Register Field Descriptions

Field	Description
7-0 RDRx7-0	**Reduced Drive Register** — Select reduced drive for output pin This bit configures the drive strength of the associated output pin as either full or reduced. If a pin is used as input this bit has no effect. The reduced drive function is independent of which function is being used on a particular pin. 1 Reduced drive selected (approx. 1/10 of the full drive strength) 0 Full drive strength enabled

2.3.3.10 Wired-Or Mode Register

Address 0x02DF WOMS
0x031F WOMJ

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	WOMx7	WOMx6	WOMx5	WOMx4	WOMx3	WOMx2	WOMx1	WOMx0
Reset	0	0	0	0	0	0	0	0

Figure 2-19. Wired-Or Mode Register

[1] Read: Anytime
Write: Anytime

This is a generic description of the standard wired-or registers. Refer to Table 2-33 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-20. Wired-Or Mode Register Field Descriptions

Field	Description
7-0 WOMx7-0	**Wired-Or Mode** — Enable open-drain output This bit configures the output buffer as wired-or. If enabled the output is driven active low only (open-drain) while the active high drive is turned off. This allows a multipoint connection of several serial modules. These bits have no influence on pins used as inputs. 1 Output buffers operate as open-drain outputs 0 Output buffers operate as push-pull outputs

2.3.3.11 PIM Reserved Register

Address (any reserved)

Access: User read[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-20. PIM Reserved Register

[1] Read: Always reads 0x00
Write: Unimplemented

2.3.4 PIM Generic Register Exceptions

This section lists registers with deviations from the generic description in one or more register bits.

2.3.4.1 Port P Over-Current Protection Enable Register (OCPEP)

Address 0x02F9 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	OCPEP6	OCPEP5	OCPEP4	0	OCPEP2	0	OCPEP0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-21. Over-Current Protection Enable Register (OCPEP)

[1] Read: Anytime
Write:Anytime

Table 2-21. OCPEP Register Field Descriptions

Field	Description
6 OCPEP6	**Over-Current Protection Enable** — Activate over-current detector on PP6 Refer to Section ”2.5.4, “Over-Current Protection on PP[6-4,0]”” 1 PP6 over-current detector enabled 0 PP6 over-current detector disabled
5 OCPEP5	**Over-Current Protection Enable** — Activate over-current detector on PP5 Refer to Section 2.5.4, “Over-Current Protection on PP[6-4,0]”” 1 PP5 over-current detector enabled 0 PP5 over-current detector disabled
4 OCPEP4	**Over-Current Protection Enable** — Activate over-current detector on PP4 Refer to Section 2.5.4, “Over-Current Protection on PP[6-4,0]”” 1 PP4 over-current detector enabled 0 PP4 over-current detector disabled
2 OCPEP2	**Over-Current Protection Enable** — Activate over-current detector on EVDD1 Refer to Section 2.5.3, “Over-Current Protection on PP2 (EVDD1)”” 1 EVDD1 over-current detector enabled 0 EVDD1 over-current detector disabled
0 OCPEP0	**Over-Current Protection Enable** — Activate over-current detector on PP0 Refer to Section 2.5.4, “Over-Current Protection on PP[6-4,0]”” 1 PP0 over-current detector enabled 0 PP0 over-current detector disabled

3.4.4.11 READ_MEM.sz, READ_MEM.sz_WS

READ_MEM.sz

Read memory at the specified address **Non-intrusive**

0x30	Address[23-0]		Data[7-0]
host → target	host → target	D A C K	target → host

0x34	Address[23-0]		Data[15-8]	Data[7-0]
host → target	host → target	D A C K	target → host	target → host

0x38	Address[23-0]		Data[31-24]	Data[23-16]	Data[15-8]	Data[7-0]
host → target	host → target	D A C K	target → host	target → host	target → host	target → host

READ_MEM.sz_WS

Read memory at the specified address with status **Non-intrusive**

0x31	Address[23-0]		BDCCSRL	Data[7-0]
host → target	host → target	D L Y	target → host	target → host

0x35	Address[23-0]		BDCCSRL	Data [15-8]	Data [7-0]
host → target	host → target	D L Y	target → host	target → host	target → host

0x39	Address[23-0]		BDCCSRL	Data[31-24]	Data[23-16]	Data [15-8]	Data [7-0]
host → target	host → target	D L Y	target → host	target → host	target → host	target → host	target → host

Read data at the specified memory address. The address is transmitted as three 8-bit packets (msb to lsb) immediately after the command.

The hardware forces low-order address bits to zero longword accesses to ensure these accesses are on 0-modulo-size alignments. Byte alignment details are described in Section 3.4.5.2, “BDC Access Of Device Memory Mapped Resources”. If the with-status option is specified, the BDCCSR status byte is returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted.

The examples show the READ_MEM.B{_WS}, READ_MEM.W{_WS} and READ_MEM.L{_WS} commands.

if the contents of the addressed bytes match because all 32-bits must match. In Table 6-29 the Access Address column refers to the address bits[1:0] of the lowest accessed address (most significant data byte).

Table 6-29. Data Register Use Dependency On CPU Access Type

			Memory Address[2:0]						
Case	**Access Address**	**Access Size**	**000**	**001**	**010**	**011**	**100**	**101**	**110**
1	00	32-bit	DBGxD0	DBGxD1	DBGxD2	DBGxD3			
2	01	32-bit		DBGxD1	DBGxD2	DBGxD3	DBGxD0		
3	10	32-bit			DBGxD2	DBGxD3	DBGxD0	DBGxD1	
4	11	32-bit				DBGxD3	DBGxD0	DBGxD1	DBGxD2
5	00	16-bit	DBGxD0	DBGxD1					
6	01	16-bit		DBGxD1	DBGxD2				
7	10	16-bit			DBGxD2	DBGxD3			
8	11	16-bit				DBGxD3	DBGxD0		
9	00	8-bit	DBGxD0						
10	01	8-bit		DBGxD1					
11	10	8-bit			DBGxD2				
12	11	8-bit				DBGxD3			
13	00	8-bit					DBGxD0		
				Denotes byte that is not accessed.					

For a match of a 32-bit access with data compare, the address comparator must be loaded with the address of the lowest accessed byte. For Case1 Table 6-29 this corresponds to 000, for Case2 it corresponds to 001. To compare all 32-bits, it is required that no bits are masked.

6.4.2.3 Data Bus Comparison NDB Dependency

The NDB control bit allows data bus comparators to be configured to either match on equivalence or on difference. This allows monitoring of a difference in the contents of an address location from an expected value.

When matching on an equivalence (NDB=0), each individual data bus bit position can be masked out by clearing the corresponding mask bit, so that it is ignored in the comparison. A match occurs when all data bus bits with corresponding mask bits set are equivalent. If all mask register bits are clear, then a match is based on the address bus only, the data bus is ignored.

When matching on a difference, mask bits can be cleared to ignore bit positions. A match occurs when any data bus bit with corresponding mask bit set is different. Clearing all mask bits, causes all bits to be ignored and prevents a match because no difference can be detected. In this case address bus equivalence does not cause a match. Bytes that are not accessed are ignored. Thus when monitoring a multi byte field for a difference, partial accesses of the field only return a match if a difference is detected in the accessed bytes.

Chapter 7
ECC Generation Module (SRAM_ECCV1)

7.1 Introduction

The purpose of ECC logic is to detect and correct as much as possible memory data bit errors. These soft errors, mainly generated by alpha radiation, can occur randomly during operation. "Soft error" means that only the information inside the memory cell is corrupt; the memory cell itself is not damaged. A write access with correct data solves the issue. If the ECC algorithm is able to correct the data, then the system can use this corrected data without any issues. If the ECC algorithm is able to detect, but not correct the error, then the system is able to ignore the memory read data to avoid system malfunction.

The ECC value is calculated based on an aligned 2 byte memory data word. The ECC algorithm is able to detect and correct single bit ECC errors. Double bit ECC errors will be detected but the system is not able to correct these errors. This kind of ECC code is called SECDED code. This ECC code requires 6 additional parity bits for each 2 byte data word.

7.1.1 Features

The SRAM_ECC module provides the ECC logic for the system memory based on a SECDED algorithm. The SRAM_ECC module includes the following features:

- SECDED ECC code
  - Single bit error detection and correction per 2 byte data word
  - Double bit error detection per 2 byte data word
- Memory initialization function
- Byte wide system memory write access
- Automatic single bit ECC error correction for read and write accesses
- Debug logic to read and write raw use data and ECC values

7.2 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the SRAM_ECC module.

7.2.1 Register Summary

Figure 7-1 shows the summary of all implemented registers inside the SRAM_ECC module.

Mode. For this COP configuration (ACLK clock source, CSAD set) a latency time occurs when entering or exiting (Full, Pseudo) Stop Mode. When bit CSAD is clear the ACLK clock source is on for the COP during Full Stop Mode and COP is operating.
During Full Stop Mode the RTI counter halts.
After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). The COP runs on ACLK and RTI is running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).

- **Pseudo Stop Mode (PSTP = 1 and OSCE=1)**
  External oscillator (XOSCLCP) continues to run.
  - If COPOSCSEL1=0:
    If the respective enable bits are set (PCE=1 and PRE=1) the COP and RTI will continue to run with a clock derived from the oscillator clock.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.
  - If COPOSCSEL1=1:
    If the respective enable bit for the RTI is set (PRE=1) the RTI will continue to run with a clock derived from the oscillator clock.
    The clock for the COP is derived from ACLK (trimmable internal RC-Oscillator clock). During Pseudo Stop Mode the ACLK for the COP can be stopped (COP static) or running (COP active) depending on the setting of bit CSAD. When bit CSAD is set the ACLK for the COP is stopped during Pseudo Stop Mode and COP continues to operate after exit from Pseudo Stop Mode.
    For this COP configuration (ACLK clock source, CSAD set) a latency time occurs when entering or exiting (Pseudo, Full) Stop Mode. When bit CSAD is clear the ACLK clock source is on for the COP during Pseudo Stop Mode and COP is operating.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.

NOTE

When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.

8.1.2.4 Freeze Mode (BDM active)

For S12CPMU_UHV_V7 Freeze Mode is the same as Run Mode except for RTI and COP which can be frozen in Active BDM Mode with the RSBCK bit in the CPMUCOP register. After exiting BDM Mode RTI and COP will resume its operations starting from this frozen status.

Additionally the COP can be forced to the maximum time-out period in Active BDM Mode. For details please see also the RSBCK and CR[2:0] bit description field of Table 8-13 in Section 8.3.2.10, “S12CPMU_UHV_V7 COP Control Register (CPMUCOP)

8.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the S12CPMU_UHV_V7.

8.3.1 Module Memory Map

The S12CPMU_UHV_V7 registers are shown in Figure 8-3.

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	CPMU RESERVED00	R	0	0	0	0	0	0	0	0
		W								
0x0001	CPMU RESERVED01	R	0	0	0	0	0	0	0	0
		W								
0x0002	CPMU RESERVED02	R	0	0	0	0	0	0	0	0
		W								
0x0003	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x0004	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0005	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0006	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0007	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x0008	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0009	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x000A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x000B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x000C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x000D	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x000E	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
			= Unimplemented or Reserved							

Figure 8-3. CPMU Register Summary

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0010	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x0011	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x0012	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x0013	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x0014	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x0015	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x0016	RESERVED CPMUTEST3	R	0	0	0	0	0	0	0	0
		W								
0x0017	CPMUHTTR	R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
		W								
0x0018	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x0019	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x001A	CPMUOSC	R	OSCE	0	Reserved	0	0	0	0	0
		W								
0x001B	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x001C	RESERVED CPMUTEST2	R	0	0	0	0	0	0	0	0
		W								
0x001D	CPMU VREGCTL	R	0	0	0	0	0	EXTCON	EXTXON	INTXON
		W								
0x001E	CPMUOSC2	R	0	0	0	0	0	0	OMRE	OSCMOD
		W								
0x001F	CPMU RESERVED1F	R	0	0	0	0	0	0	0	0
		W								

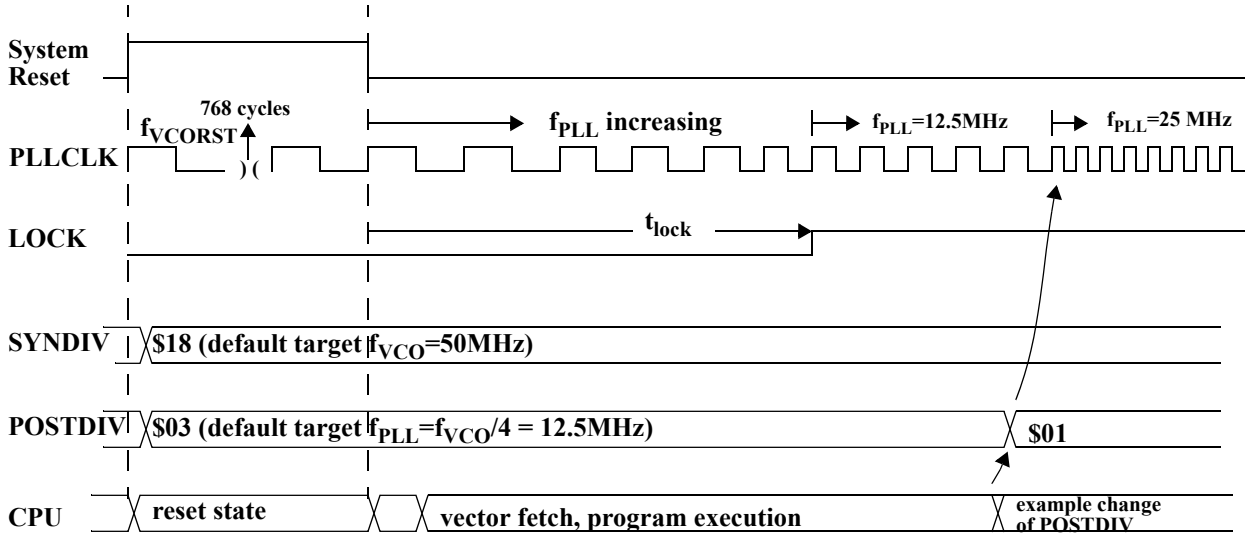
= Unimplemented or Reserved

Figure 8-3. CPMU Register Summary

8.4.2 Startup from Reset

An example for startup of the clock system from Reset is given in Figure 8-36.

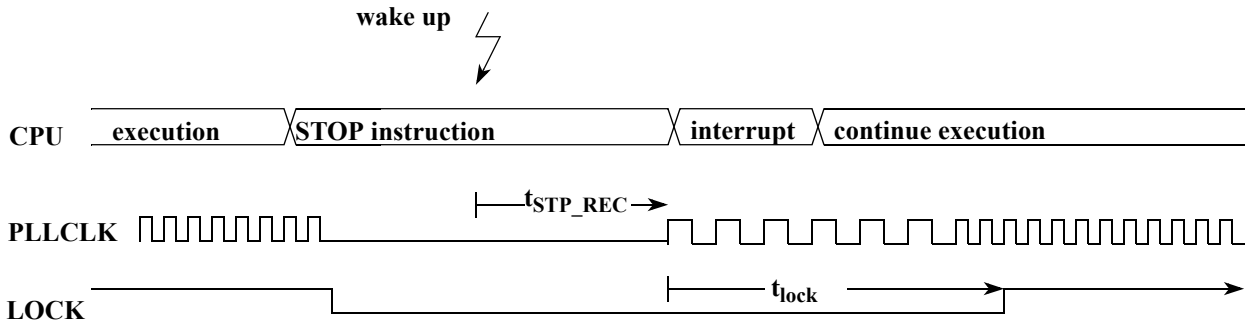
Figure 8-36. Startup of clock system after Reset



8.4.3 Stop Mode using PLLCLK as source of the Bus Clock

An example of what happens going into Stop Mode and exiting Stop Mode after an interrupt is shown in Figure 8-37. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop Mode.

Figure 8-37. Stop Mode using PLLCLK as source of the Bus Clock



Depending on the COP configuration there might be an additional significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time of 2 ACLK cycles occurs if COP clock source is ACLK and the CSAD bit is set and must be added to the device Stop Mode recovery time t_{STP_REC}. After exit from Stop Mode (Pseudo, Full) for this latency time

9.4.2.3 ADC Status Register (ADCSTS)

It is important to note that if flag DBECC_ERR is set the ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. An ADC Soft-Reset clears bits CSL_SEL and RVL_SEL.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
W								
Reset	0	0	0	0	1	0	0	0

= Unimplemented or Reserved

Figure 9-6. ADC Status Register (ADCSTS)

Read: Anytime

Write:

- Bits CSL_SEL and RVL_SEL anytime if bit ADC_EN is clear or bit SMOD_ACC is set
- Bits DBECC_ERR and READY not writable

Table 9-5. ADCSTS Field Descriptions

Field	Description
7 CSL_SEL	**Command Sequence List Select bit** — This bit controls and indicates which ADC Command List is active. This bit can only be written if ADC_EN bit is clear. This bit toggles in CSL double buffer mode when no conversion or conversion sequence is ongoing and bit LDOK is set and bit RSTA is set. In CSL single buffer mode this bit is forced to 1'b0 by bit CSL_BMOD. 0 ADC Command List 0 is active. 1 ADC Command List 1 is active.
6 RVL_SEL	**Result Value List Select Bit** — This bit controls and indicates which ADC Result List is active. This bit can only be written if bit ADC_EN is clear. After storage of the initial Result Value List this bit toggles in RVL double buffer mode whenever the conversion result of the first conversion of the current CSL is stored or a CSL got aborted. In RVL single buffer mode this bit is forced to 1'b0 by bit RVL_BMOD. Please see also Section 9.2.1.2, "MCU Operating Modes for information regarding Result List usage in case of Stop or Wait Mode. 0 ADC Result List 0 is active. 1 ADC Result List 1 is active.
5 DBECC_ERR	**Double Bit ECC Error Flag** — This flag indicates that a double bit ECC error occurred during conversion command load or result storage and ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. This bit is cleared if bit ADC_EN is clear. 0 No double bit ECC error occurred. 1 A double bit ECC error occurred.
3 READY	**Ready For Restart Event Flag** — This flag indicates that ADC is in its idle state and ready for a Restart Event. It can be used to verify after exit from Wait Mode if a Restart Event can be issued and processed immediately without any latency time due to an ongoing Sequence Abort Event after exit from MCU Wait Mode (see also the Note in Section 9.2.1.2, "MCU Operating Modes). 0 ADC not in idle state. 1 ADC is in idle state.

15.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 15-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 15-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 15-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 15-10).

[1] Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 18-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

18.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 18.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

21.7.2.3 SENT Transmitter Configuration Register (CONFIG)

Module Base + 0x0004 Access: User read/write[1]

	15	14	13	12	11	10	9	8
R	TXINIT	TXEN	0	0	0	DNIBBLECOUNT[2:0]		
W								
Reset	1	0	0	0	0	0	0	1

	7	6	5	4	3	2	1	0
R	0	0	0	OPTEDGE	SINGLE	CRCSCN	CRCLEG	CRCBYP
W								
Reset	0	0	0	0	0	0	0	0

[1] Read: Anytime.
Write: TXINIT bit: Anytime. All other bits: Anytime, if TXINIT is one.

Table 21-6. SENT Transmitter Configuration Register (CONFIG) Field Descriptions

Field	Description
15 TXINIT	**SENTTX Initialization Enable** — If this bit is set, sending SENT messages is aborted and other configuration bits can be written. Setting this bit immediately aborts any ongoing transmission, resets interrupt flags INTFLG[PPRE,CS,TC,TBE] to their respective reset state and the SENTTX pin returns to idle level. Interrupt flags can only be cleared, if this bit is zero and CONFIG[TXEN] is one. 1 - Writing configuration bits is enabled. Data transmission is disabled. 0 - Writing configuration bits is disabled. Data transmission is enabled.
14 TXEN	**SENTTX Pin Enable** — This bit enables the SENTTX module function on the SENTTX output pin. This bit can only be changed if the CONFIG[TXINIT] bit is one. 1 - Output pin is controlled by the SENTTX module 0 - Output pin is not controlled by the SENTTX module
10–8 DNIBBLE-COUNT[2:0]	**SENTTX Data Nibble Count** — These bits represent the number of data nibbles to be transmitted. These bits can only be changed if the CONFIG[TXINIT] bit is one. Available range for the number of data nibbles in a SENT message is 1 to 6, encoded in the CONFIG[DNIBBLECOUNT] bits as follows: 000 - Reserved 001 - One data nibble is transmitted 010 - Two data nibbles are transmitted 011 - Three data nibbles are transmitted 100 - Four data nibbles are transmitted 101 - Five data nibbles are transmitted 110 - Six data nibbles are transmitted 111 - Reserved
4 OPTEDGE	**SENTTX Optimized Rising Edge Position** — If set, this bit causes the SENTTX module to place the rising edge at half the number of the pulse period ticks after the falling edge to yield a duty cycle of about 50%. If the pulse period is an odd number of ticks, the number of ticks for the low pulse is rounded down (meaning the low pulse is one tick shorter than the high pulse). Otherwise, if this bit is cleared, a rising edge is positioned 5 ticks (UT) after a falling edge. This bit can only be changed if the CONFIG[TXINIT] bit is one. 1 - Optimized positioning of rising edges enabled 0 - Rising edges are generated 5 UT ticks after falling-edges

Appendix E
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

E.1 VREG Electrical Specifications

Table E-1. Voltage Regulator Electrical Characteristics (Junction Temperature From –40°C To +175°C)

VDDA and VDDX must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1	Input Voltages	V_{SUP}	3.5	—	40	V
2	Output Voltage VDDX (with external PNP) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop mode) V_{SUP} > =3.5V	V_{DDX}	 4.85 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.15 5.15 5.15 5.75	 V V V V
3	Output Voltage VDDX (without external PNP) Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop mode) V_{SUP} > =3.5V	V_{DDX}	 4.80 4.50 3.13 2.5	 4.95 4.95 — 5.5	 5.10 5.10 5.10 5.70	 V V V V
4	Load Current VDDX[1] (without external PNP) (-40°C < T_J < 150°C) Full Performance Mode V_{SUP} > 6V Full Performance Mode 3.5V <= V_{SUP} <=6V	I_{DDX}	 0 0	 — —	 70 25	mA
5	Load Current VDDX(1) (without external PNP) Full Performance Mode V_{SUP} > 6V Full Performance Mode 3.5V <= V_{SUP} <=6V Reduced Performance Mode (stop mode)	I_{DDX}	 0 0 0	 — — —	 55 20 5	 mA mA mA
6	Short circuit VDDX fall back current V_{DDX}<=0.5V	I_{DDX}	—	100	—	mA
7	Output Voltage VDDC with external PNP Full Performance Mode V_{SUP} > =6V Full Performance Mode 5.5V <= V_{SUP} <=6V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stop mode) V_{SUP} > =3.5V	V_{DDC}	 4.85 4.50 3.13 2.5	 5.0 5.0 — 5.5	 5.15 5.15 5.15 5.75	 V V V V
8	Load Current VDDC Reduced Performance Mode (stop mode)	I_{DDC}	 0	 —	 2.5	 mA
9	Low Voltage Interrupt Assert Level[2] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V V
10a	VDDX Low Voltage Reset deassert[3]	V_{LVRXD}	—	3.05	3.13	V
10b	VDDX Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V

Table E-3. OSC electrical characteristics (Junction Temperature From –40°C To +175°C)

Num	Rating	Symbol	Min	Typ	Max	Unit
1	Nominal crystal or resonator frequency	f_{OSC}	4.0	—	20	MHz
2	Startup Current	i_{OSC}	100	—	—	µA
3a	Oscillator start-up time (4MHz)[1]	t_{UPOSC}	—	2	10	ms
3b	Oscillator start-up time (8MHz)[1]	t_{UPOSC}	—	1.6	8	ms
3c	Oscillator start-up time (16MHz)[1]	t_{UPOSC}	—	1	5	ms
3d	Oscillator start-up time (20MHz)[1]	t_{UPOSC}	—	1	4	ms
4	Clock Monitor Failure Assert Frequency	f_{CMFA}	200	450	1200	KHz
5	Input Capacitance (EXTAL, XTAL pins)	C_{IN}	—	7	—	pF
6	EXTAL Pin Input Hysteresis	$V_{HYS,EXTAL}$	—	120	—	mV
7	EXTAL Pin oscillation amplitude (loop controlled Pierce)	$V_{PP,EXTAL}$	—	1	—	V
8	EXTAL Pin oscillation required amplitude[2]	$V_{PP,EXTAL}$	0.8	—	1.5	V

1 These values apply for carefully designed PCB layouts with capacitors that match the crystal/resonator requirements.

2 Needs to be measured at room temperature on the application board using a probe with very low (<=5pF) input capacitance.

E.3 Phase Locked Loop

E.3.1 Jitter Information

With each transition of the feedback clock, the deviation from the reference clock is measured and the input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the VCOCLK frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure E-1.**.

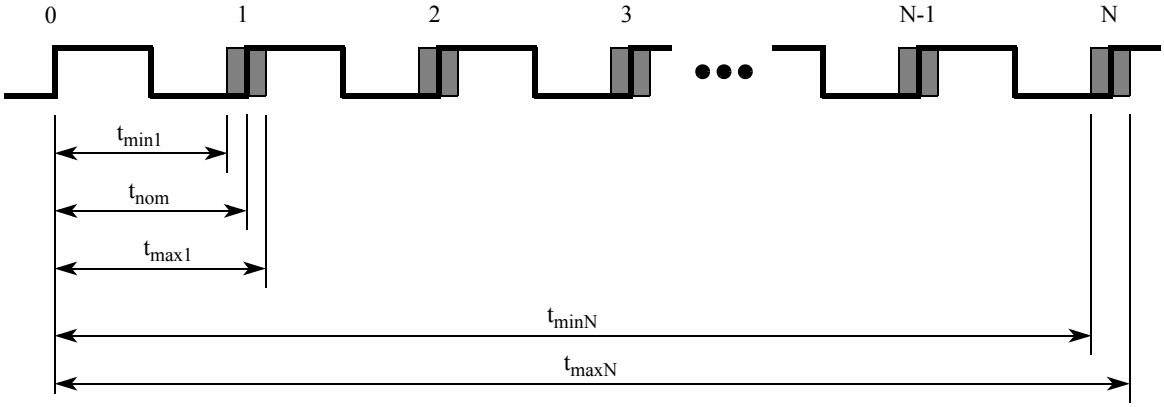


Figure E-1. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

[1] % deviation from target frequency

[2] f_{REF} = 1MHz, f_{BUS} = 32MHz

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5V <= VSUP <=18 V >, -40°C <= Tj <= 150°C > unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
	SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)					
1	Propagation Loop Delay TXD to RXD (Recessive to Dominant) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LRD}		 146 112 89 83 72 64	 (255)	ns
2	Propagation Delay TXD to CAN (Recessive to Dominant) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TRD}		 98 63 43 38 28 23		ns
3	Propagation Delay CAN to RXD (Recessive to Dominant, using slew rate 0)	t_{RRD}		42		ns
4	Propagation Loop Delay TXD to RXD (Dominant to Recessive) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LDR}		 366 224 153 139 114 102	 (255)	ns
5	Propagation Delay TXD to CAN (Dominant to Recessive) Slew Rate 6 Slew Rate 5 Slew Rate 4 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TDR}		 280 152 90 81 56 46		ns
6	Propagation Delay CAN to RXD (Dominant to Recessive, using slew rate 0)	t_{RDR}		56		ns

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0264	DDRE	R	0	0	0	0	0	0	DDRE1	DDRE0
		W								
0x0265	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0266	PERE	R	0	0	0	0	0	0	PERE1	PERE0
		W								
0x0267	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0268	PPSE	R	0	0	0	0	0	0	PPSE1	PPSE0
		W								
0x0269–0x027F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0280	PTADH	R	PTADH7	PTADH6	PTADH5	PTADH4	PTADH3	PTADH2	PTADH1	PTADH0
		W								
0x0281	PTADL	R	PTADL7	PTADL6	PTADL5	PTADL4	PTADL3	PTADL2	PTADL1	PTADL0
		W								
0x0282	PTIADH	R	PTIADH7	PTIADH6	PTIADH5	PTIADH4	PTIADH3	PTIADH2	PTIADH1	PTIADH0
		W								
0x0283	PTIADL	R	PTIADL7	PTIADL6	PTIADL5	PTIADL4	PTIADL3	PTIADL2	PTIADL1	PTIADL0
		W								
0x0284	DDRADH	R	DDRADH7	DDRADH6	DDRADH5	DDRADH4	DDRADH3	DDRADH2	DDRADH1	DDRADH0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	PERADH	R	PERADH7	PERADH6	PERADH5	PERADH4	PERADH3	PERADH2	PERADH1	PERADH0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	PPSADH	R	PPSADH7	PPSADH6	PPSADH5	PPSADH4	PPSADH3	PPSADH2	PPSADH1	PPSADH0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								