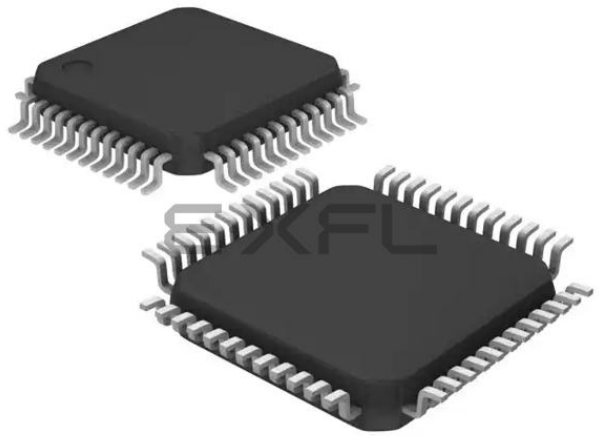

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc64f0mlf

Address	Module	Size (Bytes)
0x0718–0x077F	Reserved	104
0x0780–0x0787	SPI0	8
0x0788–0x078F	Reserved	8
0x0790–0x0797	SPI1	8
0x0798–0x07BF	Reserved	32
0x07C0–0x07C7	IIC0	8
0x07C8–0x097F	Reserved	56
0x0800–0x083F	CAN0	64
0x0840–0x098F	Reserved	336
0x0990–0x0997	CANPHY0	8
0x0998–0x099F		8
0x09A0–0x09AF	SENTTX	16
0x09B0–0x0FFF		1616

NOTE

Reserved register space shown in Table 1-2. is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns zero.

Table 1-3. S12ZVC-Family Memory Address Ranges

Device	Address	Memory Block	Size (Bytes)
MC9S12ZVC64 & MC9S12ZVCA64	0x00_1000 - 0x00_1FFF	SRAM	4K
	0x10_0000 - 0x10_03FF	EEPROM	1K
	0xFF_0000 - 0xFF_FFFF	Program Flash	64K
MC9S12ZVC96 & MC9S12ZVCA96	0x00_1000 - 0x00_2FFF	SRAM	8K
	0x10_0000 - 0x10_07FF	EEPROM	2K
	0xFE_8000 - 0xFF_FFFF	Program Flash	96K
MC9S12ZVC128 & MC9S12ZVCA128	0x00_1000 - 0x00_2FFF	SRAM	8K
	0x10_0000 - 0x10_07FF	EEPROM	2K
	0xFE_0000 - 0xFF_FFFF	Program Flash	128K
MC9S12ZVC192 & MC9S12ZVCA192	0x00_1000 - 0x00_3FFF	SRAM	12K
	0x10_0000 - 0x10_07FF	EEPROM	2K
	0xFD_0000 - 0xFF_FFFF	Program Flash	192K

1.11.5 Reprogramming the Security Bits

Security can also be disabled by erasing and reprogramming the security bits within the flash options/security byte to the unsecured value. Since the erase operation will erase the entire sector (0x7F_FE00–0x7F_FFFF) the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector containing the Flash options/security byte is not protected (see Flash protection). Thus Flash protection is a useful means of preventing this method. The microcontroller enters the unsecured state after the next reset following the programming of the security bits to the unsecured value.

This method requires that:

- The application software previously programmed into the microcontroller has been designed to have the capability to erase and program the Flash options/security byte.
- The Flash sector containing the Flash options/security byte is not protected.

1.11.6 Complete Memory Erase

The microcontroller can be unsecured by erasing the entire EEPROM and Flash memory contents. If ERASE_FLASH is successfully completed, then the Flash unsecures the device and programs the security byte automatically.

1.12 Resets and Interrupts

Table 1-12. lists all Reset sources and the vector address. Resets are explained in detail in the Chapter 8, “S12 Clock, Reset and Power Management Unit (S12CPMU_UHV_V7)””

Table 1-12. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
0xFF_FFFC	Power-On Reset (POR)	None	None
	Low Voltage Reset (LVR)	None	None
	External pin $\overline{\text{RESET}}$	None	None
	Clock monitor reset	None	OSCE Bit in CPMUOSC register & OMRE Bit in CPMUOSC2 register
	COP watchdog reset	None	CR[2:0] in CPMUCOP register

1.12.1 Interrupt Vectors

Table 1-13. lists all interrupt sources and vectors in the default order of priority. The interrupt module description provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 1-17. V_{BG} Reference Conversion Measurement Conditions for 5V operation

Description	Symbol	Value	Unit
I/O supply voltage	V_{DDX}	5	V
Analog supply voltage	V_{DDA}	5	V
ADC reference voltage	V_{RH}	5	V
ADC clock	f_{ADCCLK}	2	MHz
ADC sample time	t_{SMP}	4	ADC clock cycles
Bus frequency	f_{bus}	25	MHz
Ambient temperature	T_A	150	°C

1.14.2 Use Case Urea Concentration Level Sensor

In this application the signal runtime of ultrasonic response is measured. Sensor output is connected to PAD1. This case uses the ACMP0 to compare the sensor output voltage with a reference voltage provided by the DAC module. The output of the ACMP0 module is connected to high resolution timer (TIM1) to measure the signal runtime. See **Figure 1-5.**

1. Setup ACMP0, DAC,and PIM:
   - Select PAD1/ACMP0_1 as positive input to ACMP0
     - Set ACMP0C1.[ACPSEL1:ACPSEL0]= 0x01
   - Select Unbuffered DAC output DACU as negative input to ACMP0
     - Set ACMP0C1.[ACNSEL1:ACNSEL0]= 0x2
   - Select required ACMP0 hysteresis VACMP_hys
     - Set ACMP0C0.[ACHYS1:ACHYS0]= 11 (largest hysteresis)
   - Select required ACMP0 input filter characteristic
     - Set ACMP0C0.[ACDLY]= 0x1 (high speed characteristic).
   - Select Full Voltage Range for DAC
     - Set DACCTL[FVR]=0x1
   - Select DAC output voltage Vout = DACVOL[7:0] x (VRH-VRL)/256 + VRL
     - Set DACVOL=<required reference voltage>
   - Select DAC Mode unbuffered DAC and wait for DACU to settle Tsettle_DACU
     - Set DACCTL[DACM2:DACM0]=100

Table 2-33. Bit Indices of Implemented Register Bits per Port

		Port Data Register	Port Input Register	Data Direction Register	Pull Device Enable Register	Polarity Select Register	Port Interrupt Enable Register	Port Interrupt Flag Register	Digital Input Enable Register	Reduced Drive Register	Wired-Or Mode Register
Port		**PT**	**PTI**	**DDR**	**PER**	**PPS**	**PIE**	**PIF**	**DIE**	**RDR**	**WOM**
E		1-0	1-0	1-0	1-0	1-0	-	-	-	-	-
ADH		7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
ADL		7-0	7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-
T		7-0	7-0	7-0	7-0	7-0	-	-	-	-	-
S		7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	-	7-0
P		7-0	7-0	7-0	7-0	7-0	7-0	7-0	-	6-4,2,0	-
J		1-0	1-0	1-0	1-0	1-0	-	-	-	-	1-0
L		-	1-0	-	-	1-0	1-0	1-0	1-0	-	-

Table 2-34 shows the effect of enabled peripheral features on I/O state and enabled pull devices.

Table 2-34. Effect of Enabled Features

Enabled Feature[1]	Related Signal(s)	Effect on I/O state	Effect on enabled pull device
CPMU OSC	EXTAL, XTAL	CPMU takes control	Forced off
TIMx output compare y	IOCx_y	Forced output	Forced off, pulldown forced off if open-drain
TIMx input capture y	IOCx_y	None[2]	None[3]
SPIx	MISOx, MOSx, SCKx, $\overline{SSx}$	SPI takes control	Forced off if output, pulldown forced off if open-drain
SCIx transmitter	TXDx	Forced output	Forced off, pulldown forced off if open-drain
SCIx receiver	RXDx	Forced input	None[3]
IICx	SDAx, SCLx	Forced open-drain	Pulldown forced off
S12ZDBG	DBGEEV	None[2]	None[3]
PWMx channel y	PWMx_y	Forced output	Forced off
ADCx	ANy	None[2 4]	None[3]
	VRH		
ACMPx	ACMPx_0, ACMPx_1	None[2 4]	None[3]
	ACMPOx	Forced output	Forced off
DACx	AMPPx, AMPMx	None[2 4]	None[3]
	DACUx, AMPx	Digital output forced off	Forced off

4.3.2.1 Mode Register (MODE)

Address: 0x0070

	7	6	5	4	3	2	1	0
R	MODC	0	0	0	0	0	0	0
W								
Reset	MODC[1]	0	0	0	0	0	0	0

1. External signal (see Table 4-3).

= Unimplemented or Reserved

Figure 4-3. Mode Register (MODE)

Read: Anytime.

Write: Only if a transition is allowed (see Figure 4-4).

The MODE register determines the operating mode of the MCU.

CAUTION

Table 4-4. MODE Field Descriptions

Field	Description
7 MODC	**Mode Select Bit** — This bit determines the current operating mode of the MCU. Its reset value is captured from the MODC pin at the rising edge of the $\overline{\text{RESET}}$ pin. Figure 4-4 illustrates the only valid mode transition from special single-chip mode to normal single chip mode.

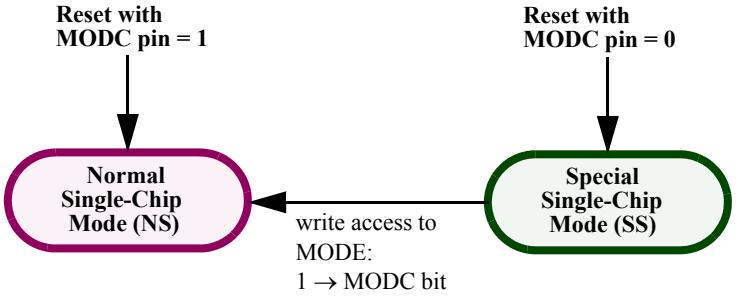

Figure 4-4. Mode Transition Diagram

6.3.2.14 Debug Comparator D Control Register (DBGDCTL)

Address: 0x0140

	7	6	5	4	3	2	1	0
R	0	0	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-17. Debug Comparator D Control Register

Read: Anytime.

Write: If DBG not armed.

Table 6-24. DBGDCTL Field Descriptions

Field[1]	Description
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

1 If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 6-25 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 6-25. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

frequency as shown in Table 8-2. Setting the VCOFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 8-2. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32MHz <= f_{VCO} <= 48MHz	00
48MHz < f_{VCO} <= 64MHz	01
Reserved	10
Reserved	11

8.3.2.3 S12CPMU_UHV_V7 Reference Divider Register (CPMUREFDIV)

The CPMUREFDIV register provides a finer granularity for the PLL multiplier steps when using the external oscillator as reference.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
W								
Reset	0	0	0	0	1	1	1	1

Figure 8-6. S12CPMU_UHV_V7 Reference Divider Register (CPMUREFDIV)

Read: Anytime

Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

If XOSCLCP is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If XOSCLCP is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 8-3.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1MHz <= f_{REF} <= 2MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

9.4.2.24 ADC Command and Result Offset Register 1 (ADCCROFF1)

It is important to note that these bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).

Module Base + 0x0025

	7	6	5	4	3	2	1	0
R	0	CMDRES_OFF1[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-27. ADC Command and Result Offset Register 1 (ADCCROFF1)

Read: Anytime

Write: These bits are writable if bit ADC_EN clear or bit SMOD_ACC set

Table 9-31. ADCCROFF1 Field Descriptions

Field	Description
6-0 CMDRES_OFF1 [6:0]	**ADC Result Address Offset Value** — These bits represent the conversion command and result offset value relative to the conversion command base pointer address and result base pointer address in the memory map to refer to CSL_1 and RVL_1. It is used to calculate the address inside the system RAM to which the result at the end of the current conversion is stored to and the area (RAM or NVM) from which the conversion commands are loaded from. These bits do not represent absolute addresses instead it is an sample offset (object size 16bit for RVL, object size 32bit for CSL).,These bits can only be modified if bit ADC_EN is clear. See also Section 9.5.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) and Section 9.5.3.2.3, “Introduction of the two Result Value Lists (RVLs) for more details.

9.8.5 List Usage — CSL double buffer mode and RVL double buffer mode

In this use case both list types are configured for double buffer mode (CSL_BMOD=1’b1) and RVL_BMOD=1’b1).

This setup is the same as Section 9.8.3, “List Usage — CSL double buffer mode and RVL double buffer mode but at the end of a CSL the CSL is not always swapped (bit LDOK not always set with bit RSTA). The Result Value List is swapped whenever a CSL is finished or a CSL got aborted.

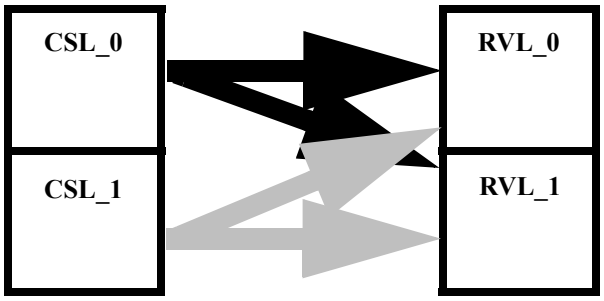

Figure 9-39. CSL Double Buffer Mode — RVL Double Buffer Mode Diagram

9.8.6 RVL swapping in RVL double buffer mode and related registers ADCIMDRI and ADCEOLRI

When using the RVL in double buffer mode, the registers ADCIMDRI and ADCEOLRI can be used by the application software to identify which RVL holds relevant and latest data and which CSL is related to this data. These registers are updated at the setting of one of the CON_IF[15:1] or the EOL_IF interrupt flags. As described in the register description Section 9.4.2.13, “ADC Intermediate Result Information Register (ADCIMDRI) and Section 9.4.2.14, “ADC End Of List Result Information Register (ADCEOLRI), the register ADCIMDRI, for instance, is always updated at the occurrence of a CON_IF[15:1] interrupt flag amongst other cases. Also each time the last conversion command of a CSL is finished and the corresponding result is stored, the related EOL_IF flag is set and register ADCEOLRI is updated. Hence application software can pick up conversion results, or groups of results, or an entire result list driven fully by interrupts. A use case example diagram is shown in Figure 9-40.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0021 PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
	W								
0x0022 PACNTH	R	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
	W								
0x0023 PACNTL	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	OCPD7	OCPD6	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 11-5. TIM16B8CV3 Register Summary (Sheet 2 of 2)

[1] The register is available only if corresponding channel exists.

11.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
Reset	0	0	0	0	0	0	0	0

Figure 11-6. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 11-2. TIOS Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 IOS[7:0]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding implemented channel acts as an input capture. 1 The corresponding implemented channel acts as an output compare.

Only bits related to implemented channels are valid.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	RESERVED	RESERVED	RESERVED	RESERVED	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	RESERVED	RESERVED	RESERVED	RESERVED	FOC3	FOC2	FOC1	FOC0
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
	W								
0x0007 TTOV	R	RESERVED	RESERVED	RESERVED	RESERVED	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								
0x0009 TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
	W								
0x000A TCTL3	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								
0x000B TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
	W								
0x000C TIE	R	RESERVED	RESERVED	RESERVED	RESERVED	C3I	C2I	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
	W								
0x000E TFLG1	R	RESERVED	RESERVED	RESERVED	RESERVED	C3F	C2F	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL[1]	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0024–0x002B Reserved	R								
	W								
0x002C OCPD	R	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
	W								
0x002D Reserved	R								
0x002E PTPSR	R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
	W								
0x002F Reserved	R								
	W								

Figure 12-3. TIM16B4CV3 Register Summary

14.4.5.5 LIN Transmit Collision Detection

This module allows to check for collisions on the LIN bus.

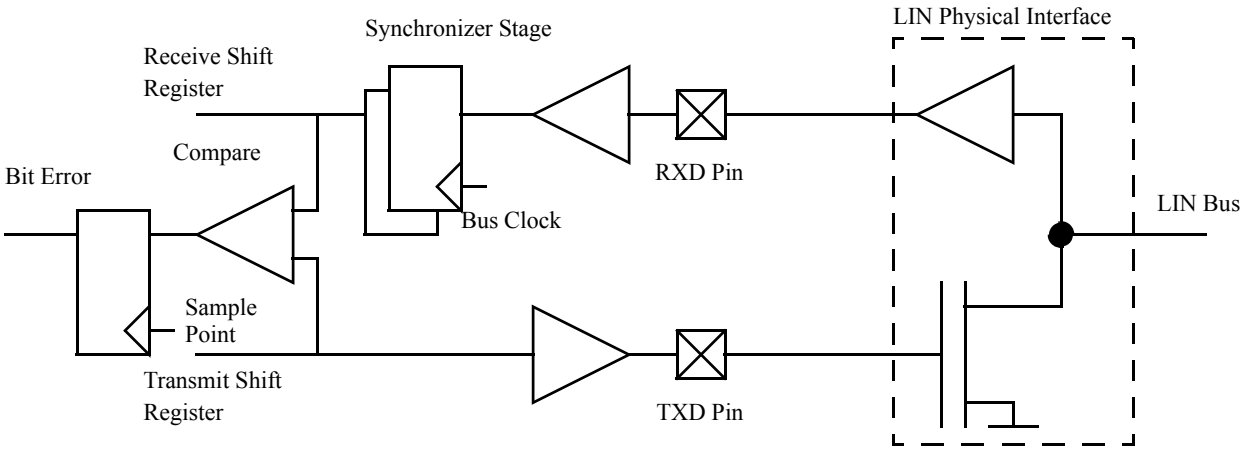

Figure 14-18. Collision Detect Principle

If the bit error circuit is enabled (BERRM[1:0] = 0:1 or = 1:0]), the error detect circuit will compare the transmitted and the received data stream at a point in time and flag any mismatch. The timing checks run when transmitter is active (not idle). As soon as a mismatch between the transmitted data and the received data is detected the following happens:

- The next bit transmitted will have a high level (TXPOL = 0) or low level (TXPOL = 1)
- The transmission is aborted and the byte in transmit buffer is discarded.
- the transmit data register empty and the transmission complete flag will be set
- The bit error interrupt flag, BERRIF, will be set.
- No further transmissions will take place until the BERRIF is cleared.

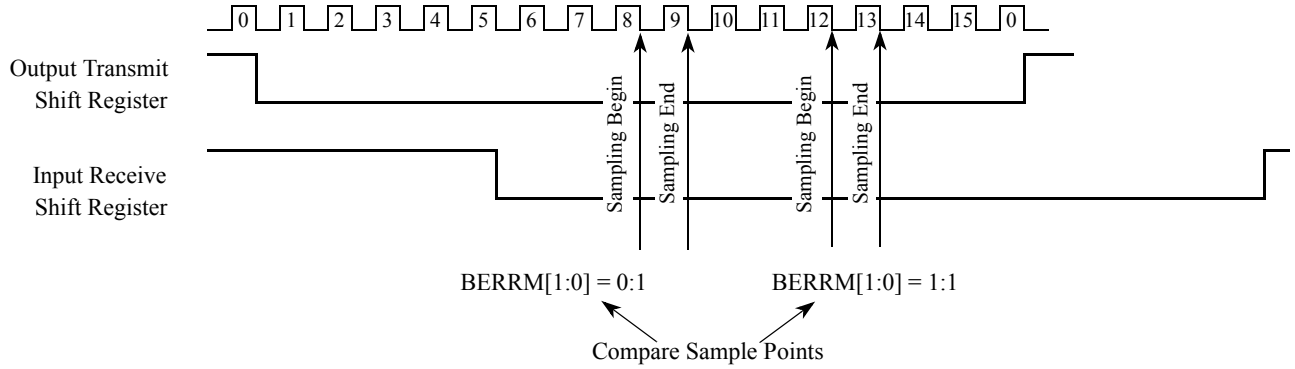

Figure 14-19. Timing Diagram Bit Error Detection

If the bit error detect feature is disabled, the bit error interrupt flag is cleared.

NOTE

The RXPOL and TXPOL bit should be set the same when transmission collision detect feature is enabled, otherwise the bit error interrupt flag may be set incorrectly.

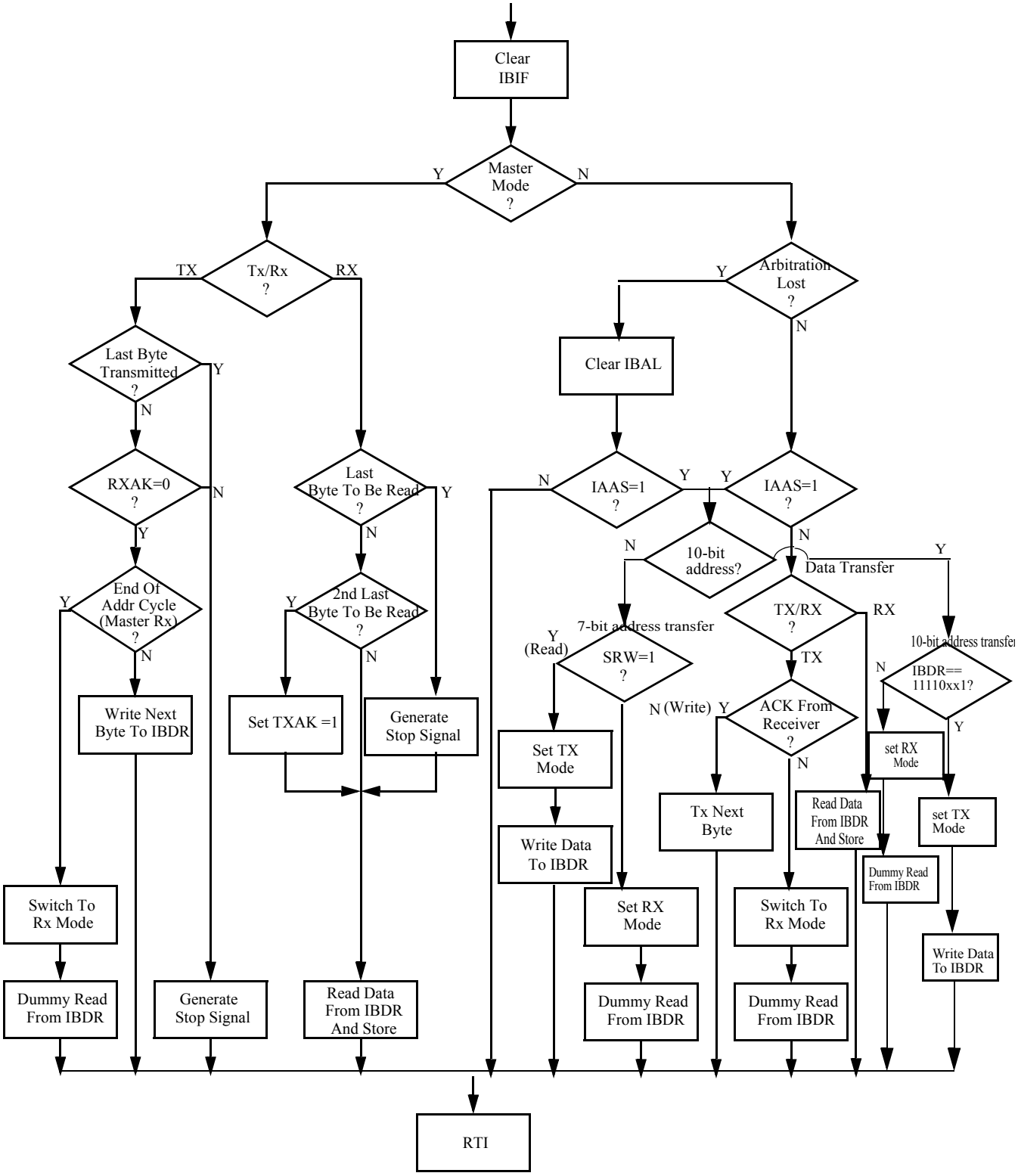

Figure 16-16. Flow-Chart of Typical IIC Interrupt Routine

17.4.2.5 Reserved Register

Module Base + 0x0004 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 17-6. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

17.4.2.6 Reserved Register

Module Base + 0x0005 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 17-7. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only and is not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

17.4.2.7 CAN Physical Layer Interrupt Enable Register (CPIE)

Module Base + 0x0006 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	CPVFIE	CPDTIE	0	0	CPOCIE
W								
Reset	0	0	0	0	0	0	0	0

Figure 17-8. CAN Physical Layer Interrupt Enable Register (CPIE)

[1] Read: Anytime
Write: Anytime

The operational amplifier is also stand alone usable.

Figure 19-1 shows the block diagram of the DAC_8B5V module.

19.2.1 Features

The DAC_8B5V module includes these distinctive features:

- 1 digital-analog converter channel with:
  - 8 bit resolution
  - full and reduced output voltage range
  - buffered or unbuffered analog output voltage usable
- operational amplifier stand alone usable

19.2.2 Modes of Operation

The DAC_8B5V module behaves as follows in the system power modes:

1. CPU run mode

   The functionality of the DAC_8B5V module is available.

2. CPU stop mode

   Independent from the mode settings, the operational amplifier is disabled, switch S1 and S2 are open.

   If the “Unbuffered DAC” mode was used before entering stop mode, then the DACU pin will reach VRH voltage level during stop mode.

   The content of the configuration registers is unchanged.

NOTE

After enabling and after return from CPU stop mode, the DAC_8B5V module needs a settling time to get fully operational, see Settling time specification of dac_8b5V_analog_ll18.

22.1.1 Glossary

Command Write Sequence — An MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

EEPROM Memory — The EEPROM memory constitutes the nonvolatile memory store for data.

EEPROM Sector — The EEPROM sector is the smallest portion of the EEPROM memory that can be erased. The EEPROM sector consists of 4 bytes.

NVM Command Mode — An NVM mode using the CPU to setup the FCCOB register to pass parameters required for Flash command execution.

Phrase — An aligned group of four 16-bit words within the P-Flash memory. Each phrase includes two sets of aligned double words with each set including 7 ECC bits for single bit fault correction and double bit fault detection within each double word.

P-Flash Memory — The P-Flash memory constitutes the main nonvolatile memory store for applications.

P-Flash Sector — The P-Flash sector is the smallest portion of the P-Flash memory that can be erased. Each P-Flash sector contains 512 bytes.

Program IFR — Nonvolatile information register located in the P-Flash block that contains the Version ID, and the Program Once field.

22.1.2 Features

22.1.2.1 P-Flash Features

- 192 KB of P-Flash divided into 384 sectors of 512 bytes
- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the EEPROM memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

22.1.2.2 EEPROM Features

- 2 KB of EEPROM memory composed of one 2 KB Flash block divided into 512 sectors of 4 bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation

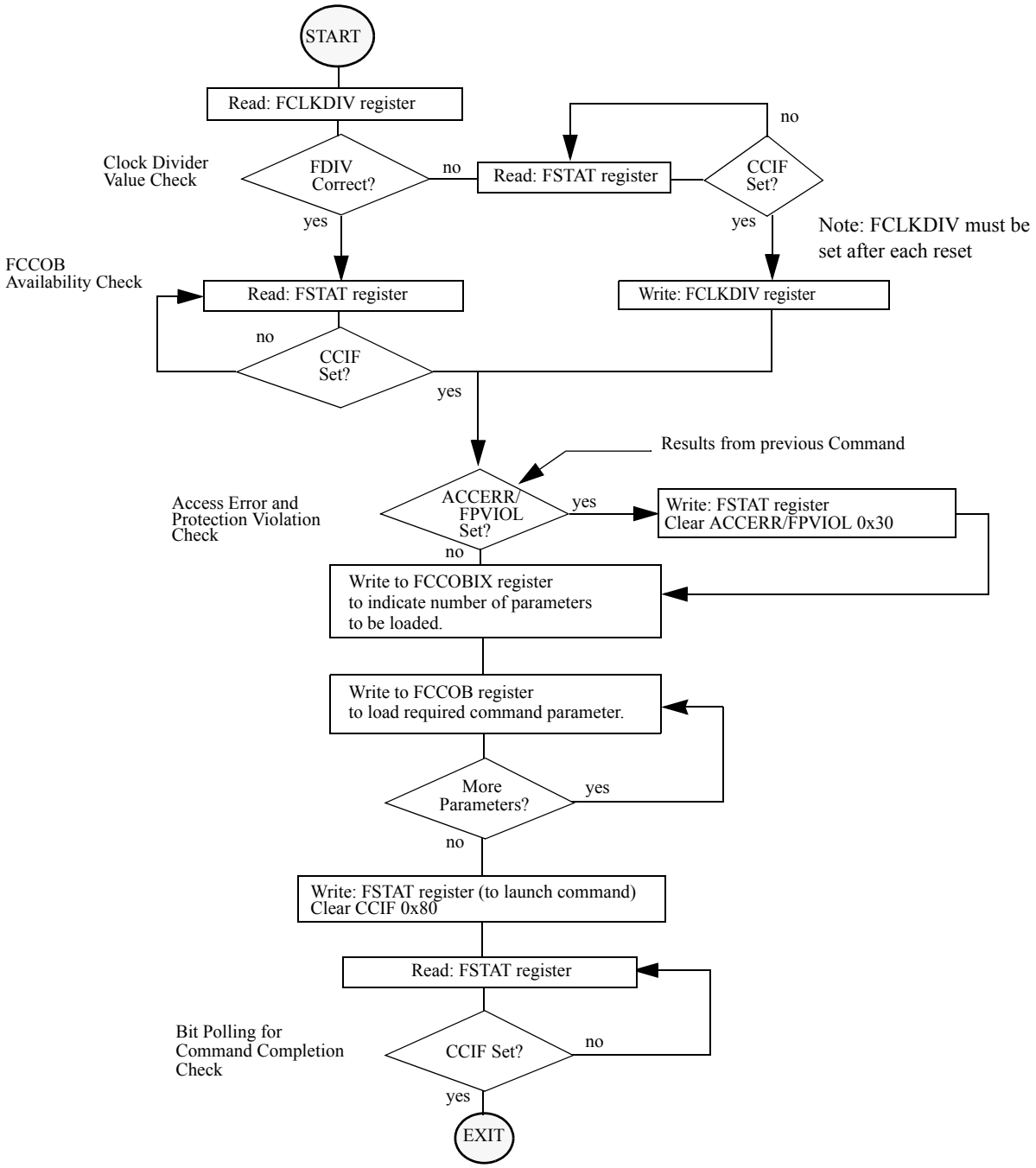

Figure 22-30. Generic Flash Command Write Sequence Flowchart

B.1.2.1 ADC Accuracy Definitions

For the following definitions see also **Figure B-2.**.
Differential non-linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The integral non-linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

The following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N(POSTDIV + 1)}}$$

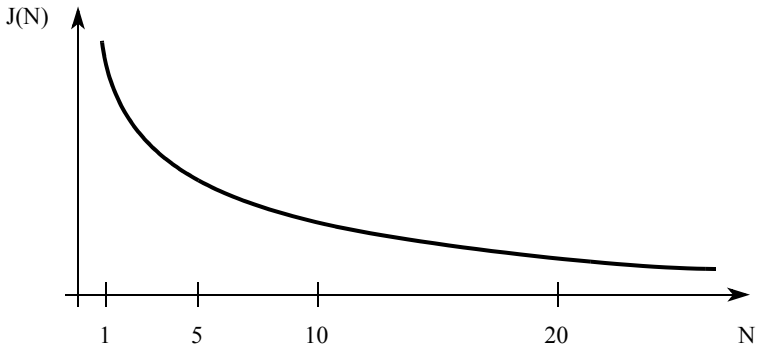

Figure E-2. Maximum Bus Clock Jitter Approximation (N = Number of Bus Cycles)

NOTE

Peripheral module prescalers eliminate the effect of jitter to a large extent.

Table E-4. PLL Characteristics (Junction Temperature From –40°C To +175°C)

Conditions are 4.5 V < V_{DDX}< 5.5 V unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VCO frequency during system reset	f_{VCORST}	8	—	32	MHz
2	VCO locking range	f_{VCO}	32	—	64	MHz
3	Reference Clock	f_{REF}	1	—	—	MHz
4	Lock Detection	$\|\Delta_{Lock}\|$	0	—	1.5	%[1]
5	Un-Lock Detection Threshold	$\|\Delta_{unl}\|$	0.5	—	2.5	%[1]
7	Time to lock	t_{lock}	—	—	150 + 256/f_{REF}	µs
8	Jitter fit parameter [2] 40°C < T_J < 150°C	j_1	—	—	2	%
9a	PLL Clock Monitor Failure assert frequency	f_{PMFA}	0.45	1.1	1.6	MHz