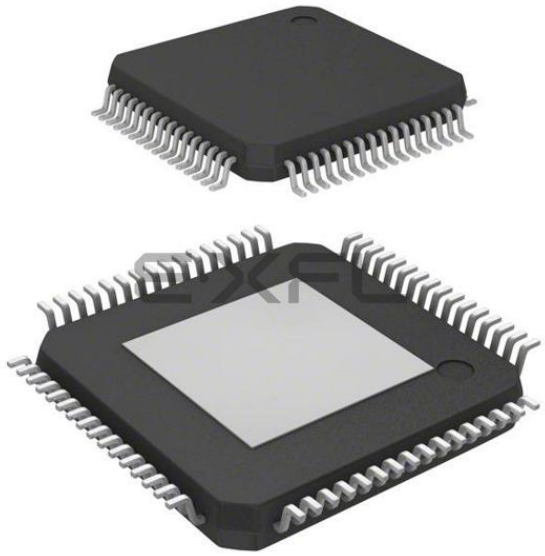

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 16x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvc96f0mkh

Chapter 13
Pulse-Width Modulator (S12PWM8B8CV2)

Chapter 14
Serial Communication Interface (S12SCIV6)

Figure 1-2. MC9S12ZVC-Family Global Memory Map

1.6.1 Part ID Assignments

The ID is located in four 8-bit registers at addresses 0x0000 to 0x0003. The read-only value is a unique part ID for each revision of the chip. Table 1-4 shows the assigned Part ID register value.

Table 1-4. Assigned ID Numbers

Device	Mask Set Number	Part ID
MC9S12ZVCA64	N23N	05.1D.10.00
MC9S12ZVCA96	N23N	05.1D.10.00
MC9S12ZVCA128	N23N	05.1D.10.00
MC9S12ZVCA192	N23N	05.1D.10.00
MC9S12ZVC64	N23N	05.1D.10.00
MC9S12ZVC96	N23N	05.1D.10.00
MC9S12ZVC128	N23N	05.1D.10.00
MC9S12ZVC192	N23N	05.1D.10.00

1.7 Signal Description and Device Pinouts

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the individual IP blocks on the device.

NOTE

To avoid current drawn from floating inputs, all non-bonded pins should be configured as output or configured as input with a pull up or pull down device enabled.

2.3.2.4 Module Routing Register 3 (MODRR3)

Address 0x0203 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	T0IC3RR1	T0IC3RR0	T0IC2RR	T0IC1RR	0
W								
	—	—	—	TIM0 IC3		TIM0 IC2	TIM0 IC1	—
Reset	0	0	0	0	0	0	0	0

Figure 2-5. Module Routing Register 3 (MODRR3)

[1] Read: Anytime
Write: Anytime

Table 2-8. MODRR3 Routing Register Field Descriptions

Field	Description
4 T0IC3RR1	**Module Routing Register** — TIM0 IC3 routing bit 1 If timer channel is not used with a pin (T0IC3RR0=0) then one out of two internal sources can be selected as input. 1 TIM0 input capture channel 3 to RXD1 0 TIM0 input capture channel 3 to RXD0
3 T0IC3RR0	**Module Routing Register** — TIM0 IC3 routing bit 0 1 TIM0 input capture channel 3 to PS4 0 TIM0 input capture channel 3 internally to RXD (see T0IC3RR1)
2 T0IC2RR	**Module Routing Register** — TIM0 IC2 routing 1 TIM0 input capture channel 2 to PS5 0 TIM0 input capture channel 2 internally to ACLK
1 T0IC1RR	**Module Routing Register** — TIM0 IC1 routing 1 TIM0 input capture channel 1 to PS6 0 TIM0 input capture channel 1 to PS7 (SENT_TX)

- General-purpose data output availability depends on prioritization; input data registers always reflect the pin status independent of the use.
- Pull-device availability, pull-device polarity, wired-or mode, key-wake up functionality are independent of the prioritization unless noted differently.
- For availability of individual bits refer to Section 2.3.1, “Register Map” and Table 2-33.

2.3.3.1 Port Data Register

Address 0x0260 PTE
0x0280 PTADH
0x0281 PTADL
0x02C0 PTT
0x02D0 PTS
0x02F0 PTP
0x0310 PTJ

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	PTx7	PTx6	PTx5	PTx4	PTx3	PTx2	PTx1	PTx0
Reset	0	0	0	0	0	0	0	0

Figure 2-10. Port Data Register

[1] Read: Anytime. The data source is depending on the data direction value.
Write: Anytime

This is a generic description of the standard port data registers. Refer to Table 2-33 to determine the implemented bits in the respective register. Unimplemented bits read zero.

Table 2-11. Port Data Register Field Descriptions

Field	Description
7-0 PTx7-0	**Port Data — General purpose input/output data** This register holds the value driven out to the pin if the pin is used as a general purpose output. When not used with the alternative function (refer to Table 2-2), these pins can be used as general purpose I/O. If the associated data direction bits of these pins are set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read.

3.3.2.2 BDC Control Status Register Low (BDCCSRL)

Register Address: This register is not in the device memory map. It is accessible using BDC inherent addressing commands

	7	6	5	4	3	2	1	0
R W	WAIT	STOP	RAMWF	OVRUN	NORESP	RDINV	ILLACC	ILLCMD
Reset	0	0	0	0	0	0	0	0

Figure 3-4. BDC Control Status Register Low (BDCCSRL)

Read: BDC access only.

Write: Bits [7:5], [3:0] BDC access only, restricted to flag clearing by writing a “1” to the bit position.
Write: Bit 4 never. It can only be cleared by a SYNC pulse.

If ACK handshaking is enabled then BDC commands with ACK causing a BDCCSRL[3:1] flag setting condition also generate a long ACK pulse. Subsequent commands that are executed correctly generate a normal ACK pulse. Subsequent commands that are not correctly executed generate a long ACK pulse. The first ACK pulse after WAIT or STOP have been set also generates a long ACK. Subsequent ACK pulses are normal, whilst STOP and WAIT remain set.

Long ACK pulses are not immediately generated if an overrun condition is caused by the host driving the BKGD pin low whilst a target ACK is pending, because this would conflict with an attempted host transmission following the BKGD edge. When a whole byte has been received following the offending BKGD edge, the OVRUN bit is still set, forcing subsequent ACK pulses to be long.

Unimplemented BDC opcodes causing the ILLCMD bit to be set do not generate a long ACK because this could conflict with further transmission from the host. If the ILLCMD is set for another reason, then a long ACK is generated for the current command if it is a BDC command with ACK.

Table 3-6. BDCCSRL Field Descriptions

Field	Description
7 WAIT	**WAIT Indicator Flag** — Indicates that the device entered wait mode. Writing a “1” to this bit whilst in wait mode has no effect. Writing a “1” after exiting wait mode, clears the bit. 0 Device did not enter wait mode 1 Device entered wait mode.
6 STOP	**STOP Indicator Flag** — Indicates that the CPU requested stop mode following a STOP instruction. Writing a “1” to this bit whilst not in stop mode clears the bit. Writing a “1” to this bit whilst in stop mode has no effect. This bit can only be set when the BDC is enabled. 0 Device did not enter stop mode 1 Device entered stop mode.
5 RAMWF	**RAM Write Fault** — Indicates an ECC double fault during a BDC write access to RAM. Writing a “1” to this bit, clears the bit. 0 No RAM write double fault detected. 1 RAM write double fault detected.

- One non-maskable system call interrupt (SYS)
- One non-maskable machine exception vector request
- One spurious interrupt vector request
- One system reset vector request

Each of the I-bit maskable interrupt requests can be assigned to one of seven priority levels supporting a flexible priority scheme. The priority scheme can be used to implement nested interrupt capability where interrupts from a lower level are automatically blocked if a higher level interrupt is being processed.

5.1.1 Glossary

The following terms and abbreviations are used in the document.

Table 5-2. Terminology

Term	Meaning
CCW	Condition Code Register (in the S12Z CPU)
DMA	Direct Memory Access
INT	Interrupt
IPL	Interrupt Processing Level
ISR	Interrupt Service Routine
MCU	Micro-Controller Unit
$\overline{\text{IRQ}}$	refers to the interrupt request associated with the $\overline{\text{IRQ}}$ pin
$\overline{\text{XIRQ}}$	refers to the interrupt request associated with the $\overline{\text{XIRQ}}$ pin

5.1.2 Features

- Interrupt vector base register (IVBR)
- One system reset vector (at address 0xFFFFFC).
- One non-maskable unimplemented page1 op-code trap (SPARE) vector (at address vector base[1] + 0x0001F8).
- One non-maskable unimplemented page2 op-code trap (TRAP) vector (at address vector base[1] + 0x0001F4).
- One non-maskable software interrupt request (SWI) vector (at address vector base[1] + 0x0001F0).
- One non-maskable system call interrupt request (SYS) vector (at address vector base[1] + 0x00001EC).
- One non-maskable machine exception vector request (at address vector base[1] + 0x0001E8).
- One spurious interrupt vector (at address vector base[1] + 0x0001DC).
- One X-bit maskable interrupt vector request associated with $\overline{\text{XIRQ}}$ (at address vector base[1] + 0x0001D8).

1. The vector base is a 24-bit address which is accumulated from the contents of the interrupt vector base register (IVBR, used as the upper 15 bits of the address) and 0x000 (used as the lower 9 bits of the address).

Figure 8-2 shows a block diagram of the XOSCLCP.

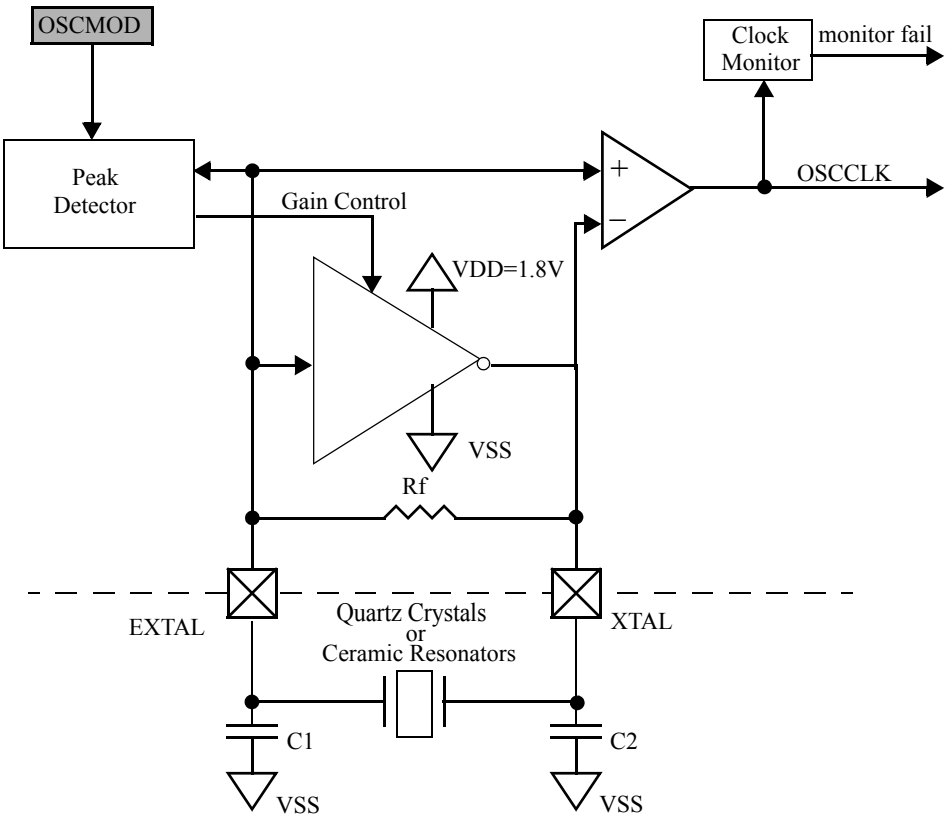


Figure 8-2. XOSCLCP Block Diagram

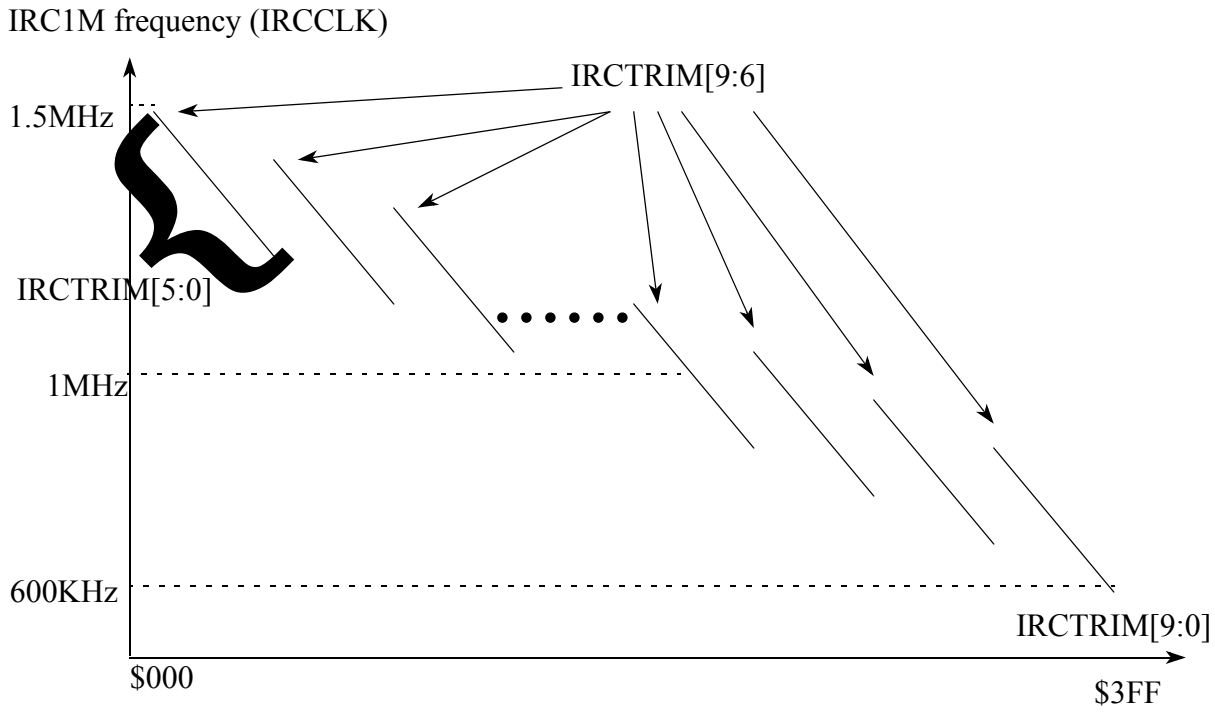


Figure 8-29. IRC1M Frequency Trimming Diagram

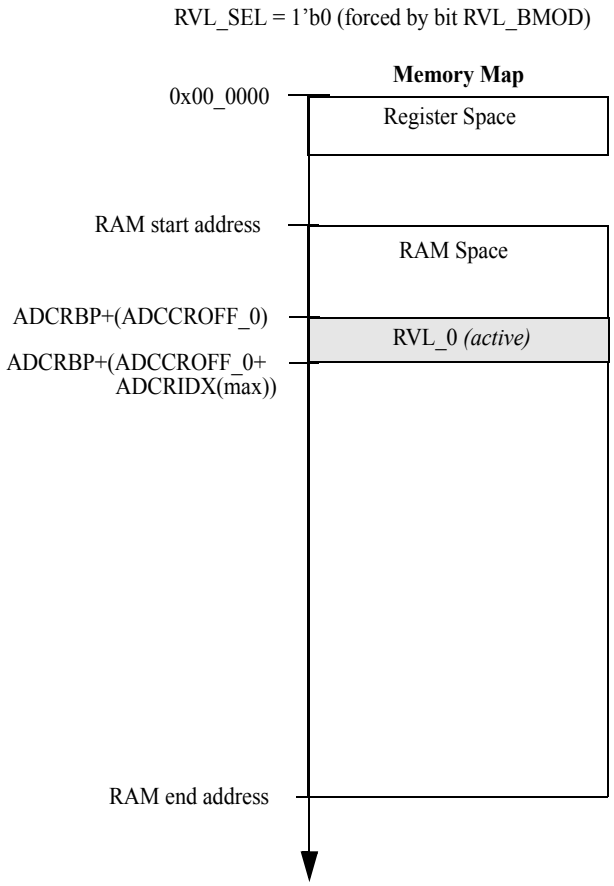
9.2 Key Features

- Programmer's Model with List Based Architecture for conversion command and result value organization
- Selectable resolution of 8-bit, 10-bit, or 12-bit
- Channel select control for n external analog input channels
- Provides up to eight device internal channels (please see the device reference manual for connectivity information and Figure 9-2)
- Programmable sample time
- A sample buffer amplifier for channel sampling (improved performance in view to influence of channel input path resistance versus conversion accuracy)
- Left/right justified result data
- Individual selectable VRH_0/1 and VRL_0/1 inputs on a conversion command basis (please see Figure 9-2)
- Special conversions for selected VRH_0/1, VRL_0/1, (VRL_0/1 + VRH_0/1) / 2
- 15 conversion interrupts with flexible interrupt organization per conversion result
- One dedicated interrupt for "End Of List" type commands
- Command Sequence List (CSL) with a maximum number of 64 command entries
- Provides conversion sequence abort
- Restart from top of active Command Sequence List (CSL)
- The Command Sequence List and Result Value List are implemented in double buffered manner (two lists in parallel for each function)
- Conversion Command (CSL) loading possible from System RAM or NVM
- Single conversion flow control register with software selectable access path
- Two conversion flow control modes optimized to different application use cases

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ADCEOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0011	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	Reserved	Reserved					0	0
		W								
0x0014	ADCCMD_0	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0015	ADCCMD_1	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0016	ADCCMD_2	R	SMP[4:0]					0	0	Reserved
		W								
0x0017	ADCCMD_3	R	Reserved	Reserved	Reserved					
		W								
0x0018	Reserved	R	Reserved							
		W								
0x0019	Reserved	R	Reserved							
		W								
0x001A	Reserved	R	Reserved							
		W								
0x001B	Reserved	R	Reserved							
		W								
0x001C	ADCCIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x001D	ADCCBP_0	R	CMD_PTR[23:16]							
		W								
0x001E	ADCCBP_1	R	CMD_PTR[15:8]							
		W								
0x001F	ADCCBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0020	ADCRIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0021	ADCRBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0022	ADCRBP_1	R	RES_PTR[15:8]							
		W								
0x0023	ADCRBP_2	R	RES_PTR[7:2]						0	0
		W								
0x0024	ADCCROFF0	R	0	CMDRES_OFF0[6:0]						
		W								
0x0025	ADCCROFF1	R	0	CMDRES_OFF1[6:0]						
		W								
0x0026	Reserved	R	0	0	0	0	Reserved			
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 2 of 3)



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

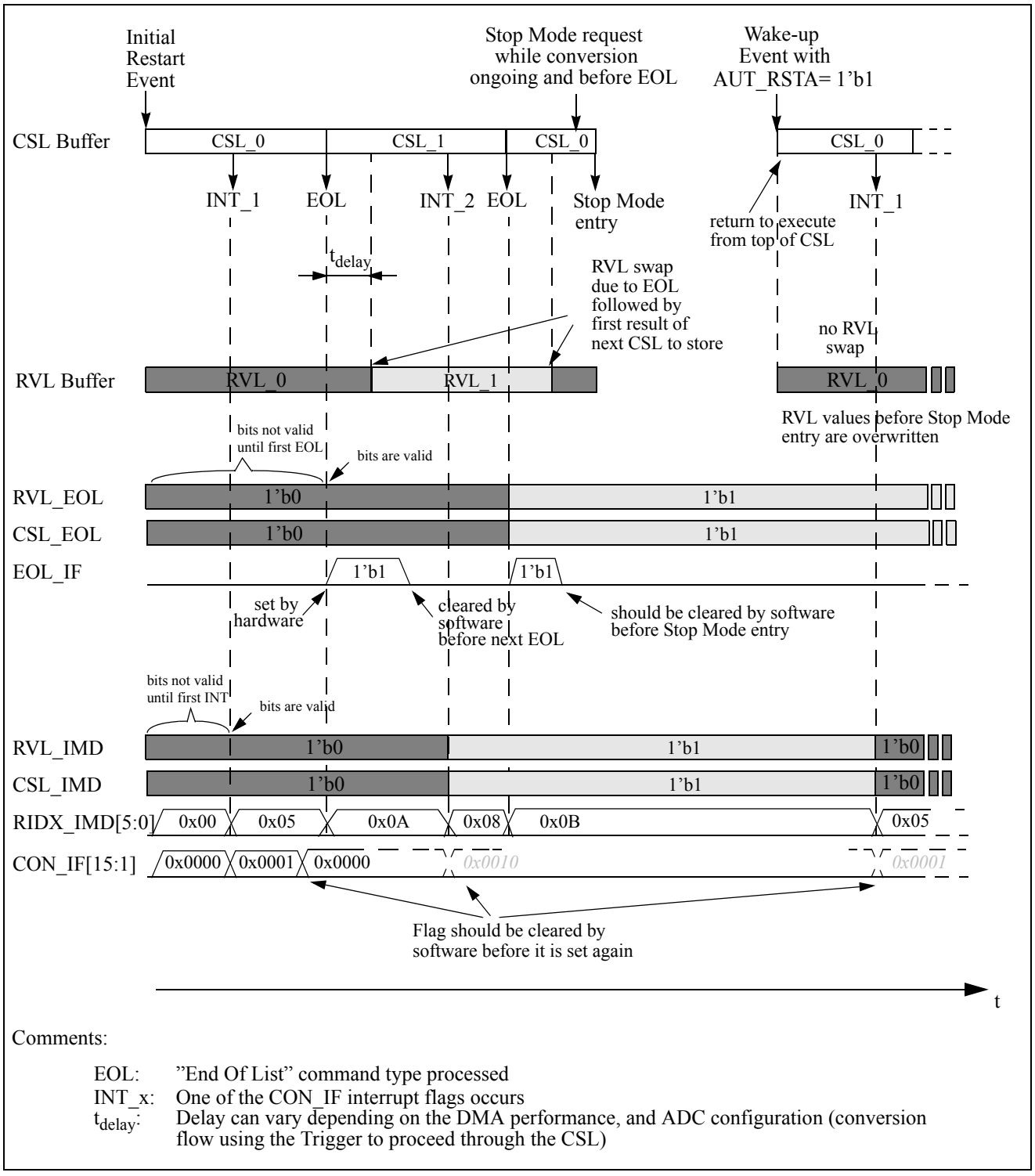
Figure 9-34. Result Value List Schema in Single Buffer Mode

While ADC is enabled, one Result Value List is active (indicated by bit RVL_SEL). The conversion Result Value List can be read anytime. When the ADC is enabled the conversion result address registers (ADCRBP, ADCCROFF_0/1, ADCRIDX) are read only and register ADCRIDX is under control of the ADC.

A conversion result is always stored as 16bit entity in unsigned data representation. Left and right justification inside the entity is selected via the DJM control bit. Unused bits inside an entity are stored zero.

Table 9-32. Conversion Result Justification Overview

Conversion Resolution (SRES[1:0])	Left Justified Result (DJM = 1'b0)	Right Justified Result (DJM = 1'b1)
8 bit	{Result[7:0],8'b00000000}	{8'b00000000,Result[7:0]}
10 bit	{Result[9:0],6'b000000}	{6'b000000,Result[9:0]}
12 bit	{Result[11:0],4'b0000}	{4'b0000,Result[11:0]}



Comments:

EOL: "End Of List" command type processed
INT_x: One of the CON_IF interrupt flags occurs
t_{delay}: Delay can vary depending on the DMA performance, and ADC configuration (conversion flow using the Trigger to proceed through the CSL)

Figure 9-40. RVL Swapping — Use Case Diagram

12.3.2.3 Timer Count Register (TCNT)

Module Base + 0x0004

	15	14	13	12	11	10	9	9
R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
Reset	0	0	0	0	0	0	0	0

Figure 12-6. Timer Count Register High (TCNTH)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Reset	0	0	0	0	0	0	0	0

Figure 12-7. Timer Count Register Low (TCNTL)

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes .

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

12.3.2.4 Timer System Control Register 1 (TSCR1)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-8. Timer System Control Register 1 (TSCR1)

Read: Anytime

Write: Anytime

Figure 14-17 shows two cases of break detect. In trace RXD_1 the break symbol starts with the start bit, while in RXD_2 the break starts in the middle of a transmission. If BRKDFE = 1, in RXD_1 case there will be no byte transferred to the receive buffer and the RDRF flag will not be modified. Also no framing error or parity error will be flagged from this transfer. In RXD_2 case, however the break signal starts later during the transmission. At the expected stop bit position the byte received so far will be transferred to the receive buffer, the receive data register full flag will be set, a framing error and if enabled and appropriate a parity error will be set. Once the break is detected the BRKDIF flag will be set.

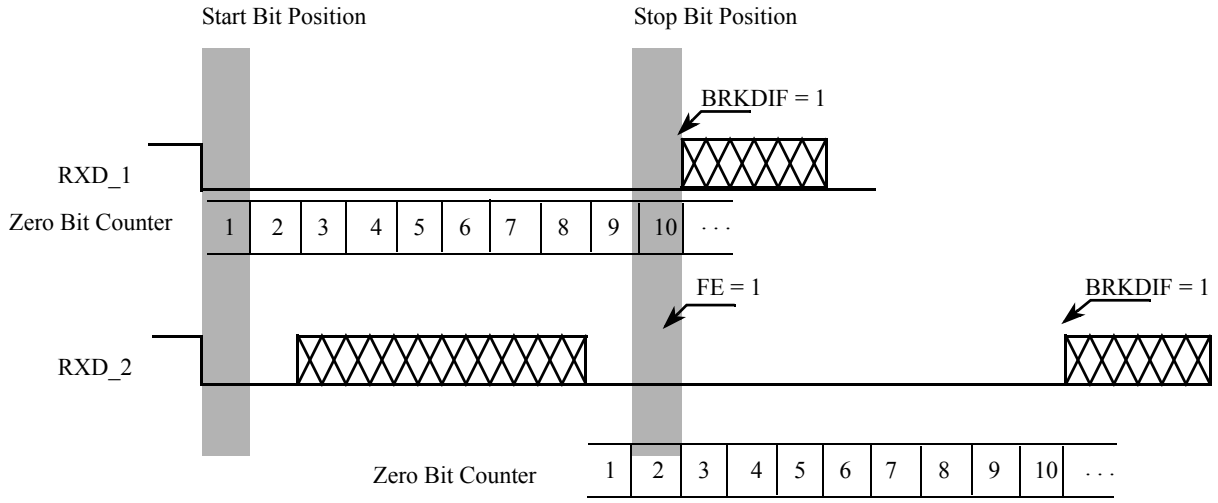


Figure 14-17. Break Detection if BRKDFE = 1 (M = 0)

14.4.5.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the SCI data register.

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

Figure 14-26 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

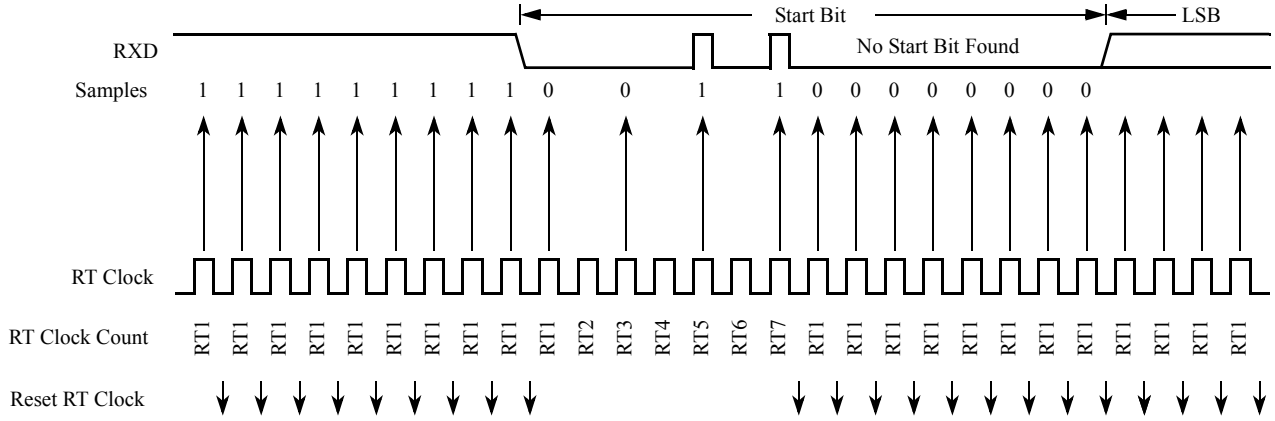


Figure 14-26. Start Bit Search Example 5

In Figure 14-27, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

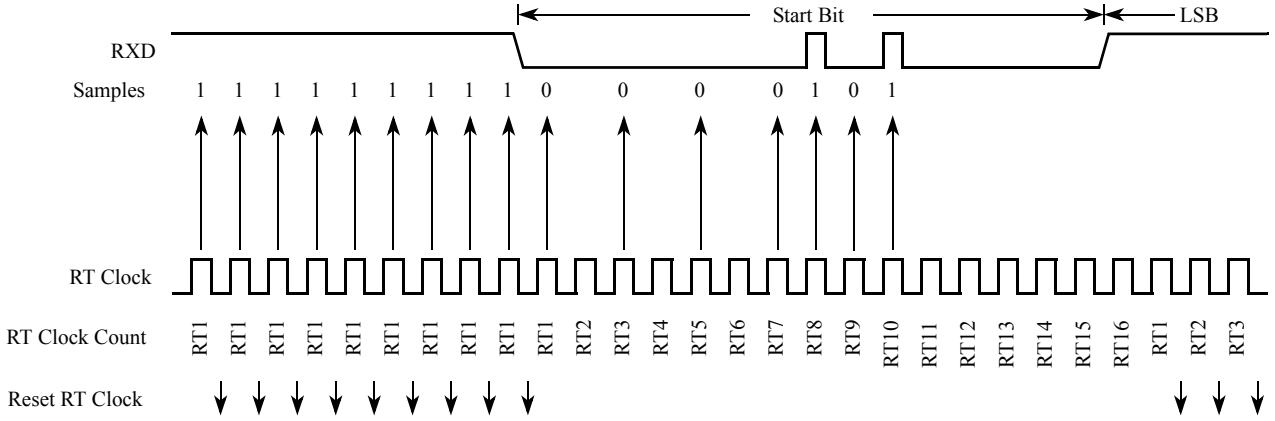


Figure 14-27. Start Bit Search Example 6

14.4.6.4 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming frame, it sets the framing error flag, FE, in SCI status register 1 (SCISR1). A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

Table 17-8. CPIF Register Field Descriptions

Field	Description
5 CLVHIF	**CANL Voltage Failure High Interrupt Flag** This flag is set to 1 when the CPCLVH bit in the CAN Physical Layer Status Register (CPSR) changes. 0 No change in CPCLVH 1 CPCLVH has changed
4 CLVLIF	**CANL Voltage Failure Low Interrupt Flag** This flag is set to 1 when the CPCLVL bit in the CAN Physical Layer Status Register (CPSR) changes. 0 No change in CPCLVL 1 CPCLVL has changed
3 CPDTIF	**CAN CPTXD-Dominant Timeout Interrupt Flag** This flag is set to 1 when CPTXD is dominant longer than $t_{CPTXDDT}$. It signals a timeout event and entry of listen-only mode disabling the transmitter. Exit of listen-only mode which was entered at timeout is requested by clearing CPDTIF when CPDT is clear after setting CPTXD to recessive state. It takes 1 to 2 µs to return to normal mode. If CPTXD is dominant or dominant timeout status is still active (CPDT=1) when clearing the flag, the CAN Physical Layer remains in listen-only mode and this flag is set again after a delay (see 17.5.4.2, “CPTXD-Dominant Timeout Interrupt””). 0 No CPTXD-dominant timeout has occurred 1 CPTXD-dominant timeout has occurred
1 CHOCIF	**CANH Over-Current Interrupt Flag** This flag is set to 1 if an over current condition was detected on CANH when driving a dominant bit to the CAN bus. While this flag is asserted the CAN Physical Layer remains in listen-only mode. 0 Normal current level $I_{CANH} < I_{CANHOC}$ 1 Error event $I_{CANH} \geq I_{CANHOC}$ occurred
0 CLOCIF	**CANL Over-Current Interrupt Flag** This flag is set to 1 if an over current condition was detected on CANL when driving a dominant bit to the CAN bus. While this flag is asserted the CAN Physical Layer remains in listen-only mode. 0 Normal current level $I_{CANL} < I_{CANLOC}$ 1 Error event $I_{CANL} \geq I_{CANLOC}$ occurred

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0008	TXBUF	R	STATCONF[3:0]				CRC[3:0]			
		W								
		R	DATA0[3:0]				DATA1[3:0]			
		W								
0x000A		R	DATA2[3:0]				DATA3[3:0]			
		W								
		R	DATA4[3:0]				DATA5[3:0]			
		W								
0x000C – 0x000F	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

21.7.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register location do not have any effect and reads of these locations return a zero.Details of register bit and field function follow the register diagrams, in bit order.

21.7.2.1 SENT Transmitter Tick Rate Register (TICKRATE)

Module Base + 0x0000 Access: User read/write[1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	PRE[13:0]													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] Read: Anytime.
Write: Anytime, if CONFIG[TXINIT] is one.

Table 21-4. SENT Transmitter Tick Rate Register (TICKRATE) Field Descriptions

Field	Description
13–0 PRE[13:0]	**SENTTX Tick Rate Bits** — The tick rate for the SENTTX module is determined by these 14 bits. The SENT transmitter Tick Rate Register can contain a value from 0 to 16383. It is used to derive the SENT unit-time (UT) from the SENTTX bus clock. The SENT unit-time has an allowable range of 3 to 90 µs. The formula for calculating the tick rate is: SENTTX tick rate = SENTTX bus clock rate / (PRE+1)

Offset Module Base + 0x0016

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 22-28. Flash Common Command Object 5 High Register (FCCOB5HI)

Offset Module Base + 0x0017

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 22-29. Flash Common Command Object 5 Low Register (FCCOB5LO)

22.3.2.13.1 FCCOB - NVM Command Mode

NVM command mode uses the FCCOB registers to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 22-26. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. The value written to the FCCOBIX field must reflect the amount of CCOB words loaded for command execution.

Table 22-26 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in <st-blue>Section 22.4.7 Flash Command Description.

Table 22-26. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	FCCOB0	HI	FCMD[7:0] defining Flash command
		LO	Global address [23:16]
001	FCCOB1	HI	Global address [15:8]
		LO	Global address [7:0]

B.1.1.1 Port AD Output Drivers Switching

PortAD output drivers switching can adversely affect the ADC accuracy whilst converting the analog voltage on other PortAD pins because the output drivers are supplied from the VDDA/VSSA ADC supply pins. Although internal design measures are implemented to minimize the effect of output driver noise, it is recommended to configure PortAD pins as outputs only for low frequency, low load outputs. The impact on ADC accuracy is load dependent and not specified. The values specified are valid under condition that no PortAD output drivers switch during conversion.

B.1.1.2 Source Resistance

Due to the input pin leakage current as specified in conjunction with the source resistance there will be a voltage drop from the signal source to the ADC input. The maximum source resistance R_S specifies results in an error (10-bit resolution) of less than 1/2 LSB (2.5 mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage induced error is acceptable, larger values of source resistance of up to 10Kohm are allowed.

B.1.1.3 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external capacitance and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB (10-bit resolution), then the external filter capacitor, $C_f \geq 1024 * (C_{INS}–C_{INN})$.

B.1.1.4 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (in 10-bit mode) for analog inputs greater than V_{RH} and 0x000 for values less than V_{RL} unless the current is higher than specified as a disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as:

   $$V_{ERR} = K * R_S * I_{INJ}$$

   with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Appendix I
S12CANPHY Electrical Specifications

I.1 Maximum Ratings

Table I-1. Maximum Ratings

Characteristics noted under conditions 5.5V <= VSUP <=18 V >, -40°C <= Tj <= 150°C > unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.				
Num	**Ratings**	**Symbol**	**Value**	**Unit**
1	DC voltage on CANL, CANH, SPLIT	V_{BUS}	-32 to +40	V
2	Continuous current on CANH and CANL	I_{LH}	200	mA
3	ESD on CANH, CANL and SPLIT (HBM)	V_{ESDCH}	± 4000	V
4	ESD on CANH, CANL (IEC61000-4, Czap = 150 pF, Rzap = 330 Ω)	V_{ESDIEC}	± 6000	V

I.2 Static Electrical Characteristics

Table I-2. Static Electrical Characteristics

Characteristics noted under conditions 5.5V <= VSUP <=18 V >, -40°C <= Tj <= 150°C > unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
CAN TRANSCEIVER CURRENT						
1	Supply Current of canphy_ll18uhv Normal mode, Bus Recessive State Normal mode, Bus Dominant State without Bus Load Standby mode Shutdown mode	 I_{RES} I_{DOM} I_{STB} I_{SDN}		 1.7 3.8 0.022 0		mA
PINS (CANH AND CANL)						
2	Bus Pin Common Mode Voltage	V_{COM}	-12	-	12	V
3a	Differential Input Voltage (Normal mode) Recessive State at RXD Dominant State at RXD	 V_{CANH} - V_{CANL}	 -1.0 0.9	 - -	 0.5 5.0	 V V
3b	Differential Input Voltage (Standby mode) Recessive State at RXD Dominant State at RXD	 V_{CANH} - V_{CANL}	 -1.0 1.1	 - -	 0.4 5.0	 V V
4	Differential Input Hysteresis	V_{HYS}		175		mV