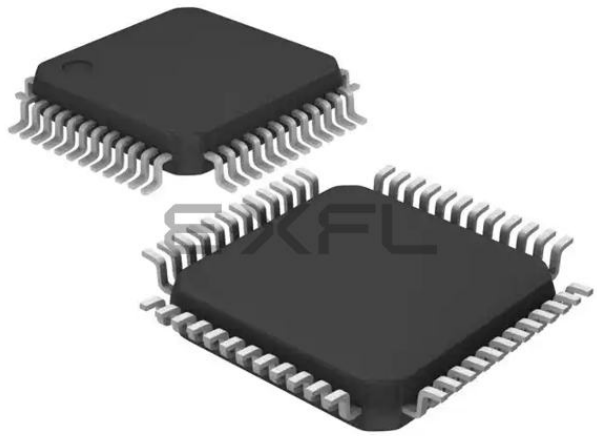

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvca19f0mlf

2.3.1 Register Map

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0200	MODRR0	R	IIC0RR1-0		SCI1RR	SCI0RR	SPI0RR	M0C0RR2-0		
		W								
0x0201	MODRR1	R	T1IC3RR	T1IC2RR	0	0	0	TRIG0NEG	TRIG0RR1-0	
		W								
0x0202	MODRR2	R	P0C7RR	0	0	0	P0C3RR	0	0	0
		W								
0x0203	MODRR3	R	0	0	0	T0IC3RR1	T0IC3RR0	T0IC2RR	T0IC1RR	0
		W								
0x0204–0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	ECLKCTL	R	NECLK	0	0	0	0	0	0	0
		W								
0x0209	IRQCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								
0x020A–0x020D	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x020E	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x020F	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0210–0x025F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0260	PTE	R	0	0	0	0	0	0	PTE1	PTE0
		W								
0x0261	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0262	PTIE	R	0	0	0	0	0	0	PTIE1	PTIE0
		W								
0x0263	Reserved	R	0	0	0	0	0	0	0	0
		W								

3.4.5.2.2 READ_SAME Effects Of Variable Access Size

READ_SAME uses the unadjusted address given in the previous READ_MEM command as a base address for subsequent READ_SAME commands. When the READ_MEM and READ_SAME size parameters differ then READ_SAME uses the original base address buts aligns 32-bit and 16-bit accesses, where those accesses would otherwise cross the aligned 4-byte boundary. Table 3-12 shows some examples of this.

Table 3-12. Consecutive READ_SAME Accesses With Variable Size

Row	Command	Base Address	00	01	10	11
1	READ_MEM.32	0x004003	Accessed	Accessed	Accessed	Accessed
2	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
3	READ_SAME.16	—			Accessed	Accessed
4	READ_SAME.08	—				Accessed
5	READ_MEM.08	0x004000	Accessed			
6	READ_SAME.08	—	Accessed			
7	READ_SAME.16	—	Accessed	Accessed		
8	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
9	READ_MEM.08	0x004002			Accessed	
10	READ_SAME.08	—			Accessed	
11	READ_SAME.16	—			Accessed	Accessed
12	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
13	READ_MEM.08	0x004003				Accessed
14	READ_SAME.08	—				Accessed
15	READ_SAME.16	—			Accessed	Accessed
16	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
17	READ_MEM.16	0x004001		Accessed	Accessed	
18	READ_SAME.08	—		Accessed		
19	READ_SAME.16	—		Accessed	Accessed	
20	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed
21	READ_MEM.16	0x004003			Accessed	Accessed
22	READ_SAME.08	—				Accessed
23	READ_SAME.16	—			Accessed	Accessed
24	READ_SAME.32	—	Accessed	Accessed	Accessed	Accessed

3.4.6 BDC Serial Interface

The BDC communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDC.

The BDC serial interface uses an internal clock source, selected by the CLKSW bit in the BDCCSR register. This clock is referred to as the target clock in the following explanation.

Table 6-4. DBGC2 Field Descriptions

Field	Description
1–0 ABCM[1:0]	**A and B Comparator Match Control** — These bits determine the A and B comparator match mapping as described in Table 6-5.

Table 6-5. ABCM Encoding

ABCM	Description
00	Match0 mapped to comparator A match..... Match1 mapped to comparator B match.
01	Match0 mapped to comparator A/B inside range..... Match1 disabled.
10	Match0 mapped to comparator A/B outside range..... Match1 disabled.
11	Reserved[1]

[1] Currently defaults to Match0 mapped to inside range: Match1 disabled

6.3.2.3 Debug State Control Register 1 (DBGSCR1)

Address: 0x0107

	7	6	5	4	3	2	1	0
R	C3SC1	C3SC0	0	0	C1SC1	C1SC0	C0SC1	C0SC0
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-6. Debug State Control Register 1 (DBGSCR1)

Read: Anytime.

Write: If DBG is not armed.

The state control register 1 selects the targeted next state whilst in State1. The matches refer to the outputs of the comparator match control logic as depicted in Figure 6-1 and described in Section 6.3.2.8, “Debug Comparator A Control Register (DBGACTL)”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 6-7. DBGSCR1 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State1 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State1 following a match1.
7–6 C3SC[1:0]	Channel 3 State Control. If EEVE !=10, these bits select the targeted next state whilst in State1 following a match3. If EEVE = 10, these bits select the targeted next state whilst in State1 following an external event.

Be aware that the output frequency varies with the TC trimming. A frequency trimming correction is therefore necessary. The values provided in Table 8-27 are typical values at ambient temperature which can vary from device to device.

8.3.2.22 S12CPMU_UHV_V7 Oscillator Register (CPMUOSC)

This registers configures the external oscillator (XOSCLCP).

Module Base + 0x001A

	7	6	5	4	3	2	1	0
R	OSCE	0	Reserved	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-31. S12CPMU_UHV_V7 Oscillator Register (CPMUOSC)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010	ADCEOLRI	R	CSL_EOL	RVL_EOL	0	0	0	0	0	0
		W								
0x0011	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	Reserved	Reserved					0	0
		W								
0x0014	ADCCMD_0	R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
		W								
0x0015	ADCCMD_1	R	VRH_SEL	VRL_SEL	CH_SEL[5:0]					
		W								
0x0016	ADCCMD_2	R	SMP[4:0]					0	0	Reserved
		W								
0x0017	ADCCMD_3	R	Reserved	Reserved	Reserved					
		W								
0x0018	Reserved	R	Reserved							
		W								
0x0019	Reserved	R	Reserved							
		W								
0x001A	Reserved	R	Reserved							
		W								
0x001B	Reserved	R	Reserved							
		W								
0x001C	ADCCIDX	R	0	0	CMD_IDX[5:0]					
		W								
0x001D	ADCCBP_0	R	CMD_PTR[23:16]							
		W								
0x001E	ADCCBP_1	R	CMD_PTR[15:8]							
		W								
0x001F	ADCCBP_2	R	CMD_PTR[7:2]						0	0
		W								
0x0020	ADCRIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0021	ADCRBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0022	ADCRBP_1	R	RES_PTR[15:8]							
		W								
0x0023	ADCRBP_2	R	RES_PTR[7:2]						0	0
		W								
0x0024	ADCCROFF0	R	0	CMDRES_OFF0[6:0]						
		W								
0x0025	ADCCROFF1	R	0	CMDRES_OFF1[6:0]						
		W								
0x0026	Reserved	R	0	0	0	0	Reserved			
		W								

= Unimplemented or Reserved

Figure 9-3. ADC12B_LBA Register Summary (Sheet 2 of 3)

9.5.3.2.6 Conversion flow control in case of conversion sequence control bit overrun scenarios

Restart Request Overrun:
If a legal Restart Request is detected and no Restart Event is in progress, the RSTA bit is set due to the request. The set RSTA bit indicates that a Restart Request was detected and the Restart Event is in process. In case further Restart Requests occur while the RSTA bit is set, this is defined a overrun situation. This scenario is likely to occur when bit STR_SEQA is set or when a Restart Event causes a Sequence Abort Event. The request overrun is captured in a background register that always stores the last detected overrun request. Hence if the overrun situation occurs more than once while a Restart Event is in progress, only the latest overrun request is pending. When the RSTA bit is cleared, the latest overrun request is processed and RSTA is set again one cycle later.

LoadOK Overrun:
Simultaneously at any Restart Request overrun situation the LoadOK input is evaluated and the status is captured in a background register which is alternated anytime a Restart Request Overrun occurs while Load OK Request is asserted. The Load OK background register is cleared as soon as the pending Restart Request gets processed.

Trigger Overrun:
If a Trigger occurs whilst bit TRIG is already set, this is defined as a Trigger overrun situation and causes the ADC to cease conversion at the next conversion boundary and to set bit TRIG_EIF. A overrun is also detected if the Trigger Event occurs automatically generated by hardware in “Trigger Mode” due to a Restart Event and simultaneously a Trigger Event is generated via data bus or internal interface. In this case the ADC ceases operation before conversion begins to sample. In “Trigger Mode” a Restart Request Overrun does not cause a Trigger Overrun (bit TRIG_EIF not set).

Sequence Abort Request Overrun:
If a Sequence Abort Request occurs whilst bit SEQA is already set, this is defined as a Sequence Abort Request Overrun situation and the overrun request is ignored.

10.3.2.1 BATS Module Enable Register (BATE)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	BVHS	BVLS[1:0]		BSUAE	BSUSE	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-3. BATS Module Enable Register (BATE)

[1] Read: Anytime
Write: Anytime

Table 10-2. BATE Field Description

Field	Description
6 BVHS	**BATS Voltage High Select** — This bit selects the trigger level for the Voltage Level High Condition (BVHC). 0 Voltage level V_{HBI1} is selected 1 Voltage level V_{HBI2} is selected
5:4 BVLS[1:0]	**BATS Voltage Low Select** — This bit selects the trigger level for the Voltage Level Low Condition (BVLC). 00 Voltage level V_{LBI1} is selected 01 Voltage level V_{LBI2} is selected 10 Voltage level V_{LBI3} is selected 11 Voltage level V_{LBI4} is selected
3 BSUAE	**BATS VSUP ADC Connection Enable** — This bit connects the VSUP pin through the resistor chain to ground and connects the ADC channel to the divided down voltage. 0 ADC Channel is disconnected 1 ADC Channel is connected
2 BSUSE	**BATS VSUP Level Sense Enable** — This bit connects the VSUP pin through the resistor chain to ground and enables the Voltage Level Sense features measuring BVLC and BVHC. 0 Level Sense features disabled 1 Level Sense features enabled

NOTE

When opening the resistors path to ground by changing BSUSE or BSUAE then for a time T_{EN_UNC} + two bus cycles the measured value is invalid. This is to let internal nodes be charged to correct value. BVHIE, BVLIE might be cleared for this time period to avoid false interrupts.

13.2.1 PWM7 - PWM0 — PWM Channel 7 - 0

Those pins serve as waveform output of PWM channel 7 - 0.

13.3 Memory Map and Register Definition

13.3.1 Module Memory Map

This section describes the content of the registers in the scalable PWM module. The base address of the scalable PWM module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. The figure below shows the registers associated with the scalable PWM and their relative offset from the base address. The register detail description follows the order they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

13.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the scalable PWM module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 PWME[1]	R	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
	W								
0x0001 PWMPOL[1]	R	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
	W								
0x0002 PWMCLK[1]	R	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
	W								
0x0003 PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
0x0004 PWMCAE[1]	R	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
	W								
0x0005 PWMCTL[1]	R	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
	W								

= Unimplemented or Reserved

Figure 13-2. The scalable PWM Register Summary (Sheet 1 of 4)

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 13.4.2.5, “Left Aligned Outputs” and Section 13.4.2.6, “Center Aligned Outputs” for more details).

Table 13-12. PWM Timer Counter Conditions

Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

13.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 13-16. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 13-16, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 13.4.2.3, “PWM Period and Duty”. The counter counts from 0 to the value in the period register – 1.

Clock Source = PWM clock, where PWM clock= 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 MHz/8 = 1.25 MHz

PWMx Period = 800 ns

PWMx Duty Cycle = 3/4 *100% = 75%

Shown in Figure 13-20 is the output waveform generated.

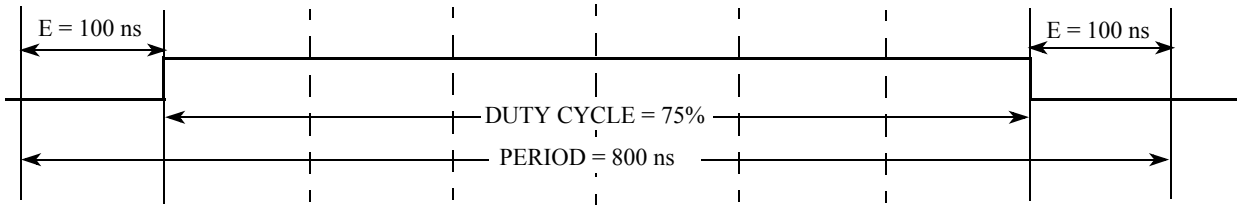

Figure 13-20. PWM Center Aligned Output Example Waveform

13.4.2.7 PWM 16-Bit Functions

The scalable PWM timer also has the option of generating up to 8-channels of 8-bits or 4-channels of 16-bits for greater PWM resolution. This 16-bit channel option is achieved through the concatenation of two 8-bit channels.

The PWMCTL register contains four control bits, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. Channels 6 and 7 are concatenated with the CON67 bit, channels 4 and 5 are concatenated with the CON45 bit, channels 2 and 3 are concatenated with the CON23 bit, and channels 0 and 1 are concatenated with the CON01 bit.

NOTE

Change these bits only when both corresponding channels are disabled.

When channels 6 and 7 are concatenated, channel 6 registers become the high order bytes of the double byte channel, as shown in Figure 13-21. Similarly, when channels 4 and 5 are concatenated, channel 4 registers become the high order bytes of the double byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high order bytes of the double byte channel.

When using the 16-bit concatenated mode, the clock source is determined by the low order 8-bit channel clock select control bits. That is channel 7 when channels 6 and 7 are concatenated, channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low order 8-bit channel as also shown in Figure 13-21. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low order 8-bit channel as well.

16.4.1.11 General Call Address

To broadcast using a general call, a device must first generate the general call address($00), then after receiving acknowledge, it must transmit data.

In communication, as a slave device, provided the GCEN is asserted, a device acknowledges the broadcast and receives data until the GCEN is disabled or the master device releases the bus or generates a new transfer. In the broadcast, slaves always act as receivers. In general call, IAAS is also used to indicate the address match.

In order to distinguish whether the address match is the normal address match or the general call address match, IBDR should be read after the address byte has been received. If the data is $00, the match is general call address match. The meaning of the general call address is always specified in the first data byte and must be dealt with by S/W, the IIC hardware does not decode and process the first data byte.

When one byte transfer is done, the received data can be read from IBDR. The user can control the procedure by enabling or disabling GCEN.

16.4.2 Operation in Run Mode

This is the basic mode of operation.

16.4.3 Operation in Wait Mode

IIC operation in wait mode can be configured. Depending on the state of internal bits, the IIC can operate normally when the CPU is in wait mode or the IIC clock generation can be turned off and the IIC module enters a power conservation state during wait mode. In the later case, any transmission or reception in progress stops at wait mode entry.

16.4.4 Operation in Stop Mode

The IIC is inactive in stop mode for reduced power consumption. The STOP instruction does not affect IIC register states.

16.5 Resets

The reset state of each individual bit is listed in Section 16.3, “Memory Map and Register Definition,” which details the registers and their bit-fields.

16.6 Interrupts

IICV3 uses only one interrupt vector.

Table 16-11. Interrupt Summary

Interrupt	Offset	Vector	Priority	Source	Description
IIC Interrupt	—	—	—	IBAL, TCF, IAAS bits in IBSR register	When either of IBAL, TCF or IAAS bits is set may cause an interrupt based on arbitration lost, transfer complete or address detect conditions

[1] Read: or transmit buffers: Anytime when TXEx flag is set (see Section 18.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”) and the corresponding transmit buffer is selected in CANTBSEL (see Section 18.3.2.11, “MSCAN Transmit Buffer Selection Register (CANTBSEL)”). For receive buffers: Anytime when RXF is set.
Write: Unimplemented

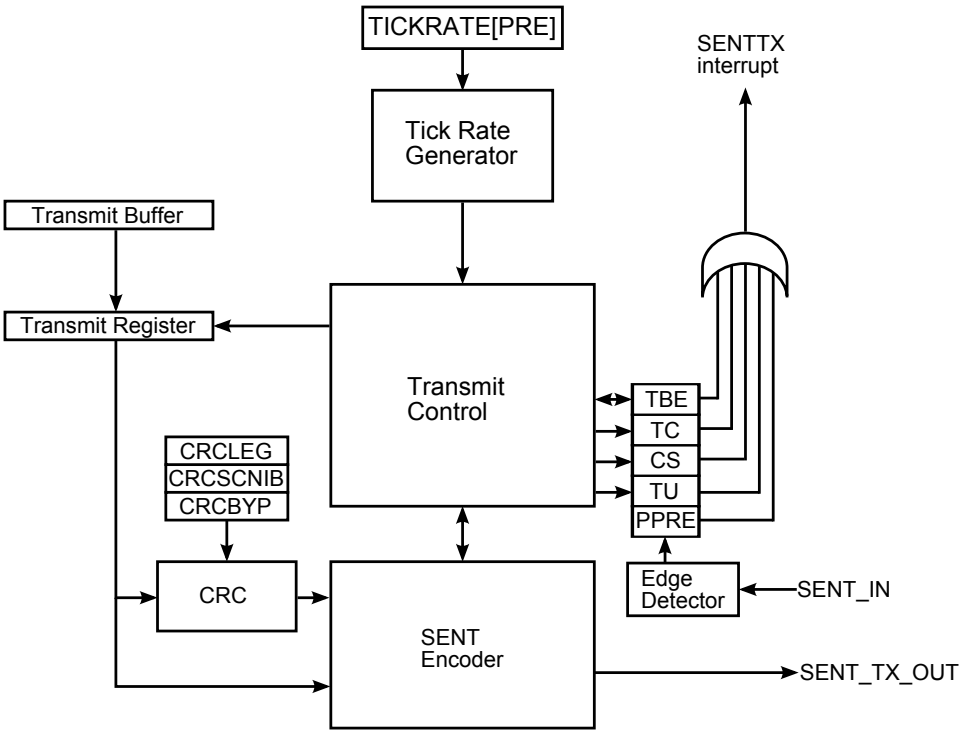

Figure 21-1. SENTTX Block Diagram

21.5 External Signals

The SENTTX module has two external signals.

21.5.1 SENT_TX_OUT - SENT Transmitter Output

The SENT_TX_OUT signal is the transmitter output signal.

21.5.2 SENT_IN - SENT Transmitter Input

The SENT_IN signal is used as a feedback input to compensate for the output delay on the transmitter output. This signal is used to detect when the Pause pulse rising-edge appears on the external pin.

21.6 Modes of Operation

- Run mode

  This is the basic mode of operation.
- Wait mode

  Wait mode does not affect the function of the SENTTX module. Operation is the same as in Run mode.
- Stop mode

Address Offset	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0008	TXBUF	R	STATCONF[3:0]				CRC[3:0]			
		W								
		R	DATA0[3:0]				DATA1[3:0]			
		W								
0x000A		R	DATA2[3:0]				DATA3[3:0]			
		W								
		R	DATA4[3:0]				DATA5[3:0]			
		W								
0x000C – 0x000F	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

21.7.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register location do not have any effect and reads of these locations return a zero.Details of register bit and field function follow the register diagrams, in bit order.

21.7.2.1 SENT Transmitter Tick Rate Register (TICKRATE)

Module Base + 0x0000 Access: User read/write[1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	PRE[13:0]													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] Read: Anytime.
Write: Anytime, if CONFIG[TXINIT] is one.

Table 21-4. SENT Transmitter Tick Rate Register (TICKRATE) Field Descriptions

Field	Description
13–0 PRE[13:0]	**SENTTX Tick Rate Bits** — The tick rate for the SENTTX module is determined by these 14 bits. The SENT transmitter Tick Rate Register can contain a value from 0 to 16383. It is used to derive the SENT unit-time (UT) from the SENTTX bus clock. The SENT unit-time has an allowable range of 3 to 90 µs. The formula for calculating the tick rate is: SENTTX tick rate = SENTTX bus clock rate / (PRE+1)

Field	Description
7–4 DATA4[3:0]	**SENTTX Data Nibble 4** — These bits represent data which is sent as the fifth SENT protocol data nibble, if enabled by the data nibble count bits in the SENTTX CONFIG register (CONFIG[DNIBBLECOUNT]>=5).
3–0 DATA5[3:0]	**SENTTX Data Nibble 5** — These bits represent data which is sent as the sixth SENT protocol data nibble, if enabled by the data nibble count bits in the SENTTX CONFIG register (CONFIG[DNIBBLECOUNT]=6).

21.8 Functional Description

This section provides a complete functional description of the SENTTX module, describing the operation of the design in a number of subsections.

21.8.1 Message Format

The SENTTX module uses the standard SENT message format. The transmitted information is encoded into the distance between two consecutive falling edges. A message consists of:

1. One calibration/synchronization pulse period with a length of 56 unit-time (UT) ticks.
2. One status and serial communication nibble pulse period with a length of 12 to 27 UT ticks.
3. One to six data nibble pulse periods with a length of 12 to 27 UT ticks each.
4. One CRC nibble pulse period with a length of 12 to 27 UT ticks.
5. An optional pause pulse.

Figure 21-2 below shows an example of a SENT message (not drawn to scale).

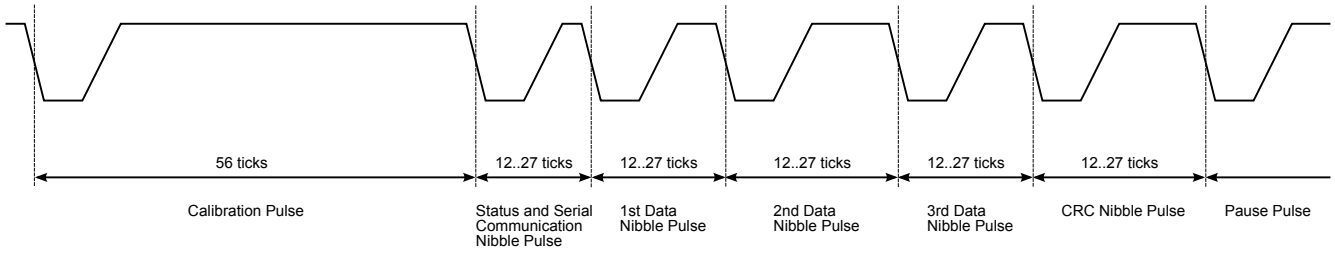

Figure 21-2. SENT Message Format

The number of transmitted data nibbles (1 to 6) is controlled by the data nibble count bits in the Configuration Register (CONFIG[DNIBBLECOUNT]).

The CRC nibble can be supplied using one of the following three methods:

1. Hardware calculates the CRC nibble from the transmitted data nibbles using the SENT recommended method (CONFIG[CRCLEG]=0, CONFIG[CRCBYP]=0).
2. Hardware calculates the CRC nibble from the transmitted data nibbles using the SENT legacy method (CONFIG[CRCLEG]=1, CONFIG[CRCBYP]=0).
3. The CRC nibble can be supplied by software, together with the status and serial communication nibble and the data nibbles in the Transmit Buffer (CONFIG[CRCBYP]=1).

Table 22-40. Program P-Flash Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x06	Global address [23:16] to identify P-Flash block
FCCOB1	Global address [15:0] of phrase location to be programmed[1]	
FCCOB2	Word 0 program value	
FCCOB3	Word 1 program value	
FCCOB4	Word 2 program value	
FCCOB5	Word 3 program value	

1 Global address [2:0] must be 000

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

Table 22-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

22.4.7.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in <st-blue>Section 22.4.7.4 Read Once Command. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 22-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
FCCOB0	0x07	Not Required
FCCOB1	Program Once phrase index (0x0000 - 0x0007)	
FCCOB2	Program Once word 0 value	
FCCOB3	Program Once word 1 value	

Table A-3. ESD and Latch-up Test Conditions

Model	Spec	Description	Symbol	Value	Unit
Human Body	JESD22-A114	Series Resistance	R	1500	Ω
		Storage Capacitance	C	100	pF
		Number of Pulse per pin positive negative	-	- 1 1	
Charged-Device	JESD22-C101	Series Resistance	R	0	Ω
		Storage Capacitance	C	4	pF
Latch-up for 5V GPIOs		Minimum Input Voltage Limit		-2.5	V
		Maximum Input Voltage Limit		+7.5	V
Latch-up for BCTL/BCTLC/ CANH/CANL /SPLIT		Minimum Input Voltage Limit		-7	V
		Maximum Input Voltage Limit		+21	V

Table A-4. ESD Protection and Latch-up Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM): -all pins except CANH/CANL/SPLIT/HVI -CANH/CANL/SPLIT/HVI	V_{HBM}	 +/-2 +/-4	-	KV
2	Charged-Device Model (CDM): Corner Pins	V_{CDM}	+/-750	-	V
3	Charged-Device Model (CDM): all other pins	V_{CDM}	+/-500	-	V
4	Direct Contact Discharge IEC61000-4-2 with and without 220nF capacitor (R=330, C=150pF) CANL and CANH	V_{ESDIEC}	+/-6		KV
5	Latch-up Current of 5V GPIOs at T=125°C positive negative	I_{LAT}	 +100 -100	-	mA
6	Latch-up Current of 5V GPIOs at 27°C positive negative	I_{LAT}	 +200 -200	-	mA

A.1.6 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted these conditions apply to the following electrical parameters.

at Tj=-40 °C. The code is executed from RAM. The result is programmed to the IFR, otherwise there is no flash activity.

Table A-16. Measurement Conditions

Description	Symbol	Max	Unit
Regulator Supply Voltage at VSUP	V_{SUP}	5	V
Supply Voltage at VDDX and VDDA	$V_{DDX,A}$	5	V
ADC reference voltage high	V_{RH}	5	V
ADC reference voltage low	V_{RL}	0	V
ADC clock	f_{ATDCLK}	2	MHz
ADC sample time	t_{SMP}	4	ADC clock cycles
Bus clock frequency	f_{bus}	48	MHz
Junction temperature	T_j	-40 and 150	°C

Appendix F
BATS Electrical Specifications

F.1 Static Electrical Characteristics

Table F-1. Static Electrical Characteristics - BATS (Junction Temperature From -40°C To +150°C)

Characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[1] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Low Voltage Warning (LBI 1) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI1_A} V_{LBI1_D} V_{LBI1_H}	 4.75 – –	 5.5 – 0.4	 6 6.5 –	 V V V
2	Low Voltage Warning (LBI 2) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI2_A} V_{LBI2_D} V_{LBI2_H}	 6 – –	 6.75 – 0.4	 7.25 7.75 –	 V V V
3	Low Voltage Warning (LBI 3) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI3_A} V_{LBI3_D} V_{LBI3_H}	 7 – –	 7.75 – 0.4	 8.5 9 –	 V V V
4	Low Voltage Warning (LBI 4) Assert (Measured on VSUP pin, falling edge) Deassert (Measured on VSUP pin, rising edge) Hysteresis (measured on VSUP pin)	 V_{LBI4_A} V_{LBI4_D} V_{LBI4_H}	 8 – –	 9 – 0.4	 10 10.5 –	 V V V
5	High Voltage Warning (HBI 1) Assert (Measured on VSUP pin, rising edge) Deassert (Measured on VSUP pin, falling edge) Hysteresis (measured on VSUP pin)	 V_{HBI1_A} V_{HBI1_D} V_{HBI1_H}	 14.5 14.0 –	 16.5 – 1.0	 18 – –	 V V V
6	High Voltage Warning (HBI 2) Assert (Measured on VSUP pin, rising edge) Deassert (Measured on VSUP pin, falling edge) Hysteresis (measured on VSUP pin)	 V_{HBI2_A} V_{HBI2_D} V_{HBI2_H}	 25 24 –	 27.5 – 1.0	 30 – –	 V V V
7	Pin Input Divider Ratio[2] $Ratio_{VSUP} = V_{SUP} / V_{ADC}$ 5.5V < VSUP < 29 V	$Ratio_{VSUP}$	–	9	–	–
8	Analog Input Matching Absolute Error on V_{ADC} - compared to V_{SUP} / $Ratio_{VSUP}$	$AI_{Matching}$	–	+-2%	+-5%	–

1 T_A: Ambient Temperature

2 V_{ADC}: Voltage accessible at the ADC input channel

Figure L-5. 48 LQFP Package

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932–03	14 APR 2005
	STANDARD: JEDEC MS–026–BBC	

Figure L-6.