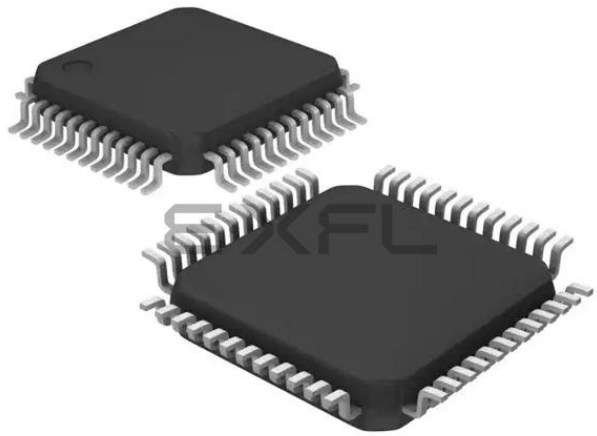

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 10x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvca19f0vlfr

Chapter 1
Device Overview MC9S12ZVC-Family

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Substantial Change(s)
V0.01	9-April-2013	• Initial Version
V0.02	22-August-2013	• Added Section 1.13.3 Flash IFR Mapping • Updated Section 1.14.1 ADC Calibration
V0.03	10-September-2013	• Added Table 1-3 • Added S12ZVCA and S12ZVC Table 1-1
V0.04	7-February-2014	• Added 12K RAM, new maskset and part ID, feedback from shared review
V0.05	6-March-2014	• Changed maskset N23N • Changed Package 48 LQFP without EP
V0.06	28-April-2014	• Removed VRL functionality from PAD4

1.1 Introduction

The MC9S12ZVC-Family is a new member of the S12 MagniV product line integrating a battery level (12V) voltage regulator, supply voltage monitoring, high voltage inputs and a CAN physical interface. It's primarily targeting at CAN nodes like sensors, switch panels or small actuators. It offers various low-power modes and wakeup management to address state of the art power consumption requirements.

Some members of the MC9S12ZVC-Family are also offered for high temperature applications requiring AEC-Q100 Grade 0 (-40°C to +150°C ambient operating temperature range).

The MC9S12ZVC-Family is based on the enhanced performance, linear address space S12Z core and delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings.

1.2 Features

This section describes the key features of the MC9S12ZVC-Family. It documents the superset of features within the family. Section 1.2.1 MC9S12ZVC-Family Comparison provides information to help access the correct information for a particular part within the family.

1.4.1 S12Z Central Processor Unit (CPU)

The S12Z CPU is a revolutionary high-speed core, with code size and execution efficiencies over the S12X CPU. The S12Z CPU also provides a linear memory map eliminating the inconvenience and performance impact of page swapping.

- Harvard Architecture - parallel data and code access
- 3-stage pipeline
- 32-bit wide instruction and databus
- 32-bit ALU
- 24-bit addressing (16 MB linear address space)
- Instructions and Addressing modes optimized for C-Programming and Compiler
  - MAC unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

1.4.1.1 Background Debug Controller (BDC)

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compare the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus onlyEach comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax

2.3.4.10 Port L ADC Connection Enable Register (PTAENL)

Address 0x033D Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PTAENL1	PTAENL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-30. Port L ADC Connection Enable Register (PTAENL)

[1] Read: Anytime
Write: Anytime

Table 2-30. PTAENL Register Field Descriptions

Field	Description
1-0 PTAENL 1-0	**Port L ADC Connection Enable —** This bit enables the analog signal link to an ADC channel. If set to 1 the analog input function takes precedence over the digital input in run mode by forcing off the input buffer if not overridden by PTTEL=1. **Note:** When enabling the resistor paths to ground by setting PTAENL=1, a delay of t_{UNC_HVI} + two bus cycles must be accounted for. 1 ADC connection enabled 0 ADC connection disabled

2.3.4.11 Port L Input Divider Ratio Selection Register (PIRL)

Address 0x033E Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PIRL1	PIRL0
W								
Reset	0	0	0	0	0	0	0	0

Figure 2-31. Port L Input Divider Ratio Selection Register (PIRL)

[1] Read: Anytime
Write: Anytime

Table 2-31. PIRL Register Field Descriptions

Field	Description
1-0 PIRL1-0	**Port L Input Divider Ratio Select —** This bit selects one of two voltage divider ratios for the associated HVI pin in analog mode. 1 $Ratio_{L\_HVI}$ selected 0 $Ratio_{H\_HVI}$ selected

Read: All modes through BDC operation only.

Write: All modes through BDC operation only, when not secured, but subject to the following:

- Bits 7,3 and 2 can only be written by WRITE_BDCCSR commands.
- Bit 5 can only be written by WRITE_BDCCSR commands when the device is not in stop mode.
- Bits 6, 1 and 0 cannot be written. They can only be updated by internal hardware.

Table 3-5. BDCCSRH Field Descriptions

Field	Description
7 ENBDC	**Enable BDC** — This bit controls whether the BDC is enabled or disabled. When enabled, active BDM can be entered and non-intrusive commands can be carried out. When disabled, active BDM is not possible and the valid command set is restricted. Further information is provided in Table 3-7. 0 BDC disabled 1 BDC enabled **Note:** ENBDC is set out of reset in special single chip mode.
6 BDMACT	**BDM Active Status** — This bit becomes set upon entering active BDM. BDMACT is cleared as part of the active BDM exit sequence. 0 BDM not active 1 BDM active **Note:** BDMACT is set out of reset in special single chip mode.
5 BDCCIS	**BDC Continue In Stop** — If ENBDC is set then BDCCIS selects the type of BDC operation in stop mode (as shown in Table 3-3). If ENBDC is clear, then the BDC has no effect on stop mode and no BDC communication is possible.If ACK pulse handshaking is enabled, then the first ACK pulse following stop mode entry is a long ACK. This bit cannot be written when the device is in stop mode. 0 Only the BDCSI clock continues in stop mode 1 All clocks continue in stop mode
3 STEAL	**Steal enabled with ACK**— This bit forces immediate internal accesses with the ACK handshaking protocol enabled. If ACK handshaking is disabled then BDC accesses steal the next bus cycle. 0 If ACK is enabled then BDC accesses await a free cycle, with a timeout of 512 cycles 1 If ACK is enabled then BDC accesses are carried out in the next bus cycle
2 CLKSW	**Clock Switch** — The CLKSW bit controls the BDCSI clock source. This bit is initialized to “0” by each reset and can be written to “1”. Once it has been set, it can only be cleared by a reset. When setting CLKSW a minimum delay of 150 cycles at the initial clock speed must elapse before the next command can be sent. This guarantees that the start of the next BDC command uses the new clock for timing subsequent BDC communications. 0 BDCCLK used as BDCSI clock source 1 Device fast clock used as BDCSI clock source **Note:** Refer to the device specification to determine which clock connects to the BDCCLK and fast clock inputs.
1 UNSEC	**Unsecure** — If the device is unsecure, the UNSEC bit is set automatically. 0 Device is secure. 1 Device is unsecure. **Note:** When UNSEC is set, the device is unsecure and the state of the secure bits in the on-chip Flash EEPROM can be changed.
0 ERASE	**Erase Flash** — This bit can only be set by the dedicated ERASE_FLASH command. ERASE is unaffected by write accesses to BDCCSR. ERASE is cleared either when the mass erase sequence is completed, independent of the actual status of the flash array or by a soft reset. Reading this bit indicates the status of the requested mass erase sequence. 0 No flash mass erase sequence pending completion 1 Flash mass erase sequence pending completion.

Table 6-15. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
000	State0 (disarmed)
001	State1
010	State2
011	State3
100	Final State
101,110,111	Reserved

6.3.2.8 Debug Comparator A Control Register (DBGACTL)

Address: 0x0110

	7	6	5	4	3	2	1	0
R	0	NDB	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-11. Debug Comparator A Control Register

Read: Anytime.

Write: If DBG not armed.

Table 6-16. DBGACTL Field Descriptions

Field	Description
6 NDB	**Not Data Bus** — The NDB bit controls whether the match occurs when the data bus matches the comparator register value or when the data bus differs from the register value. This bit is ignored if the INST bit in the same register is set. 0 Match on data bus equivalence to comparator register contents 1 Match on data bus difference to comparator register contents
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored when INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 8-6. CPMUCLKS Descriptions

Field	Description
7 PLLSEL	**PLL Select Bit** This bit selects the PLLCLK as source of the System Clocks (Core Clock and Bus Clock). PLLSEL can only be set to 0, if UPOSC=1. UPOSC= 0 sets the PLLSEL bit. Entering Full Stop Mode sets the PLLSEL bit. 0 System clocks are derived from OSCCLK if oscillator is up (UPOSC=1, $f_{bus} = f_{osc} / 2$). 1 System clocks are derived from PLLCLK, $f_{bus} = f_{PLL} / 2$.
6 PSTP	**Pseudo Stop Bit** This bit controls the functionality of the oscillator during Stop Mode. 0 Oscillator is disabled in Stop Mode (Full Stop Mode). 1 Oscillator continues to run in Stop Mode (Pseudo Stop Mode), option to run RTI and COP. **Note:** Pseudo Stop Mode allows for faster STOP recovery and reduces the mechanical stress and aging of the resonator in case of frequent STOP conditions at the expense of a slightly increased power consumption. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.
5 CSAD	**COP in Stop Mode ACLK Disable** — This bit disables the ACLK for the COP in Stop Mode. Hence the COP is static while in Stop Mode and continues to operate after exit from Stop Mode. Due to clock domain crossing synchronization there is a latency time to enter and exit Stop Mode if COP clock source is ACLK and this clock is stopped in Stop Mode. This maximum latency time is 4 ACLK cycles which must be added to the Stop Mode recovery time tSTP_REC from exit of current Stop Mode to entry of next Stop Mode. This latency time occurs no matter which Stop Mode (Full, Pseudo) is currently exited or entered next. After exit from Stop Mode (Pseudo, Full) for 2 ACLK cycles no Stop Mode request (STOP instruction) should be generated to make sure the COP counter increments at each Stop Mode exit. This bit does not influence the ACLK for the API. 0 COP running in Stop Mode (ACLK for COP enabled in Stop Mode). 1 COP stopped in Stop Mode (ACLK for COP disabled in Stop Mode)
4 COP OSCSEL1	**COP Clock Select 1** — COPOSCSEL0 and COPOSCSEL1 combined determine the clock source to the COP (see also Table 8-7). If COPOSCSEL1 = 1, COPOSCSEL0 has no effect regarding clock select and changing the COPOSCSEL0 bit does not re-start the COP time-out period. COPOSCSEL1 selects the clock source to the COP to be either ACLK (derived from trimmable internal RC-Oscillator) or clock selected via COPOSCSEL0 (IRCCLK or OSCCLK). Changing the COPOSCSEL1 bit re-starts the COP time-out period. COPOSCSEL1 can be set independent from value of UPOSC. UPOSC= 0 does not clear the COPOSCSEL1 bit. 0 COP clock source defined by COPOSCSEL0 1 COP clock source is ACLK derived from a trimmable internal RC-Oscillator
3 PRE	**RTI Enable During Pseudo Stop Bit** — PRE enables the RTI during Pseudo Stop Mode. 0 RTI stops running during Pseudo Stop Mode. 1 RTI continues running during Pseudo Stop Mode if RTIOSCSEL=1. **Note:** If PRE=0 or RTIOSCSEL=0 then the RTI will go static while Stop Mode is active. The RTI counter will not be reset.
2 PCE	**COP Enable During Pseudo Stop Bit** — PCE enables the COP during Pseudo Stop Mode. 0 COP stops running during Pseudo Stop Mode 1 COP continues running during Pseudo Stop Mode if COPOSCSEL=1 **Note:** If PCE=0 or COPOSCSEL=0 then the COP will go static while Stop Mode is active. The COP counter will not be reset.

9.8.3 List Usage — CSL double buffer mode and RVL double buffer mode

In this use case both list types are configured for double buffer mode (CSL_BMOD=1’b1 and RVL_BMOD=1’b1) and whenever a Command Sequence List (CSL) is finished or aborted the command Sequence List is swapped by the simultaneous assertion of bits LDOK and RSTA.

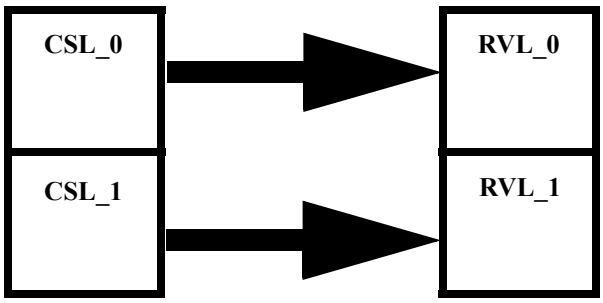


Figure 9-37. CSL Double Buffer Mode — RVL Double Buffer Mode Diagram

This use case can be used if the channel order or CSL length varies very frequently in an application.

9.8.4 List Usage — CSL double buffer mode and RVL single buffer mode

In this use case the CSL is configured for double buffer mode (CSL_BMOD=1’b1) and the RVL is configured for single buffer mode (RVL_BMOD=1’b0).

The two command lists can be different sizes and the allocated result list memory area in the RAM must be able to hold as many entries as the larger of the two command lists. Each time when the end of a Command Sequence List is reached, if bits LDOK and RSTA are set, the commands list is swapped.

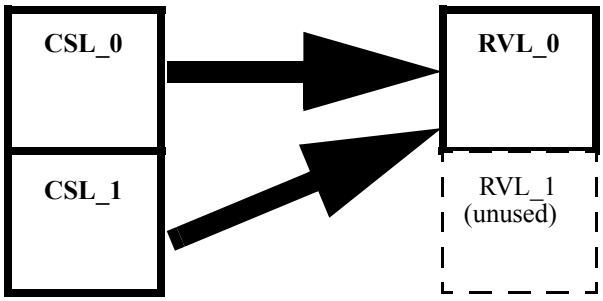


Figure 9-38. CSL Double Buffer Mode — RVL Single Buffer Mode Diagram

Table 11-19. Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the ÷64 clock is generated by the timer prescaler.

Table 11-20. Timer Clock Selection

CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer Figure 11-30**.**

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

11.3.2.16 Pulse Accumulator Flag Register (PAFLG)

[1] .

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 11-25. Pulse Accumulator Flag Register (PAFLG)

Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register. Timer module or Pulse Accumulator must stay enabled (TEN=1 or PAEN=1) while clearing these bits.

11.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

11.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

11.5 Resets

The reset state of each individual bit is listed within Section 11.3, “Memory Map and Register Definition” which details the registers and their bit fields

11.6 Interrupts

This section describes interrupts originated by the TIM16B8CV3 block. Table 11-25 lists the interrupts generated by the TIM16B8CV3 to communicate with the MCU.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

Wait: The prescaler keeps on running, unless PSWAI in PWMCTL is set to 1.

Freeze: The prescaler keeps on running, unless PFRZ in PWMCTL is set to 1.

13.1.3 Block Diagram

Figure 13-1 shows the block diagram for the 8-bit up to 8-channel scalable PWM block.

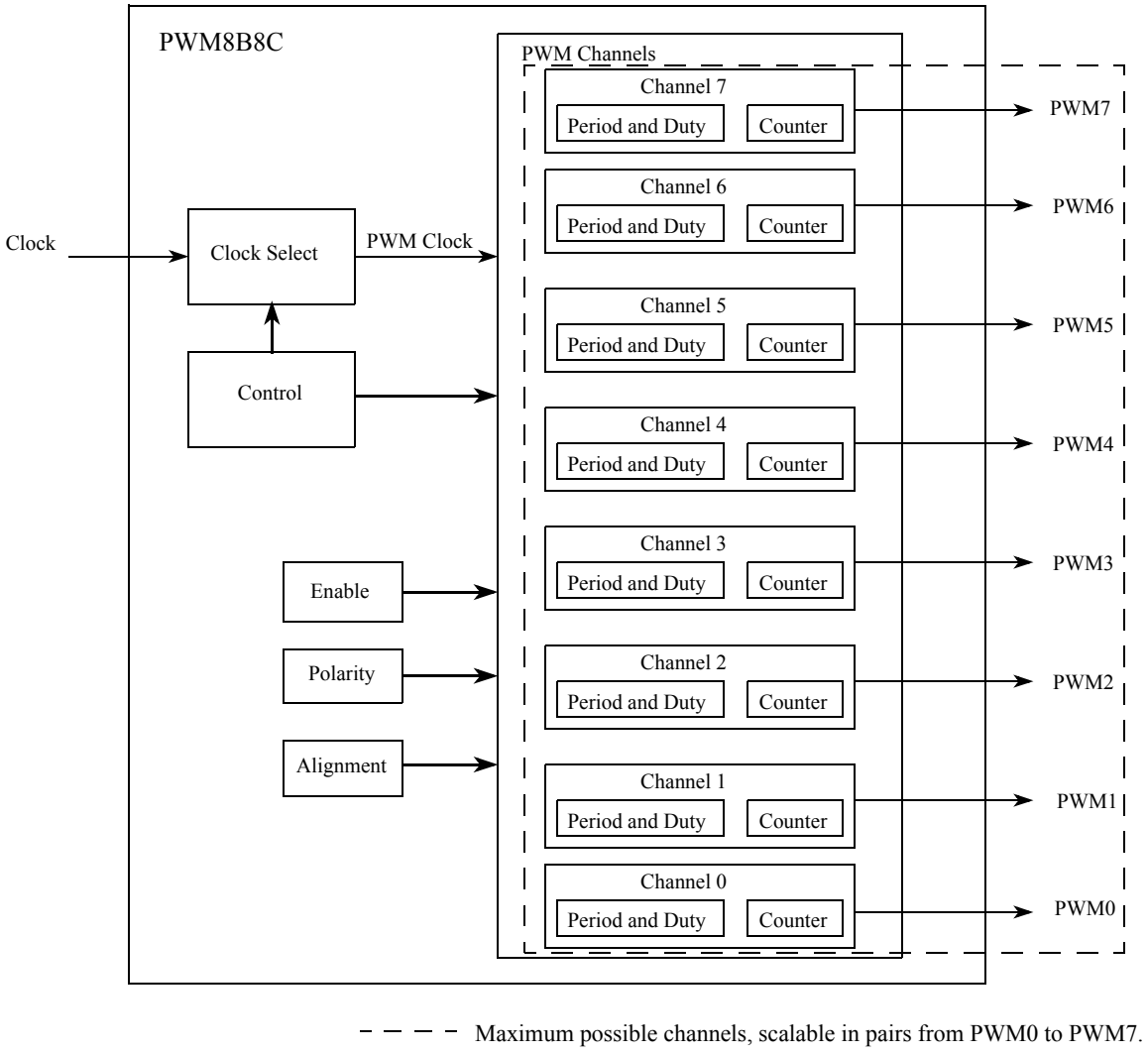


Figure 13-1. Scalable PWM Block Diagram

13.2 External Signal Description

The scalable PWM module has a selected number of external pins. Refer to device specification for exact number.

Table 16-4. I-Bus Tap and Prescale Values

IBC2-0 (bin)	SCL Tap (clocks)	SDA Tap (clocks)
000	5	1
001	6	1
010	7	2
011	8	2
100	9	3
101	10	3
110	12	4
111	15	4

Table 16-5. Prescale Divider Encoding

IBC5-3 (bin)	scl2start (clocks)	scl2stop (clocks)	scl2tap (clocks)	tap2tap (clocks)
000	2	7	4	1
001	2	7	4	2
010	2	9	6	4
011	6	9	6	8
100	14	17	14	16
101	30	33	30	32
110	62	65	62	64
111	126	129	126	128

Table 16-6. Multiplier Factor

IBC7-6	MUL
00	01
01	02
10	04
11	RESERVED

The number of clocks from the falling edge of SCL to the first tap (Tap[1]) is defined by the values shown in the scl2tap column of Table 16-4, all subsequent tap points are separated by 2^{IBC5-3} as shown in the tap2tap column in Table 16-5. The SCL Tap is used to generated the SCL period and the SDA Tap is used to determine the delay from the falling edge of SCL to SDA changing, the SDA hold time.

IBC7–6 defines the multiplier factor MUL. The values of MUL are shown in the Table 16-6.

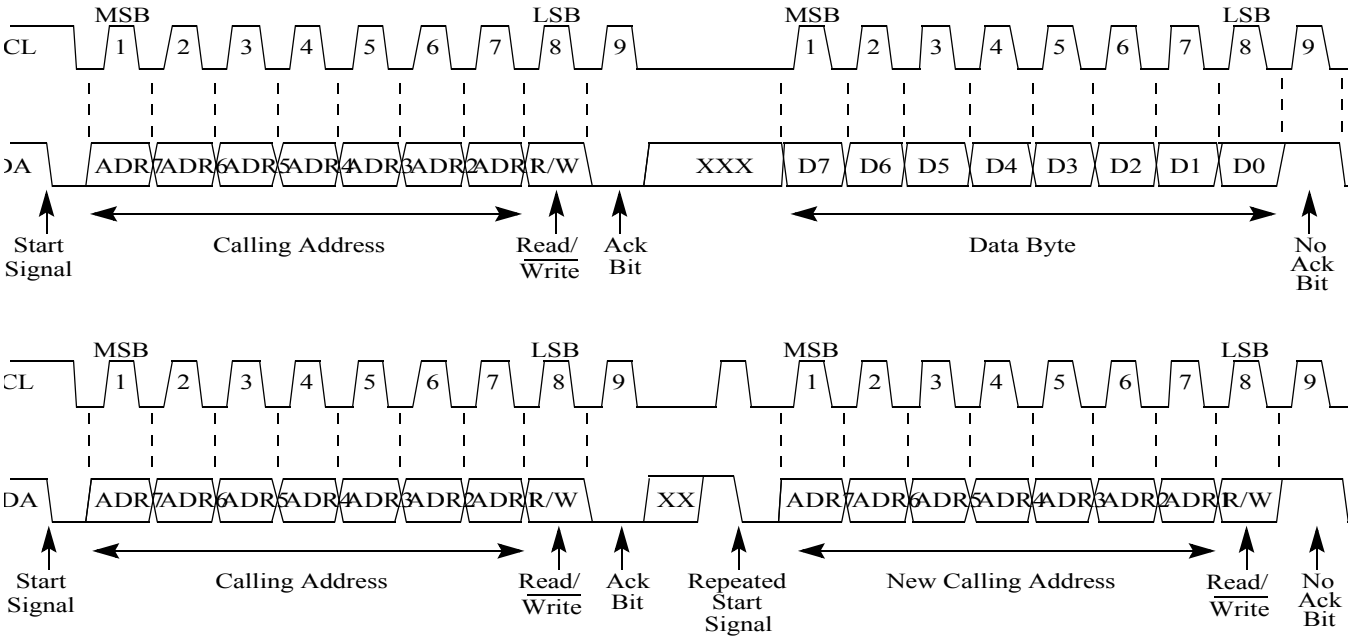


Figure 16-10. IIC-Bus Transmission Signals

16.4.1.1 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCL and SDA lines are at logical high), a master may initiate communication by sending a START signal.As shown in Figure 16-10, a START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

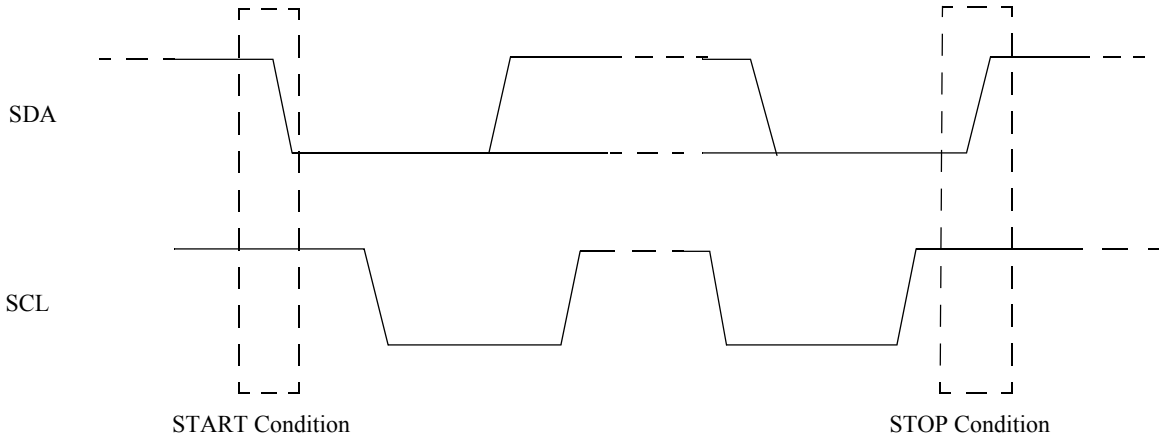


Figure 16-11. Start and Stop Conditions

Table 18-17. CANIDAC Register Field Descriptions

Field	Description
5-4 IDAM[1:0]	**Identifier Acceptance Mode** — The CPU sets these flags to define the identifier acceptance filter organization (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-18 summarizes the different settings. In filter closed mode, no message is accepted such that the foreground buffer is never reloaded.
2-0 IDHIT[2:0]	Identifier Acceptance Hit Indicator — The MSCAN sets these flags to indicate an identifier acceptance hit (see Section 18.4.3, “Identifier Acceptance Filter”). Table 18-19 summarizes the different settings.

Table 18-18. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32-bit acceptance filters
0	1	Four 16-bit acceptance filters
1	0	Eight 8-bit acceptance filters
1	1	Filter closed

Table 18-19. Identifier Acceptance Hit Indication

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit
0	0	0	Filter 0 hit
0	0	1	Filter 1 hit
0	1	0	Filter 2 hit
0	1	1	Filter 3 hit
1	0	0	Filter 4 hit
1	0	1	Filter 5 hit
1	1	0	Filter 6 hit
1	1	1	Filter 7 hit

The IDHITx indicators are always related to the message in the foreground buffer (RxFG). When a message gets shifted into the foreground buffer of the receiver FIFO the indicators are updated as well.

18.3.2.13 MSCAN Reserved Register

This register is reserved for factory testing of the MSCAN module and is not available in normal system operating modes.

Address & Name		7	6	5	4	3	2	1	0
0x0002 FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
	W								
0x0003 FPSTAT	R	FPOVRD	0	0	0	0	0	0	WSTATACK
	W								
0x0004 FCNFG	R	CCIE	0	ERSAREQ	IGNSF	WSTAT[1:0]		FDFD	FSFD
	W								
0x0005 FERCNFG	R	0	0	0	0	0	0	0	SFDIE
	W								
0x0006 FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
0x0007 FERSTAT	R	0	0	0	0	0	0	DFDF	SFDIF
	W								
0x0008 FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
	W								
0x0009 DFPROT	R	DPOPEN	0	DPS5	DPS4	DPS3	DPS2	DPS1	DPS0
	W								
0x000A FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
0x000B FRSV1	R	0	0	0	0	0	0	0	0
	W								
0x000C FCCOB0HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000D FCCOB0LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
0x000E FCCOB1HI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
0x000F FCCOB1LO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								

Figure 22-4. FTMRZ192K2K Register Summary (continued)

Table 22-26. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
010	FCCOB2	HI	Data 0 [15:8]
		LO	Data 0 [7:0]
011	FCCOB3	HI	Data 1 [15:8]
		LO	Data 1 [7:0]
100	FCCOB4	HI	Data 2 [15:8]
		LO	Data 2 [7:0]
101	FCCOB5	HI	Data 3 [15:8]
		LO	Data 3 [7:0]

22.4 Functional Description

22.4.1 Modes of Operation

The FTMRZ192K2K module provides the modes of operation normal and special . The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and DFPROT registers (see Table 22-28.).

22.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x1F_C0B6. The contents of the word are defined in Table 22-27.

Table 22-27. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

22.4.3 Flash Block Read Access

If data read from the Flash block results in a double-bit fault ECC error (meaning that data is detected to be in error and cannot be corrected), the read data will be tagged as invalid during that access (please look into the Reference Manual for details). Forcing the DFDF status bit by setting FDFD (see <st-blue>Section

Table 22-69. Protection Override Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != (001, 010 or 011) at command launch.
		Set if command not available in current mode (see Table 22-28).
		Set if protection is supposed to be restored (if key does not match or is invalid) and Protection Override command was not run previously (bit FPSTAT FPOVRD is 0), so there are no previous valid values of FPROT and DFPROT to be re-loaded.
		Set if Protection Update Selection[1:0] = 00 (in case of CCOBIX[2:0] = 010 or 011)
		Set if Protection Update Selection[1:0] = 00, CCOBIX[2:0] = 001 and a valid comparison key is loaded as a command parameter.
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

22.4.8 Interrupts

The Flash module can generate an interrupt when a Flash command operation has completed or when a Flash command operation has detected an ECC fault.

Table 22-70. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Command Complete	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit
ECC Single Bit Fault on Flash Read	SFDIF (FERSTAT register)	SFDIE (FERCNFG register)	I Bit

NOTE

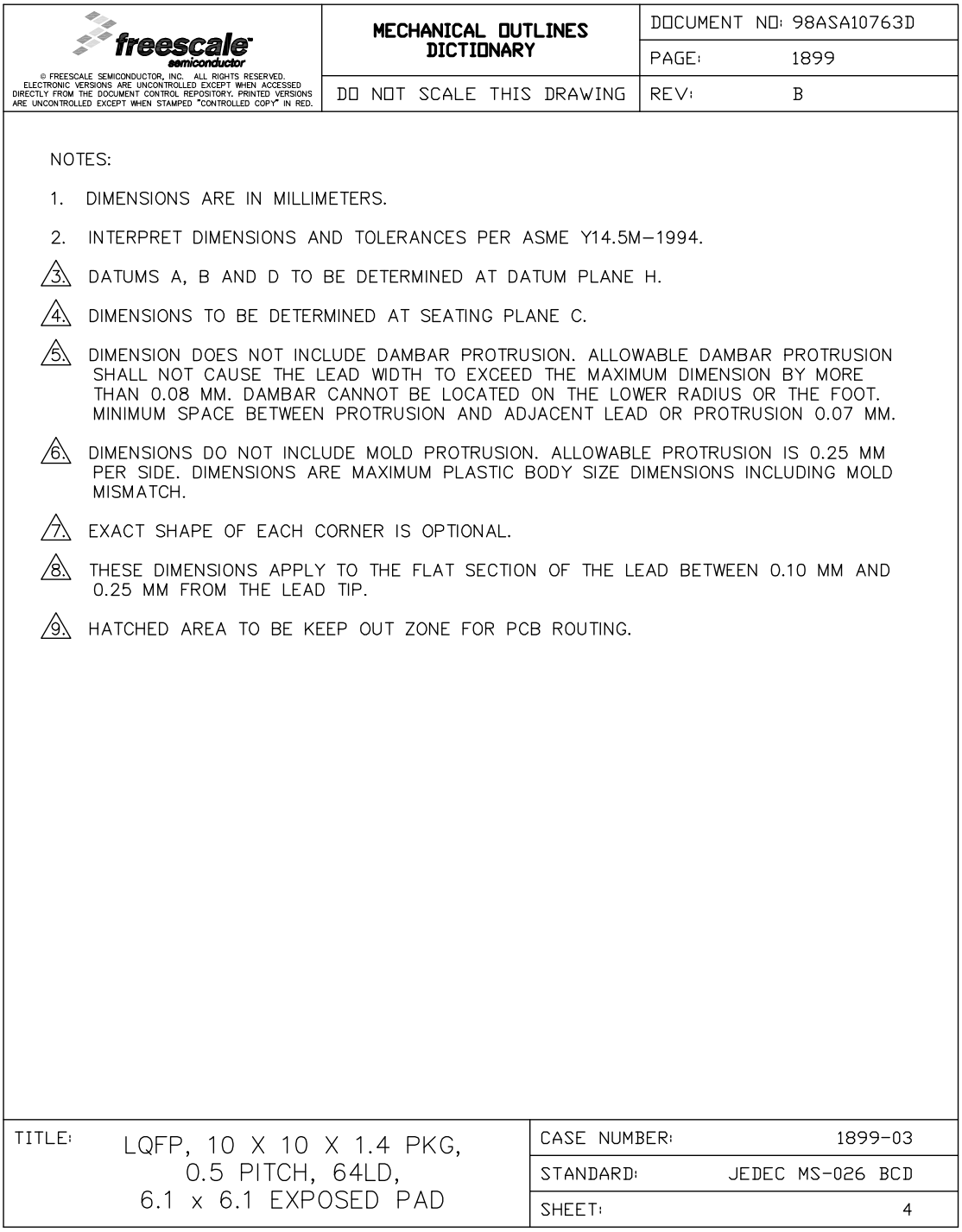
Vector addresses and their relative interrupt priority are determined at the MCU level.

22.4.8.1 Description of Flash Interrupt Operation

The Flash module uses the CCIF flag in combination with the CCIE interrupt enable bit to generate the Flash command interrupt request. The Flash module uses the SFDIF flag in combination with the SFDIE interrupt enable bits to generate the Flash error interrupt request. For a detailed description of the register bits involved, refer to Section 22.3.2.5, “Flash Configuration Register (FCNFG)”, Section 22.3.2.6, “Flash Error Configuration Register (FERCNFG)”, Section 22.3.2.7, “Flash Status Register (FSTAT)”, and Section 22.3.2.8, “Flash Error Status Register (FERSTAT)”.

The logic used for generating the Flash module interrupts is shown in Figure 22-31.

Figure L-3. 64 LQFP Exposed Pad Package



N.16 0x06C0-0x06DF CPMU

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06C0	CPMU RESERVED00	R	0	0	0	0	0	0	0	0
		W								
0x06C1	CPMU RESERVED01	R	0	0	0	0	0	0	0	0
		W								
0x06C2	CPMU RESERVED02	R	0	0	0	0	0	0	0	0
		W								
0x06C3	CPMURFLG	R	0	PORF	LVRF	0	COPRF	0	OMRF	PMRF
		W								
0x06C4	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x06C5	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x06C6	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x06C7	CPMUIFLG	R	RTIF	0	0	LOCKIF	LOCK	0	OSCIF	UPOSC
		W								
0x06C8	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x06C9	CPMUCLKS	R	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x06CA	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x06CB	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x06CC	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x06CD	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x06CE	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x06CF	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06D0	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x06D1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x06D2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								