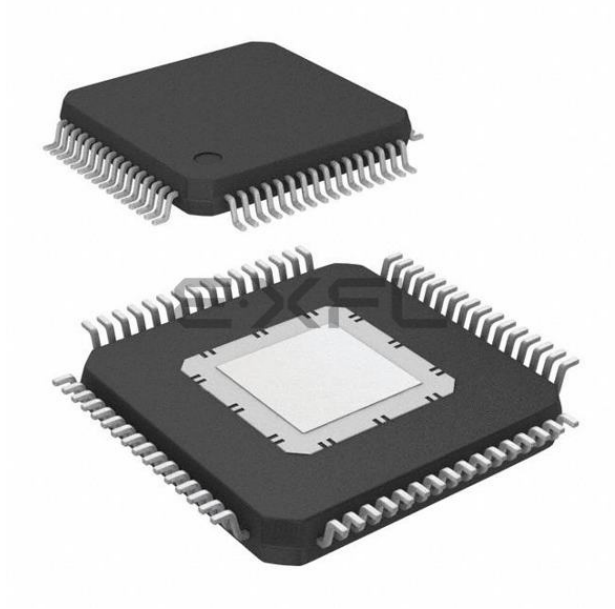

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 40V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	64-HLQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvca64f0wkh

Appendix A
MCU Electrical Specifications

Appendix B
ADC Electrical Specifications

- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIGState transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)

1.4.2 Embedded Memory

1.4.2.1 Memory Access Integrity

- Illegal address detection
- ECC support on embedded NVM and system RAM

1.4.2.2 Flash

On-chip flash memory on the MC9S12ZVC-Family on the features the following:

- Up to 192Kbytes of program flash memory
  - Automated program and erase algorithm
  - Protection scheme to prevent accidental program or erase

1.4.2.3 EEPROM

- 2 Kbytes EEPROM
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 4 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

1.4.2.4 SRAM

- 12 Kbytes of general-purpose RAM with ECC
  - Single bit error correction and double bit error detection code based on 16-bit data words

1.4.3 Clocks, Reset and Power Management Unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor, supervising the correct function of the oscillator (CM)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory

drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

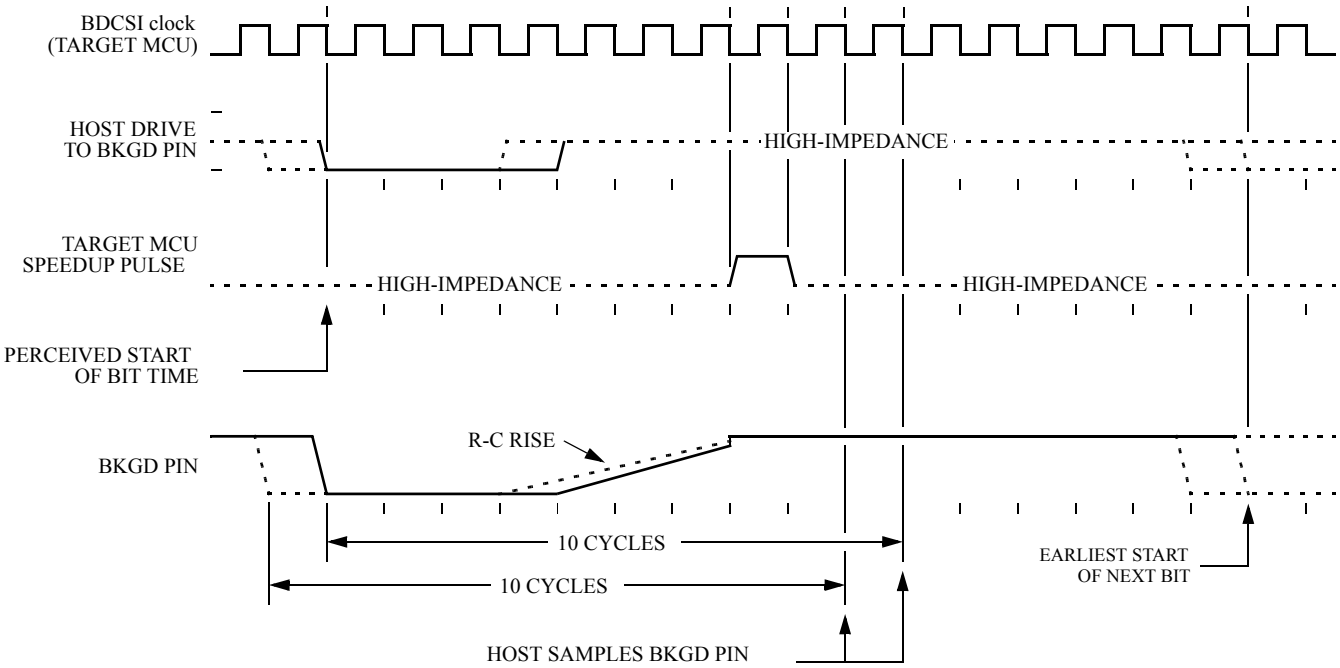


Figure 3-7. BDC Target-to-Host Serial Bit Timing (Logic 1)

Figure 3-8 shows the host receiving a logic 0 from the target. The host initiates the bit time but the target finishes it. Since the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

Field	Description
7-4 (MMCECL) ACC[3:0]	**Access Type Field** — The ACC[3:0] bits capture the type of memory access, which caused the access violation. The access type is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: opcode fetch 2: vector fetch 3: data load 4: data store 5-15: reserved
3-0 (MMCECL) ERR[3:0]	**Error Type Field** — The EC[3:0] bits capture the type of the access violation. The type is captured in form of a 4 bit value which is assigned as follows: 0: none (no error condition detected) 1: access to an illegal address 2: uncorrectable ECC error 3-15: reserved

The MMCEC register captures debug information about access violations. It is set to a non-zero value if a S12ZCPU access violation or an uncorrectable ECC error has occurred. At the same time this register is set to a non-zero value, access information is captured in the MMCPCn and MMCCCRn registers. The MMCECn, the MMCPCn and the MMCCCRn registers are not updated if the MMCECn registers contain a non-zero value. The MMCECn registers are cleared by writing the value 0xFFFF.

4.3.2.3 Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Address: 0x0082 (MMCCCRH)

	7	6	5	4	3	2	1	0
R	CPUU	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Address: 0x0083 (MMCCCRL)

	7	6	5	4	3	2	1	0
R	0	CPUX	0	CPUI	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-6. Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Read: Anytime

Write: Never

Please refer to Section 9.4.2.1, “ADC Control Register 0 (ADCCTL_0) and Section 9.5.3.2.4, “The two conversion flow control Mode Configurations for more information regarding conversion flow control.

Because internal components of the ADC are turned on/off with bit ADC_EN, the ADC requires a recovery time period (t_{REC}) after ADC is enabled until the first conversion can be launched via a trigger.

When bit ADC_EN gets cleared (transition from 1’b1 to 1’b0) any ongoing conversion sequence will be aborted and pending results, or the result of current conversion, gets discarded (not stored). The ADC cannot be re-enabled before any pending action or action in process is finished respectively aborted, which could take up to a maximum latency time of $t_{DISABLE}$ (see device level specification for more details).

Table 9-13. ADCEIF Field Descriptions (continued)

Field	Description
3 TRIG_EIF	**Trigger Error Interrupt Flag** — This flag indicates that a trigger error occurred. This flag is set in “Restart” Mode when a conversion sequence got aborted and no Restart Event occurred before the Trigger Event or if the Trigger Event occurred before the Restart Event was finished (conversion command has been loaded). This flag is set in “Trigger” Mode when a Trigger Event occurs before the Restart Event is issued to start conversion of the initial Command Sequence List. In “Trigger” Mode only a Restart Event is required to start conversion of the initial Command Sequence List. This flag is set when a Trigger Event occurs before a conversion sequence got finished. This flag is also set if a Trigger occurs while a Trigger Event is just processed - first conversion command of a sequence is beginning to sample (see also Section 9.5.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios). This flag is also set if the Trigger Event occurs automatically generated by hardware in “Trigger Mode” due to a Restart Event and simultaneously a Trigger Event is generated via data bus or internal interface. The ADC ceases operation if this error flag is set (issue of type severe). 0 No trigger error occurred. 1 A trigger error occurred.
2 RSTAR_EIF	**Restart Request Error Interrupt Flag** — This flag indicates a flow control issue. It is set when a Restart Request occurs after a Trigger Event and before one of the following conditions was reached: - The “End Of List” command type has been executed - Depending on bit STR_SEQA if the “End Of List” command type is about to be executed - The current CSL has been aborted or is about to be aborted due to a Sequence Abort Request. The ADC continues operation if this error flag is set. This flag is not set for Restart Request overrun scenarios (see also Section 9.5.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios). 0 No Restart request error situation occurred. 1 Restart request error situation occurred.
1 LDOK_EIF	**Load OK Error Interrupt Flag** — This flag can only be set in “Restart Mode”. It indicates that a Restart Request occurred without LDOK. This flag is not set if a Sequence Abort Event is already in process (bit SEQA set) when the Restart Request occurs or a Sequence Abort Request occurs simultaneously with the Restart Request. The LDOK_EIF error flag is also not set in “Restart Mode” if the first Restart Event occurs after: - ADC got enabled - Exit from Stop Mode - ADC Soft-Reset - ADC used in CSL single buffer mode The ADC continues operation if this error flag is set. 0 No Load OK error situation occurred. 1 Load OK error situation occurred.

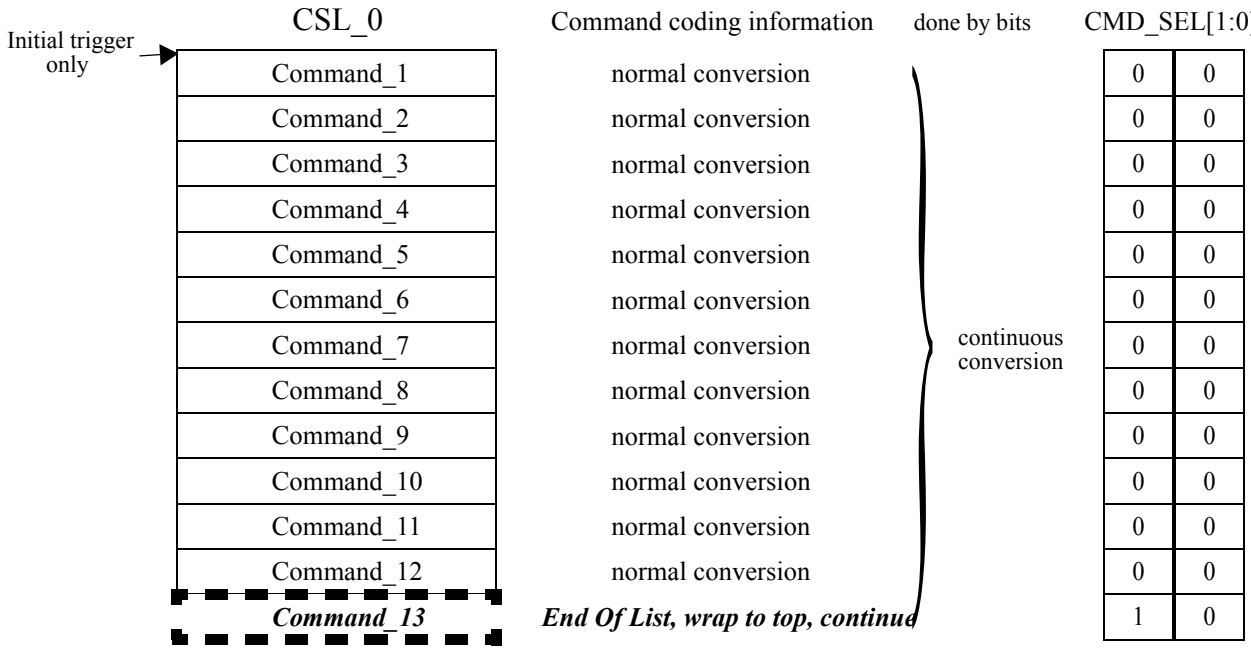


Figure 9-30. Example CSL for continues conversion

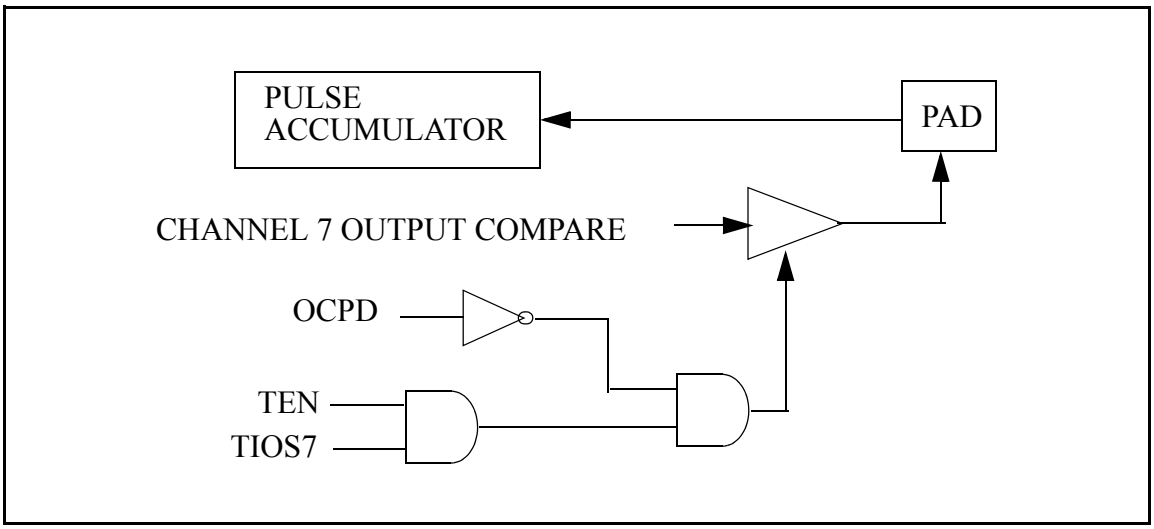


Figure 11-4. Channel 7 Output Compare/Pulse Accumulator Logic

11.2 External Signal Description

The TIM16B8CV3 module has a selected number of external pins. Refer to device specification for exact number.

11.2.1 IOC7 — Input Capture and Output Compare Channel 7

This pin serves as input capture or output compare for channel 7 . This can also be configured as pulse accumulator input.

11.2.2 IOC6 - IOC0 — Input Capture and Output Compare Channel 6-0

Those pins serve as input capture or output compare for TIM16B8CV3 channel .

NOTE

For the description of interrupts see Section 11.6, “Interrupts”.

11.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

11.3.1 Module Memory Map

The memory map for the TIM16B8CV3 module is given below in Figure 11-5. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B8CV3 module and the address offset for each register.

12.3.2.13 Output Compare Pin Disconnect Register(OCPD)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OCPD3	OCPD2	OCPD1	OCPD0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. Output Compare Pin Disconnect Register (OCPD)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-15. OCPD Field Description

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
3:0 OCPD[3:0]	**Output Compare Pin Disconnect Bits** 0 Enables the timer channel port. Output Compare action will occur on the channel pin. These bits do not affect the input capture . 1 Disables the timer channel port. Output Compare action will not occur on the channel pin, but the output compare flag still become set.

12.3.2.14 Precision Timer Prescaler Select Register (PTPSR)

Module Base + 0x002E

	7	6	5	4	3	2	1	0
R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
Reset	0	0	0	0	0	0	0	0

Figure 12-21. Precision Timer Prescaler Select Register (PTPSR)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 12-16. PTPSR Field Descriptions

Field	Description
7:0 PTPS[7:0]	**Precision Timer Prescaler Select Bits** — These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. Table 12-17 shows some selection examples in this case. The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

16.3.1.6 IIC Control Register 2(IBCR2)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
W								
Reset	0	0	0	0	0	0	0	0

Figure 16-9. IIC Bus Control Register 2(IBCR2)

This register contains the variables used in general call and in ten-bit address.

Read and write anytime

Table 16-10. IBCR2 Field Descriptions

Field	Description
7 GCEN	**General Call Enable**. 0 General call is disabled. The module dont receive any general call data and address. 1 enable general call. It indicates that the module can receive address and any data.
6 ADTYPE	**Address Type—** This bit selects the address length. The variable must be configured correctly before IIC enters slave mode. 0 7-bit address 1 10-bit address
5,4,3 RESERVED	**Reserved** — Bit 5,4 and 3 of the IBCR2 are reserved for future compatibility. These bits will always read 0.
2:0 ADR[10:8]	**Slave Address [10:8]** —These 3 bits represent the MSB of the 10-bit address when address type is asserted (ADTYPE = 1).

16.4 Functional Description

This section provides a complete functional description of the IICV3.

16.4.1 I-Bus Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts: START signal, slave address transmission, data transfer and STOP signal. They are described briefly in the following sections and illustrated in Figure 16-10.

17.1.2 Modes of Operation

There are five modes the CAN Physical Layer can take (refer to 17.5.2 for details):

1. Shutdown mode
   In shutdown mode the CAN Physical Layer is fully de-biased including the wake-up receiver.
2. Normal mode
   In normal mode the transceiver is fully biased and functional. The SPLIT pin drives 2.5 V if enabled.
3. Pseudo-normal mode
   Same as normal mode with CANL driver disabled.
4. Listen-only mode
   Same as normal mode with transmitter de-biased.
5. Standby mode with configurable wake-up feature
   In standby mode the transceiver is fully de-biased. The wake-up receiver is enabled out of reset.

- CPU Run Mode
  The CAN Physical Layer is able to operate normally in modes 1 to 4.
- CPU Wait Mode
  The CAN Physical Layer operation is the same as in CPU run mode.
- CPU Stop Mode
  The CAN Physical Layer enters standby mode when the device voltage regulator switches to reduced performance mode (“RPM”) after a CPU stop mode request.
  If enabled, the wake-up pulse filtering mechanism is activated immediately at CPU stop mode entry.

17.1.3 Block Diagram

Figure 17-1 shows a block diagram of the CAN Physical Layer. The module consists of a precision receiver, a low-power wake-up receiver, an output driver and diagnostics.

Table 17-6. CPSR Register Field Descriptions

Field	Description
4 CPCLVL	**CANL Voltage Failure Low Status Bit** This bit reflects the CANL voltage failure low monitor status. 0 Condition $V_{CANL} > V_{L0}$ 1 Condition $V_{CANL} \leq V_{L0}$
3 CPDT	**CPTXD-Dominant Timeout Status Bit** This bit is set to 1, if CPTXD is dominant for longer than $t_{CPTXDDT}$. It signals a timeout event and remains set until CPTXD returns to recessive level for longer than 1 µs. 0 No CPTXD-timeout occurred or CPTXD has ceased to be dominant after timeout 1 CPTXD-dominant timeout occurred and CPTXD is still dominant

17.5 Functional Description

17.5.1 General

The CAN Physical Layer provides an interface for the SoC-integrated MSCAN controller.

17.5.2 Modes

Figure 17-10 shows the possible mode transitions depending on control bit CPE, device reduced performance mode (“RPM”; refer to “Low Power Modes” section in device overview) and bus error conditions.

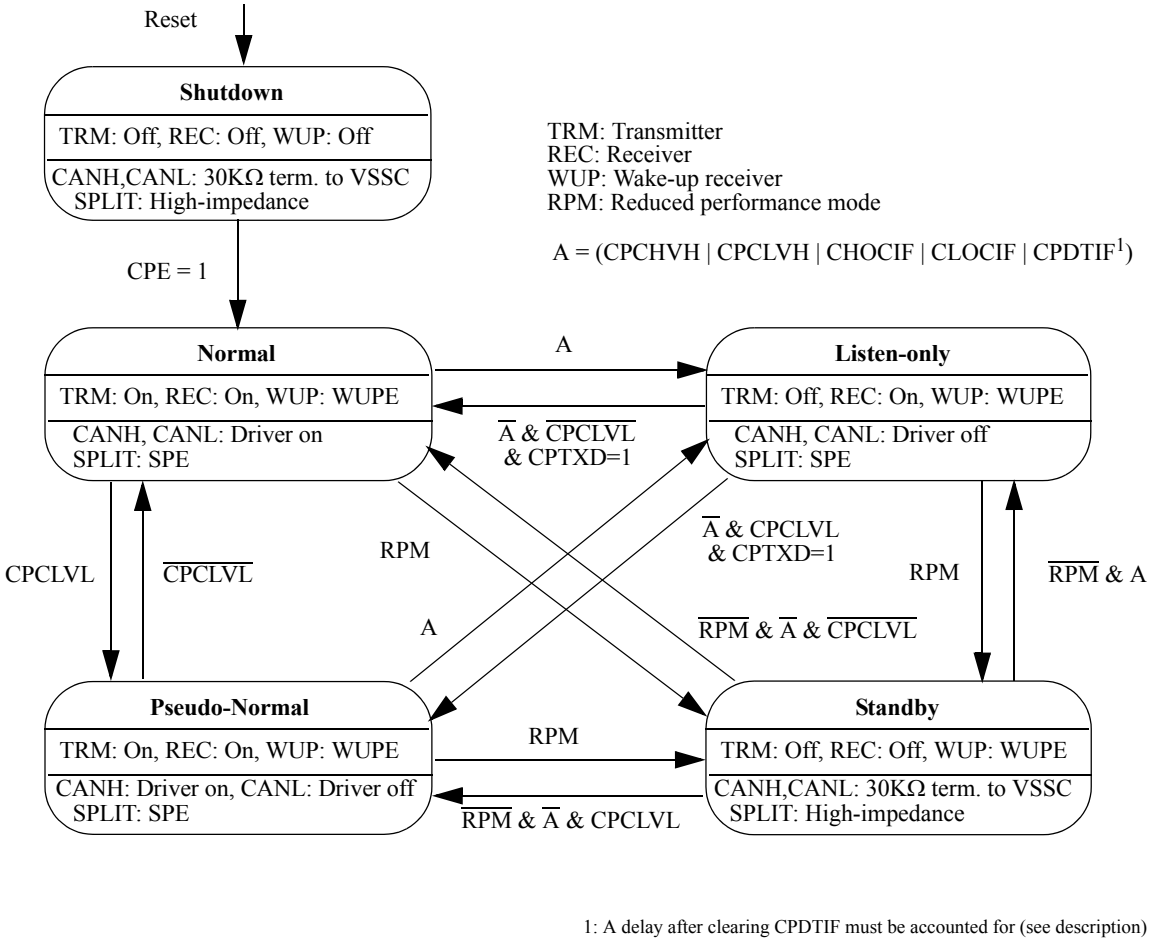


Figure 17-10. CAN Physical Layer Mode Transitions

17.5.2.1 Shutdown Mode

Shutdown mode is a low power mode and entered out of reset. The transceiver, wake-up, bus error diagnostic, dominant timeout and interrupt functionality are disabled. CANH and CANL lines are pulled

18.1.1 Glossary

Table 18-1. Terminology

ACK	Acknowledge of CAN message
CAN	Controller Area Network
CRC	Cyclic Redundancy Code
EOF	End of Frame
FIFO	First-In-First-Out Memory
IFS	Inter-Frame Sequence
SOF	Start of Frame
CPU bus	CPU related read/write data bus
CAN bus	CAN protocol related serial bus
oscillator clock	Direct clock from external oscillator
bus clock	CPU bus related clock
CAN clock	CAN protocol related clock

18.1.2 Block Diagram

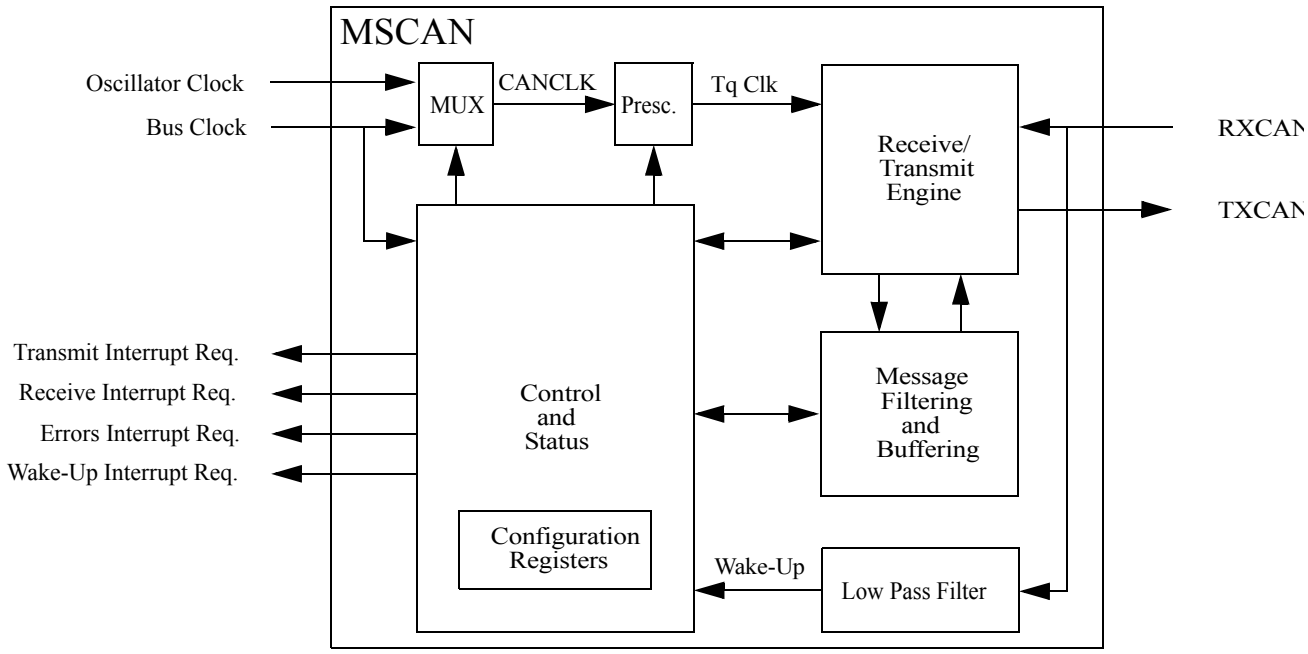


Figure 18-1. MSCAN Block Diagram

Figure 18-24. Receive/Transmit Message Buffer — Extended Identifier Mapping

Register Name		Bit 7	6	5	4	3	2	1	Bit0
0x00X0 IDR0	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	W								
0x00X1 IDR1	R	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
	W								
0x00X2 IDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	W								
0x00X3 IDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	W								
0x00X4 DSR0	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X5 DSR1	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X6 DSR2	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X7 DSR3	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X8 DSR4	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00X9 DSR5	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XA DSR6	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XB DSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	W								
0x00XC DLR	R					DLC3	DLC2	DLC1	DLC0
	W								

Table 22-45. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 22-28)
	FPVIOL	Set if any area of the P-Flash or EEPROM memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

22.4.7.7.1 Erase All Pin

The functionality of the Erase All Blocks command is also available in an uncommanded fashion from the *soc_erase_all_req* input pin on the Flash module. Refer to the Reference Manual for information on control of *soc_erase_all_req*.

The erase-all function requires the clock divider register FCLKDIV (see <st-blue>Section 22.3.2.1 Flash Clock Divider Register (FCLKDIV)) to be loaded before invoking this function using *soc_erase_all_req* input pin. Please refer to the Reference Manual for information about the default value of FCLKDIV in case direct writes to register FCLKDIV are not allowed by the time this feature is invoked. If FCLKDIV is not properly set the erase-all operation will not execute and the ACCERR flag in FSTAT register will set. After the execution of the erase-all function the FCLKDIV register will be reset and the value of register FCLKDIV must be loaded before launching any other command afterwards.

Before invoking the erase-all function using the *soc_erase_all_req* pin, the ACCERR and FPVIOL flags in the FSTAT register must be clear. When invoked from *soc_erase_all_req* the erase-all function will erase all P-Flash memory and EEPROM memory space regardless of the protection settings. If the post-erase verify passes, the routine will then release security by setting the SEC field of the FSEC register to the unsecure state (see <st-blue>Section 22.3.2.2 Flash Security Register (FSEC)). The security byte in the Flash Configuration Field will be programmed to the unsecure state (see Table 22-8.). The status of the erase-all request is reflected in the ERSAREQ bit in the FCNFG register (see <st-blue>Section 22.3.2.5 Flash Configuration Register (FCNFG)). The ERSAREQ bit in FCNFG will be cleared once the operation has completed and the normal FSTAT error reporting will be available as described inTable 22-46..

At the end of the erase-all sequence Protection will remain configured as it was before executing the erase-all function. If the application requires programming P-Flash and/or EEPROM after the erase-all function completes, the existing protection limits must be taken into account. If protection needs to be disabled the user may need to reset the system right after completing the erase-all function.

Table 22-46. Erase All Pin Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if command not available in current mode (see Table 22-28)
	MGSTAT1	Set if any errors have been encountered during the erase verify operation, or during the program verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the erase verify operation, or during the program verify operation

Table K-3. NVM Reliability Characteristics (Junction Temperature From –40°C To +175°C)

NUM	C	Rating	Symbol	Min	Typ	Max	Unit
		Program Flash Arrays					
1	C	Data retention at an average junction temperature of T_{Javg} = 85°C[1] after up to 10,000 program/erase cycles	t_{NVMRET}	20	100[2]	—	Years
2	C	Program Flash number of program/erase cycles (-40°C ≤ Tj ≤ 150°C)	n_{FLPE}	10K	100K[3]	—	Cycles
		EEPROM Array					
3	C	Data retention at an average junction temperature of T_{Javg} = 85°C[1] after up to 100,000 program/erase cycles	t_{NVMRET}	5	100[2]	—	Years
4	C	Data retention at an average junction temperature of T_{Javg} = 85°C[1] after up to 10,000 program/erase cycles	t_{NVMRET}	10	100[2]	—	Years
5	C	Data retention at an average junction temperature of T_{Javg} = 85°C[1] after less than 100 program/erase cycles	t_{NVMRET}	20	100[2]	—	Years
6	C	EEPROM number of program/erase cycles (-40°C ≤ Tj ≤ 150°C)	n_{FLPE}	100K	500K[3]	—	Cycles

1 T_{Javg} does not exceed 85°C in a typical temperature profile over the lifetime of a consumer, industrial or automotive application.

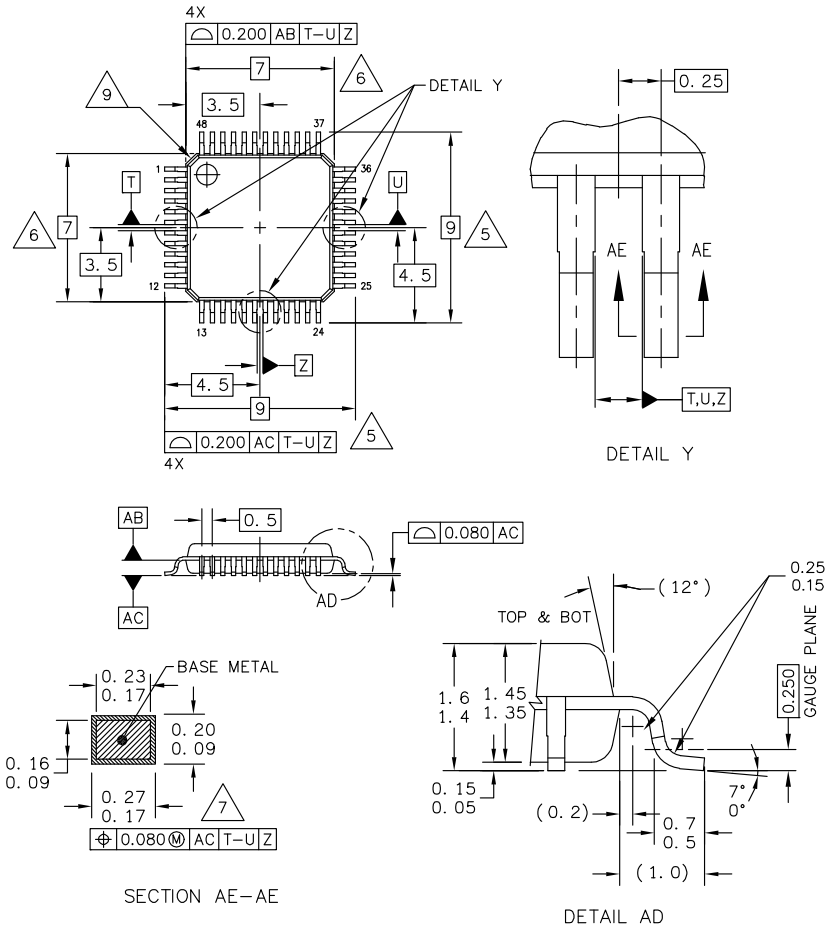
2 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how NXP defines Typical Data Retention, please refer to Engineering Bulletin EB618

3 Spec table quotes typical endurance evaluated at 25°C for this product family. For additional information on how NXP defines Typical Endurance, please refer to Engineering Bulletin EB619.

K.3 NVM Factory Shipping Condition

Devices are shipped from the factory with flash and EEPROM in the erased state. Data retention specifications begin at time of this erase operation. For additional information on how NXP defines Typical Data Retention, please refer to Engineering Bulletin EB618.

Figure L-4. 48 LQFP Package



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x028A–0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	PIEADH	R	PIEADH7	PIEADH6	PIEADH5	PIEADH4	PIEADH3	PIEADH2	PIEADH1	PIEADH0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								
0x028E	PIFADH	R	PIFADH7	PIFADH6	PIFADH5	PIFADH4	PIFADH3	PIFADH2	PIFADH1	PIFADH0
		W								
0x028F	PIFADL	R	PIFADL7	PIFADL6	PIFADL5	PIFADL4	PIFADL3	PIFADL2	PIFADL1	PIFADL0
		W								
0x0290–0x0297	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0298	DIENADH	R	DIENADH7	DIENADH6	DIENADH5	DIENADH4	DIENADH3	DIENADH2	DIENADH1	DIENADH0
		W								
0x0299	DIENADL	R	DIENADL7	DIENADL6	DIENADL5	DIENADL4	DIENADL3	DIENADL2	DIENADL1	DIENADL0
		W								
0x029A–0x02BF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02C0	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x02C1	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x02C2	DDRT	R	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x02C3	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x02C4	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x02C5–0x02CE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x02CF	Reserved	R	0	0	0	0	0	0	0	0
		W								

N.10 0x0500-0x052F PWM1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x051D	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x051E	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x051F	PWMDTY32	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0520	PWMDTY42	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0521	PWMDTY52	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0522	PWMDTY62	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0523	PWMDTY72	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0524 - 0x052F	RESERVED	R W	0	0	0	0	0	0	0	0

N.11 0x05C0-0x05EF TIM0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05C0	TIM0TIOS	R W	0	0	0	0	IOS3	IOS2	IOS1	IOS0
0x05C1	TIM0CFORC	R W	0	0	0	0	0 FOC3	0 FOC2	0 FOC1	0 FOC0
0x05C2	Reserved	R W								
0x05C3	Reserved	R W								
0x05C4	TIM0TCNTH	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x05C5	TIM0TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x05C6	TIM0TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0