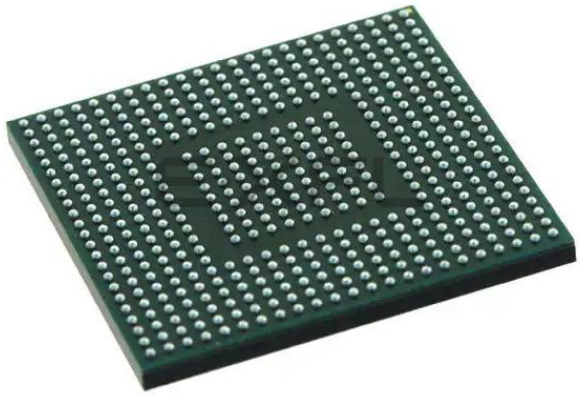

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309cvmaddca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

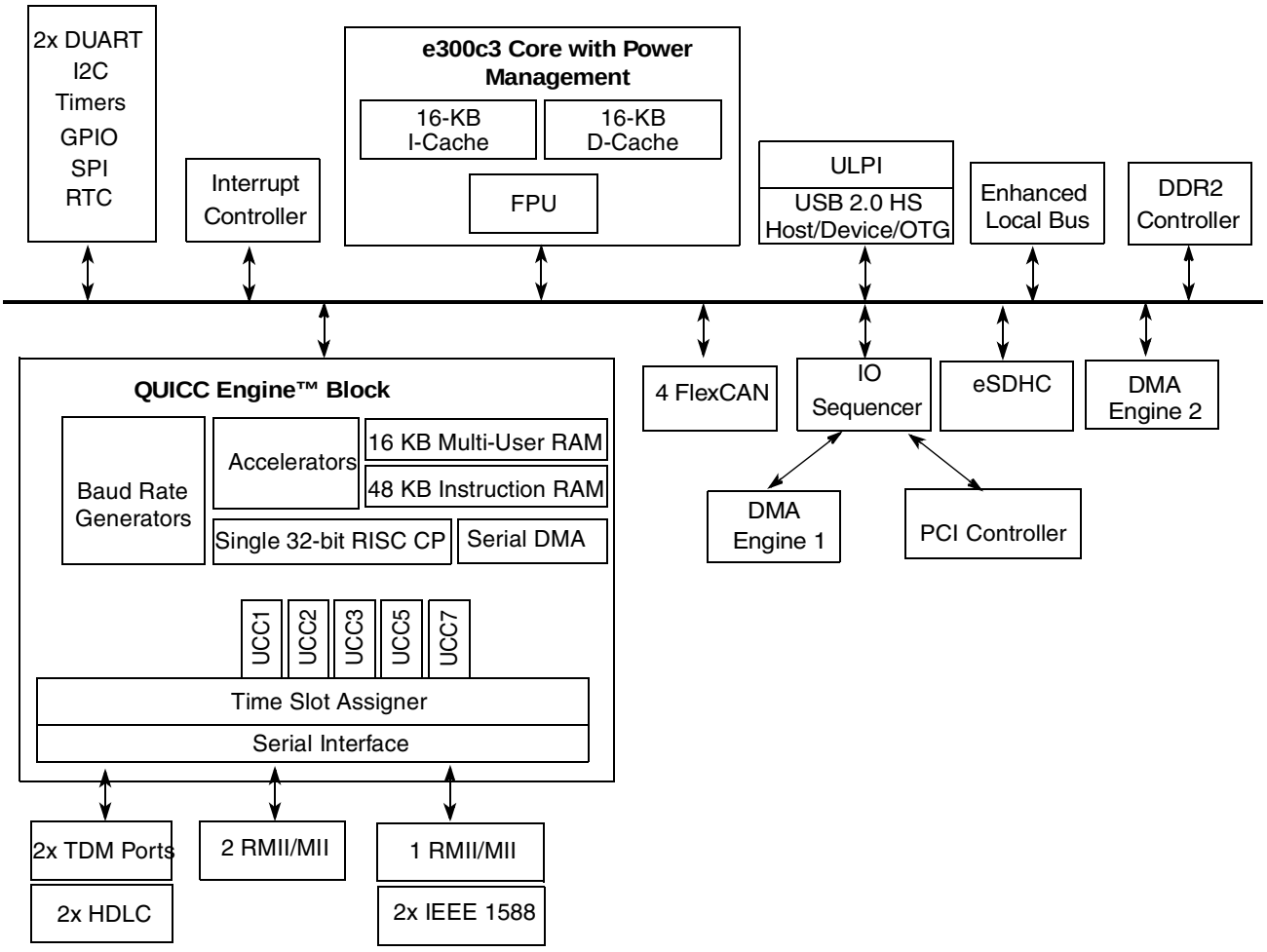

Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking.*

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - Supports 8-bit ECC
  - 16/32-bit data interface, up to 333-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 512-MB addressable space for 32 bit data interface
    - 64-Mbit to 2-Gbit devices with x8/x16/x32 data ports (no direct x4 support)
  - One 16-bit device or two 8-bit devices on a 16-bit bus, or two 16-bit devices or four 8-bit devices on a 32-bit bus Support for up to 16 simultaneous open pages for DDR2
  - Two clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources
  - Programmable highest priority request
  - Six groups of interrupts with programmable priority

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O power dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.149	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.415	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, PCI, SPI, Timer output, FlexCAN, eSDHC				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock input timing

This section provides the clock input DC and AC electrical characteristics for the MPC8309.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC electrical characteristics

The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC electrical characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

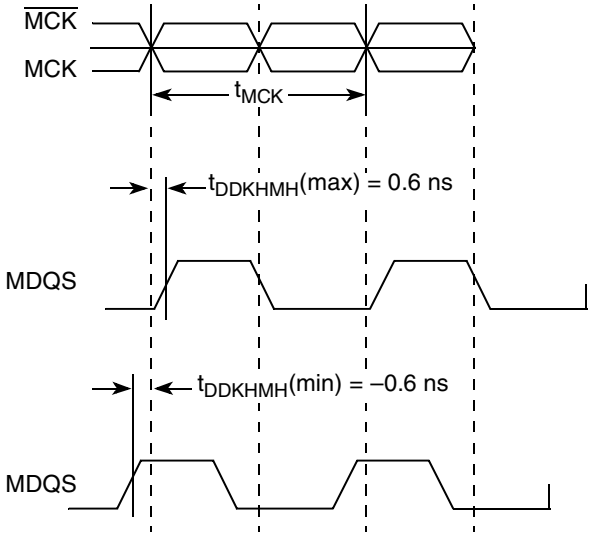

Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

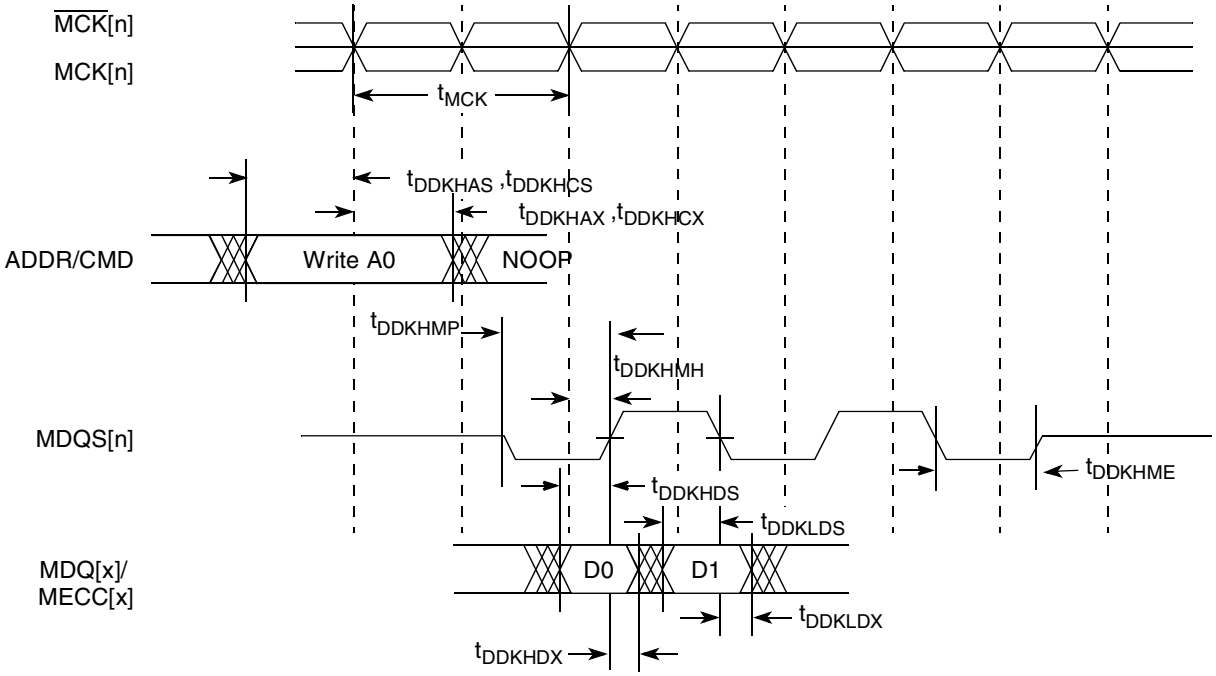

Figure 6. DDR2 SDRAM output timing diagram

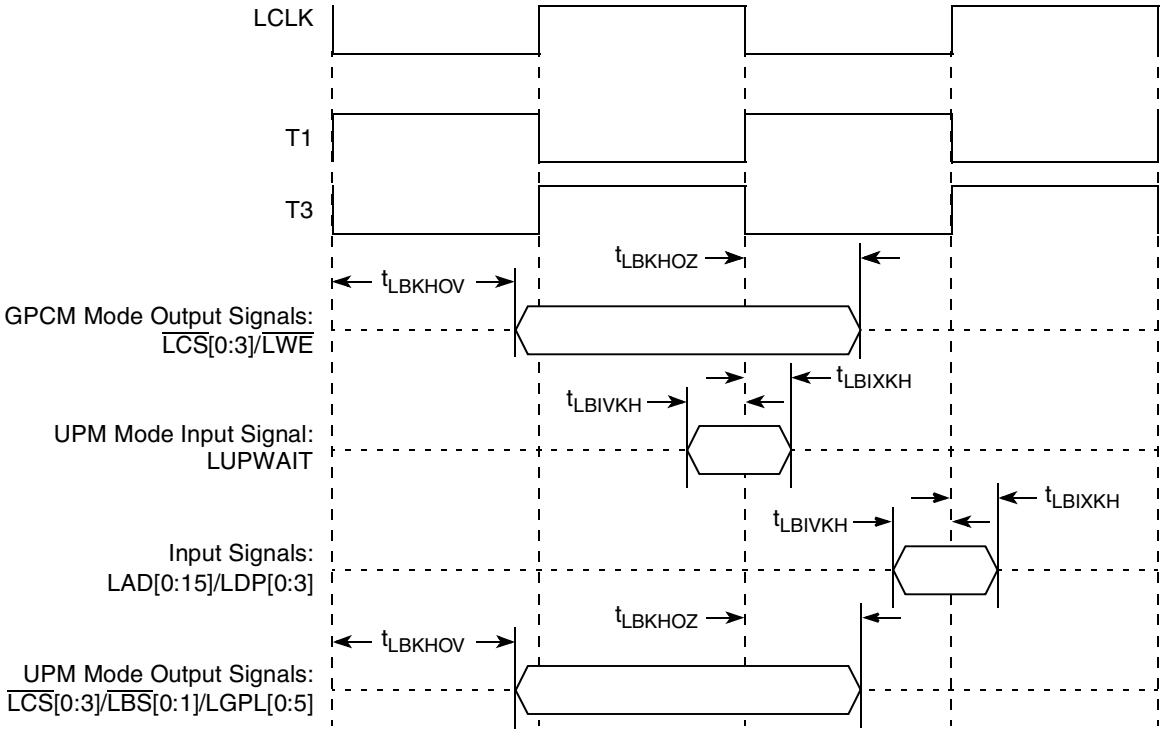

Figure 9. Enhanced local bus signals, GPCM/UPM signals for LCRR[CLKDIV] = 2

The following figure shows the RMII transmit AC timing diagram.

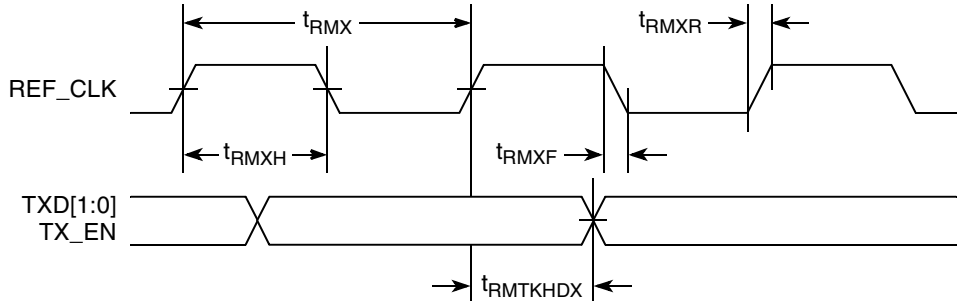

Figure 15. RMII transmit AC timing diagram

8.2.2.2 RMII receive AC timing specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 34. USB general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

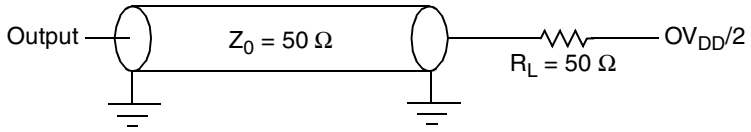

Figure 26. USB AC test load

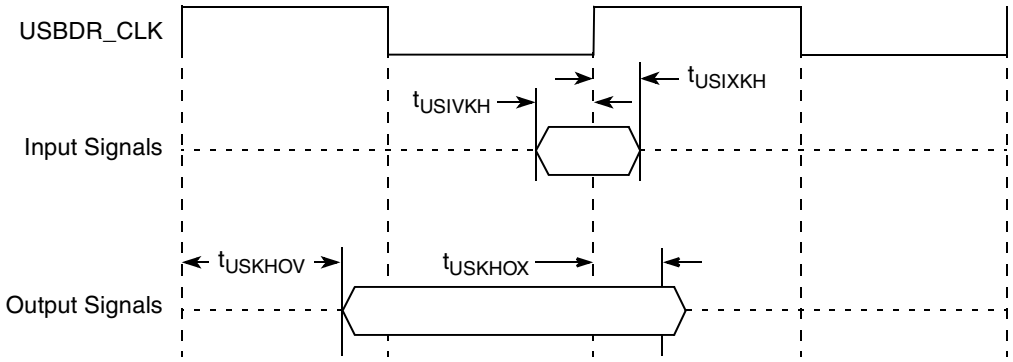

Figure 27. USB signals

Table 38. eSDHC AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–33.25 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

The following figure provides the eSDHC clock input timing diagram.

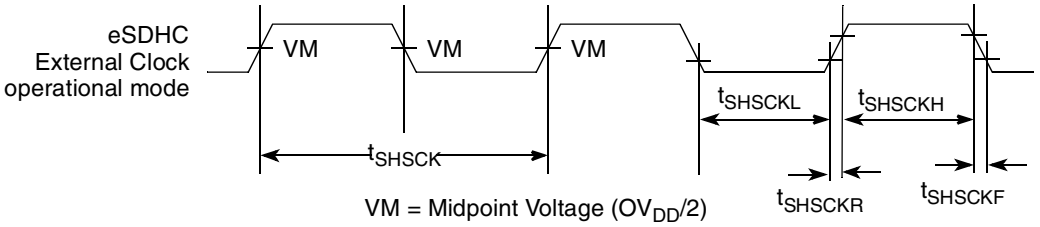

Figure 28. eSDHC clock input timing diagram

The following figure provides the data and command input/output timing diagram.

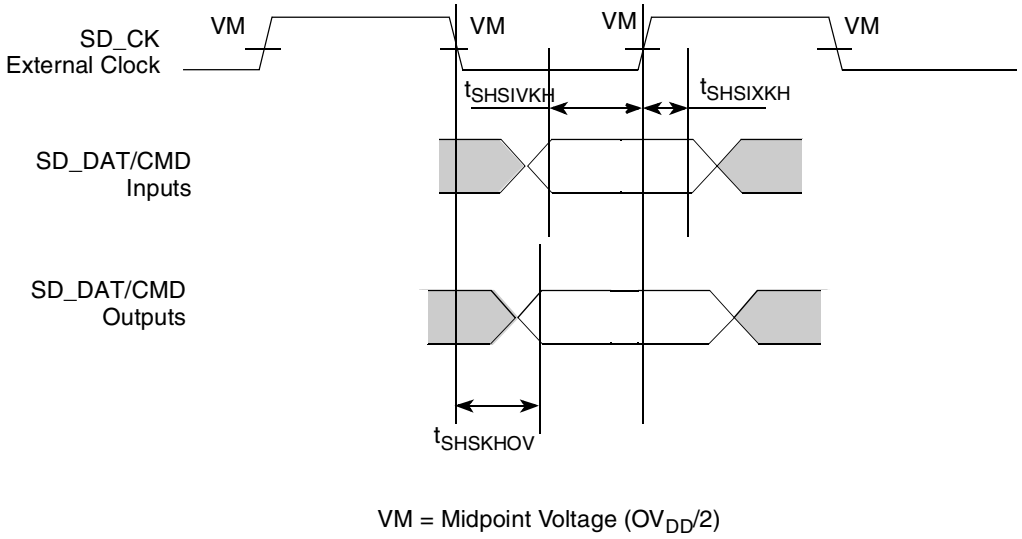

Figure 29. eSDHC data and command input/output timing diagram referenced to clock

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8309.

17.1 Timer DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 43. Timer DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

17.2 Timer AC timing specifications

The following table provides the timer input and output AC timing specifications.

Table 44. Timer input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

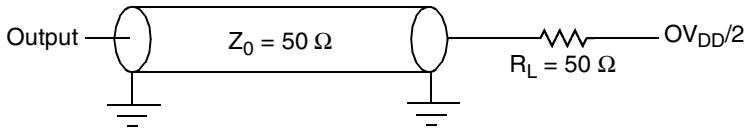

Figure 32. Timers AC test load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8309.

18.1 GPIO DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 GPIO.

Table 45. GPIO DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

18.2 GPIO AC timing specifications

The following table provides the GPIO input and output AC timing specifications.

Table 46. GPIO input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

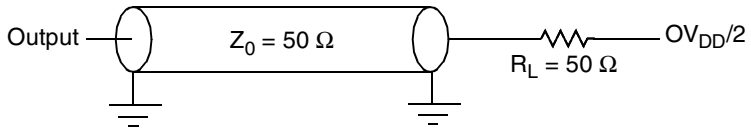

Figure 33. GPIO AC test load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8309.

19.1 IPIC DC electrical characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8309.

Table 47. IPIC DC electrical characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC timing specifications

The following table provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8309.

20.1 SPI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 SPI.

Table 49. SPI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

20.2 SPI AC timing specifications

The following table and provide the SPI input and output AC timing specifications.

Table 50. SPI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8309_output_port spimosi_lpgl0(SPI Master mode)
4. Delay units must not be enabled for Slave mode.

The following figure provides the AC test load for the SPI.

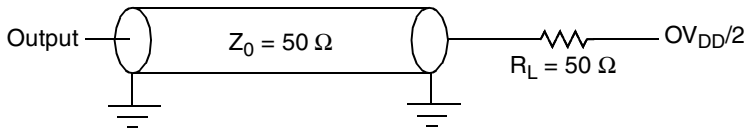

Figure 34. SPI AC test load

Figure 35 and Figure 36 represent the AC timing from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 51. JTAG interface DC electrical characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

21.2 JTAG AC electrical characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309. The following table provides the JTAG AC timing specifications as defined in Figure 38 through Figure 41.

Table 52. JTAG AC timing specifications (independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5

The following figure provides the boundary-scan timing diagram.

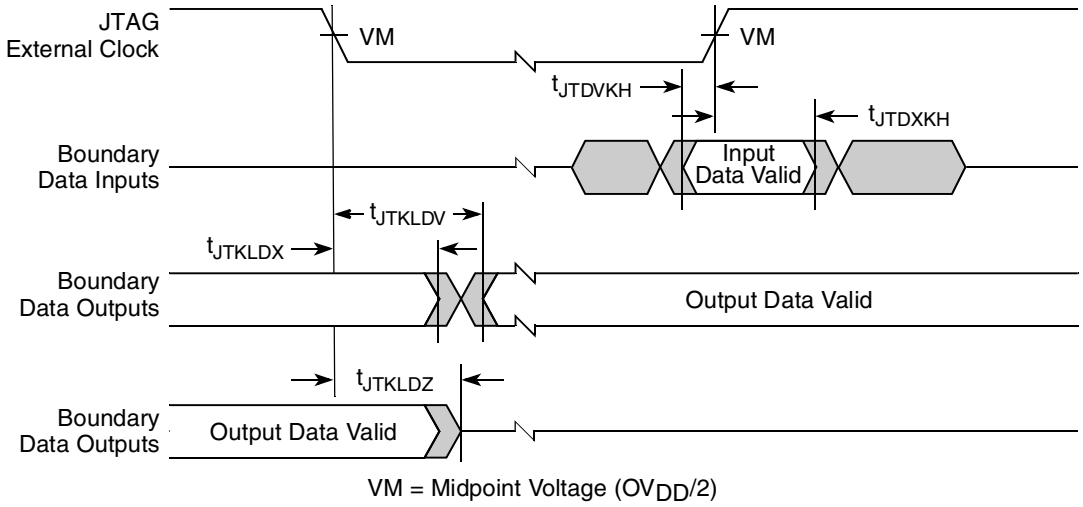

Figure 40. Boundary-Scan timing diagram

The following figure provides the test access port timing diagram.

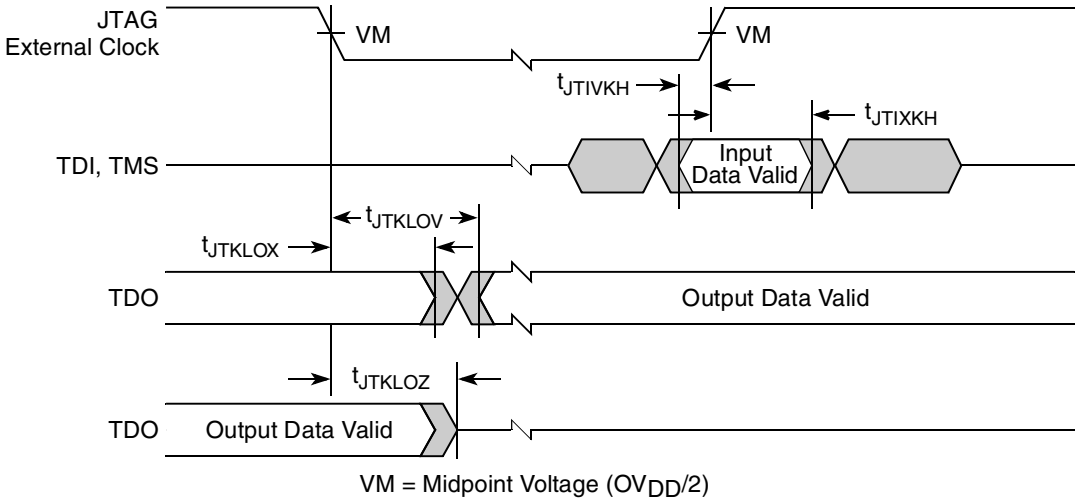

Figure 41. Test access port timing diagram

MEMC_MDQ29	D2	IO	GV_{DD}	—
MEMC_MDQ30	C2	IO	GV_{DD}	—
MEMC_MDQ31	C1	IO	GV_{DD}	—
MEMC_MECC0	Y5	IO	GV_{DD}	—
MEMC_MECC1	AA4	IO	GV_{DD}	—
MEMC_MECC2	Y4	IO	GV_{DD}	—
MEMC_MECC3	AA3	IO	GV_{DD}	—
MEMC_MECC4	AC2	IO	GV_{DD}	—
MEMC_MECC5	AB2	IO	GV_{DD}	—
MEMC_MECC6	Y3	IO	GV_{DD}	—
MEMC_MECC7	AB1	IO	GV_{DD}	—
MEMC_MDM0	W1	O	GV_{DD}	—
MEMC_MDM1	E1	O	GV_{DD}	—
MEMC_MDM2	V3	O	GV_{DD}	—
MEMC_MDM3	D1	O	GV_{DD}	—
MEMC_MDM8	W5	O	GV_{DD}	—
MEMC_MDQS0	T5	IO	GV_{DD}	—
MEMC_MDQS1	H5	IO	GV_{DD}	—
MEMC_MDQS2	P5	IO	GV_{DD}	—
MEMC_MDQS3	E5	IO	GV_{DD}	-
MEMC_MDQS8	V5	IO	GV_{DD}	-
MEMC_MBA0	K2	O	GV_{DD}	-
MEMC_MBA1	K3	O	GV_{DD}	-
MEMC_MBA2	N5	O	GV_{DD}	-
MEMC_MA0	L3	O	GV_{DD}	-
MEMC_MA1	L5	O	GV_{DD}	-
MEMC_MA2	L2	O	GV_{DD}	-
MEMC_MA3	L1	O	GV_{DD}	-
MEMC_MA4	M3	O	GV_{DD}	-
MEMC_MA5	M4	O	GV_{DD}	-
MEMC_MA6	M1	O	GV_{DD}	-
MEMC_MA7	N1	O	GV_{DD}	-
MEMC_MA8	N2	O	GV_{DD}	-
MEMC_MA9	N3	O	GV_{DD}	-
MEMC_MA10	L4	O	GV_{DD}	-
MEMC_MA11	P2	O	GV_{DD}	-
MEMC_MA12	N4	O	GV_{DD}	-

HDLC/TDM/GPIO				
HDLC1_TXCLK[CLK16]/GPIO_0/QE_BRG_5/TDM1_TCK[CLK4]	AA20	IO	OV_{DD}	-
HDLC1_RXCLK[CLK15]/GPIO_1/TDM1_RCK[CLK3]	AA21	IO	OV_{DD}	-
HDLC1_TXD/GPIO_2/TDM1_TD/CFG_RESET_SOURCE[0]	AB22	IO	OV_{DD}	1
HDLC1_RXD/GPIO_3/TDM1_RD	AB23	IO	OV_{DD}	-
HDLC1_CD_B/GPIO_4/TDM1_TFS	W19	IO	OV_{DD}	-
HDLC1_CTS_B/GPIO_5/TDM1_RFS	V19	IO	OV_{DD}	-
HDLC1_RTS_B/GPIO_6/TDM1_STROBE_B/CFG_RESET_SOURCE[1]	AA23	IO	OV_{DD}	-
HDLC2_TXCLK[CLK14]/GPIO_16/QE_BRG_7/TDM2_TCK[CLK6]	Y20	IO	OV_{DD}	-
HDLC2_RXCLK[CLK13]/GPIO_17/TDM2_RCK[CLK5]/QE_BRG_8	Y22	IO	OV_{DD}	-
HDLC2_TXD/GPIO_18/TDM2_TD/CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	1
HDLC2_RXD/GPIO_19/TDM2_RD	W21	IO	OV_{DD}	-
HDLC2_CD_B/GPIO_20/TDM2_TFS	V20	IO	OV_{DD}	-
HDLC2_CTS_B/GPIO_21/TDM2_RFS	Y23	IO	OV_{DD}	-
HDLC2_RTS_B/GPIO_22/TDM2_STROBE_B/CFG_RESET_SOURCE[3]	U20	IO	OV_{DD}	-
Power				
AVDD1	L16	-	-	-
AVDD2	M16	-	-	-
AVDD3	N8	-	-	-
GVDD	F6, G6, H6, J6, K6, L6, N6, P6, R6, T6, U6, V6, V7	-	-	-
NVDD	F7, F8, F9, F10, F11, F12, F13,F14, F15, F16, F17, F18, G18,H18, J18, L18, M18, N18, P18,R18, T18, U18, V8, V9, V10, V11, V12, V13,V14, V15, V16, V17, V18	-	-	-

Table 58. e300 Core PLL configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

23.6 QUICC Engine PLL configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 59. QUICC Engine PLL multiplication factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 60. QUICC Engine PLL VCO divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

qe_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QUICC Engine VCO Frequency = *qe_clk* × VCO divider × (1 + CEPDF)

23.7 Suggested PLL configurations

To simplify the PLL configurations, the MPC8309 might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs is configured separately.

The following table shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 61. Suggested PLL configurations

Conf No.	SPMF	Core PLL	CEPMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0111	0	33.33	133.33	266.66	233
2	0010	0000100	0111	1	66.67	133.33	266.66	233
3	0100	0000101	0111	0	33.33	133.33	333.33	233
4	0101	0000101	1001	0	25	125	312.5	225
5	0010	0000101	0111	1	66.67	133.33	333.33	233
6	0100	0000110	0111	0	33.33	133.33	399.96	233
7	0101	0000110	1000	0	25	125	375	225
8	0010	0000110	0011	0	66.67	133.33	399.96	233
9	0101	0000101	0111	0	33.33	166.67	416.67	233

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 63. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	?
R_P	42 Target	20 Target	Z_0	?
Differential	NA	NA	Z_{DIFF}	?

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

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