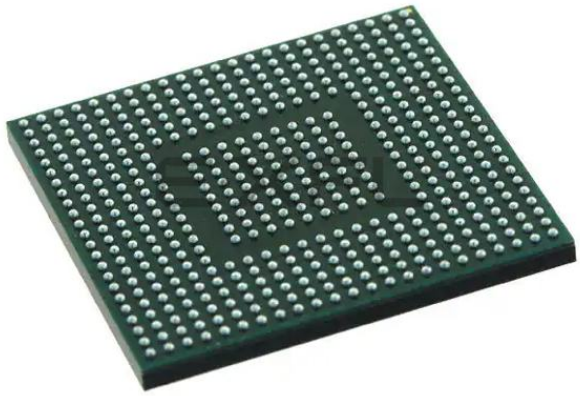

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Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309cvmafdca

Table 12. DDR2 SDRAM DC electrical characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 13. DDR2 SDRAM capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC electrical characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM input AC timing specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM input AC timing specifications for 1.8-V interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM input AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the input timing diagram for the DDR controller.

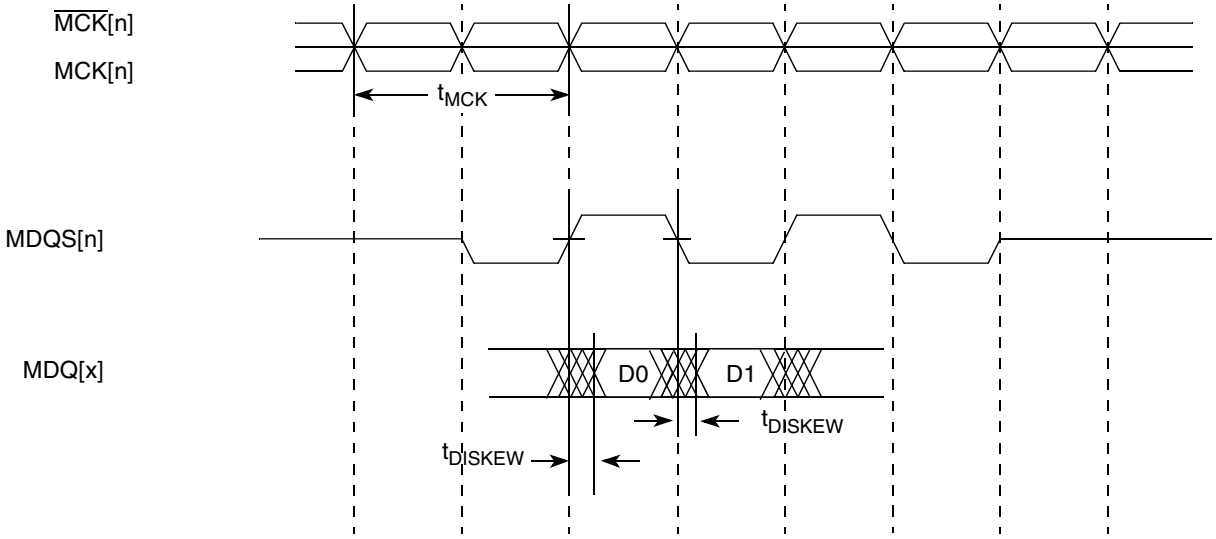


Figure 4. DDR input timing diagram

6.2.2 DDR2 SDRAM output AC timing specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM output AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK cycle time, (MCK/$\overline{MCK}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

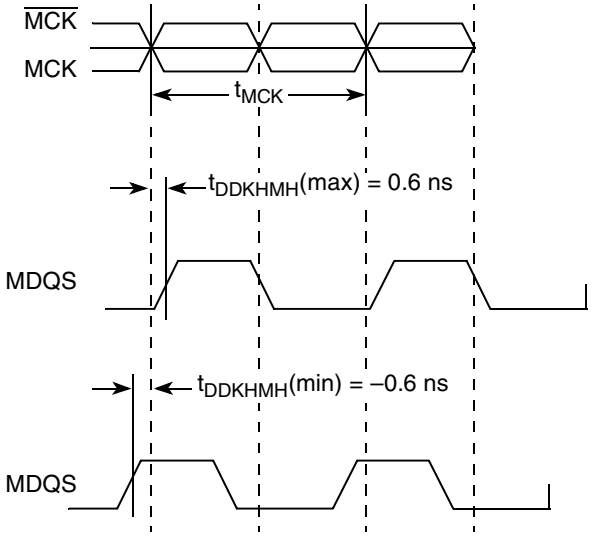


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

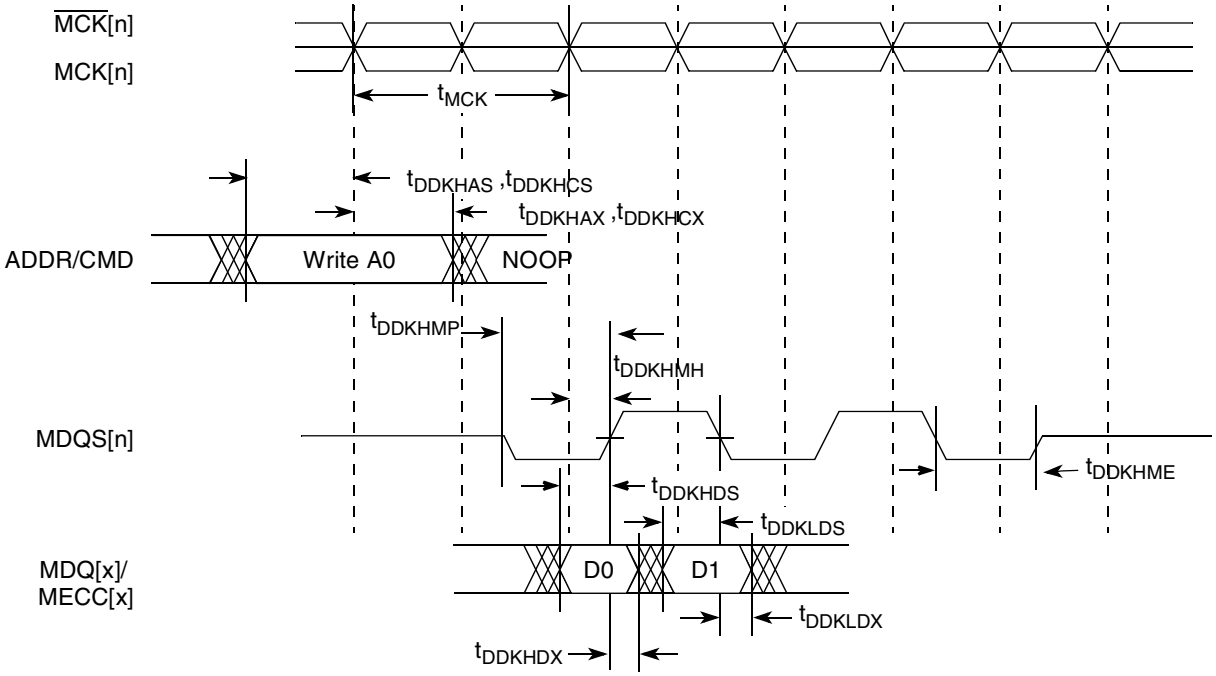


Figure 6. DDR2 SDRAM output timing diagram

The following figure shows the RMII transmit AC timing diagram.

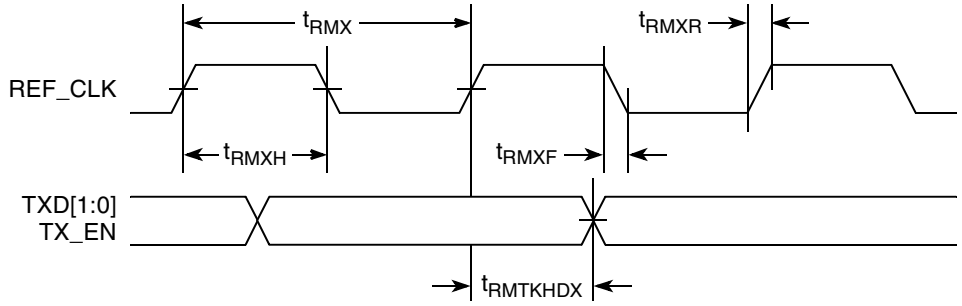


Figure 15. RMII transmit AC timing diagram

8.2.2.2 RMII receive AC timing specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 25. MII management AC timing specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

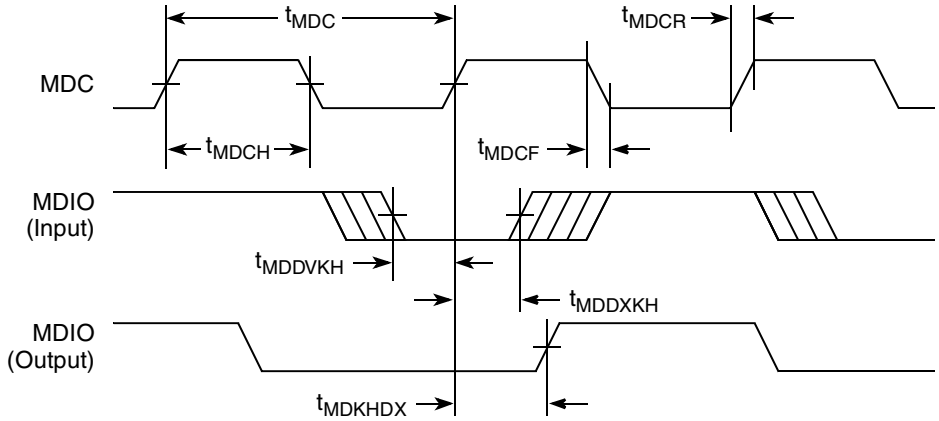


Figure 17. MII management interface timing diagram

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8309.

9.1 TDM/SI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 TDM/SI.

Table 26. TDM/SI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

9.2 TDM/SI AC timing specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 27. TDM/SI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

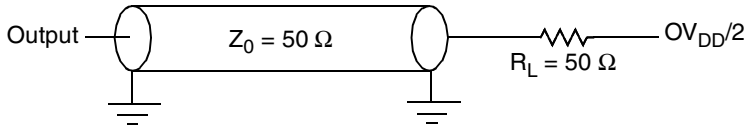


Figure 18. TDM/SI AC test load

13 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8309.

13.1 DUART DC electrical characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8309.

Table 35. DUART DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 DUART AC electrical specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8309.

Table 36. DUART AC timing specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Table 38. eSDHC AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–33.25 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

The following figure provides the eSDHC clock input timing diagram.

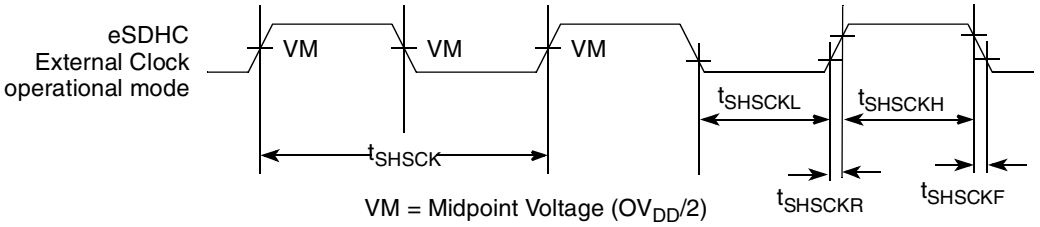


Figure 28. eSDHC clock input timing diagram

The following figure provides the data and command input/output timing diagram.

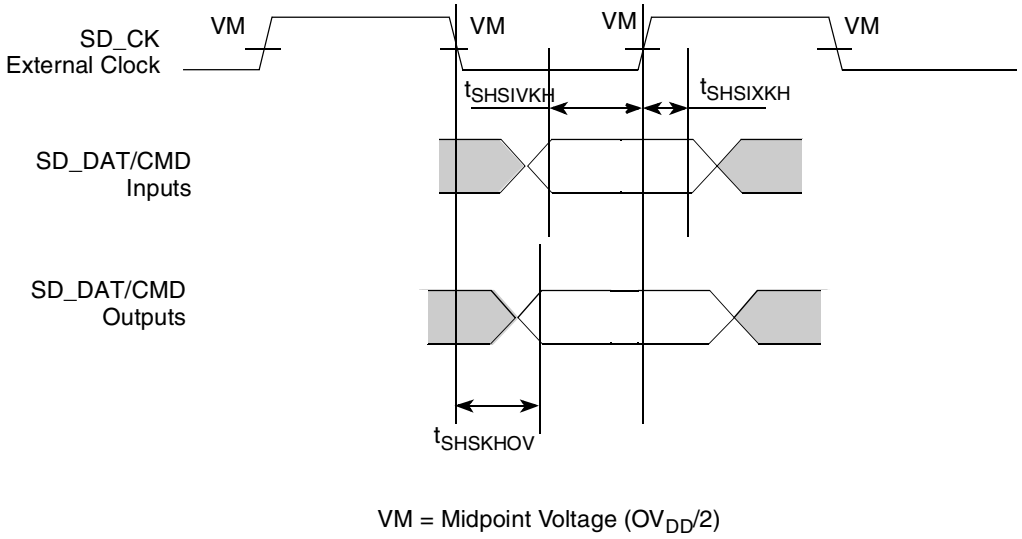


Figure 29. eSDHC data and command input/output timing diagram referenced to clock

15 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

15.1 FlexCAN DC electrical characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 39. FlexCAN DC electrical characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

15.2 FlexCAN AC timing specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 40. FlexCAN AC timing specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8309.

17.1 Timer DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 43. Timer DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

17.2 Timer AC timing specifications

The following table provides the timer input and output AC timing specifications.

Table 44. Timer input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

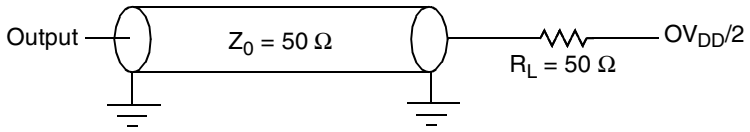
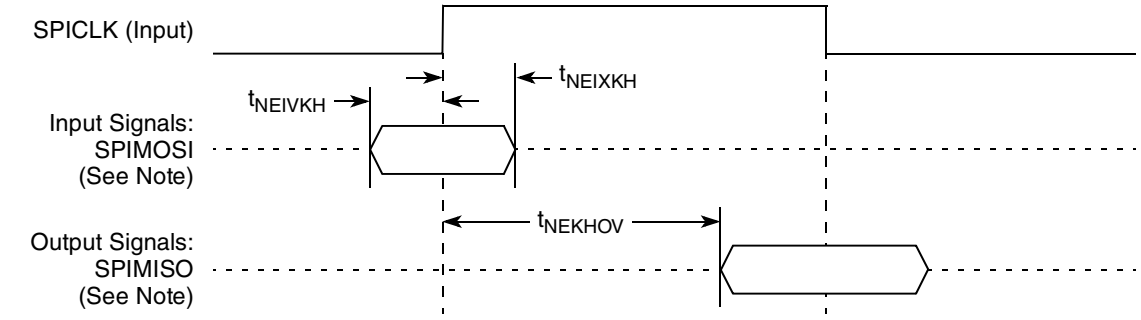


Figure 32. Timers AC test load

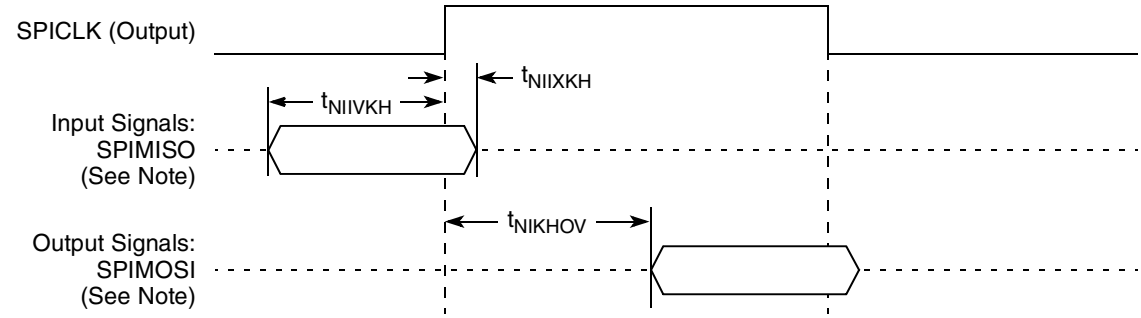
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in slave mode (external clock) diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC timing in master mode (internal clock) diagram

21 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8309.

21.1 JTAG DC electrical characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309.

Table 51. JTAG interface DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

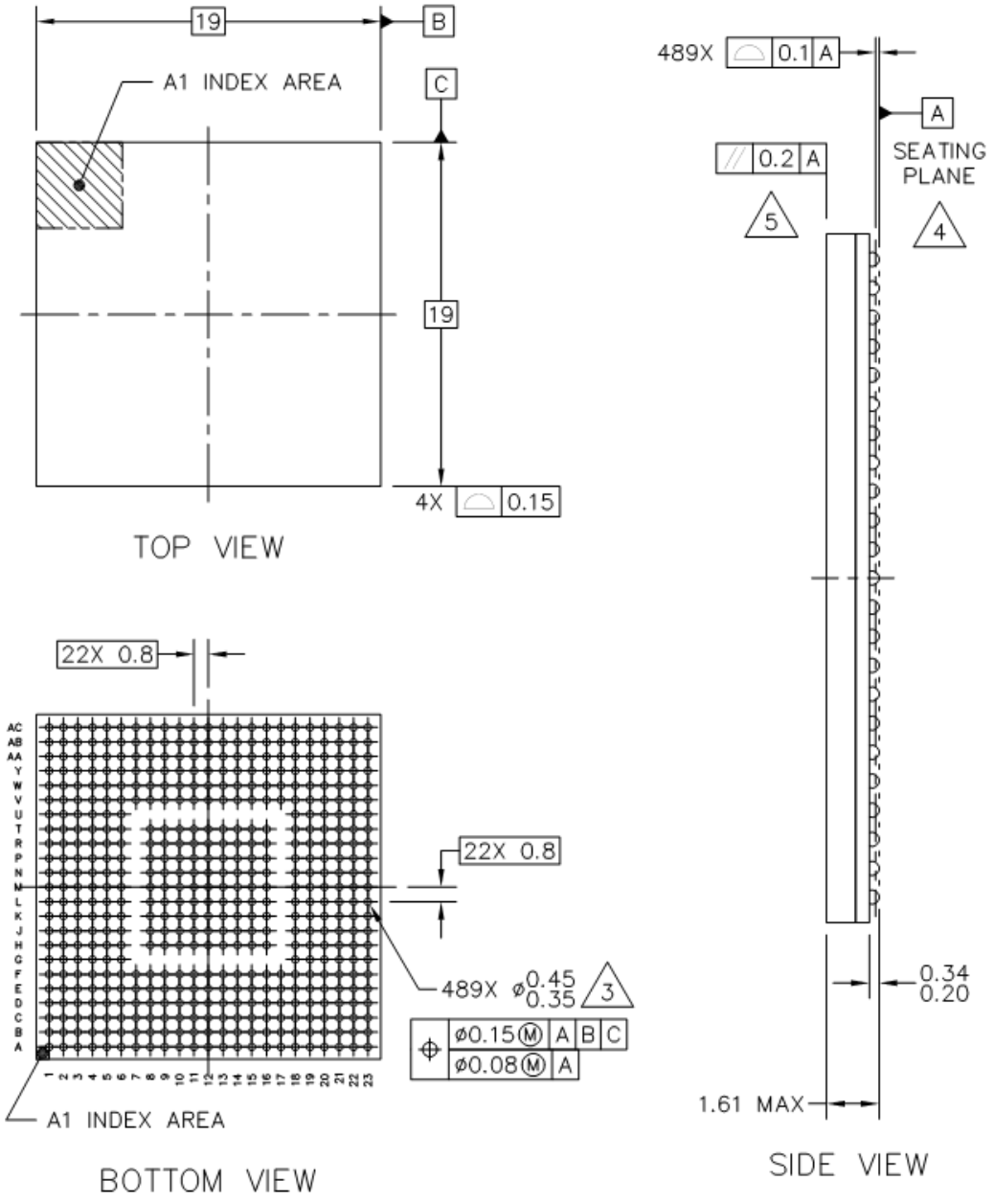


Figure 42. Mechanical dimensions and bottom surface nomenclature of the MPC8309 MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

22.3 Pinout listings

Following table shows the pin list of the MPC8309.

Table 53. MPC8309 pinout listing

Signal	Terminal	Pad Dir	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	U5	IO	GV_{DD}	—
MEMC_MDQ1	AA1	IO	GV_{DD}	—
MEMC_MDQ2	W3	IO	GV_{DD}	—
MEMC_MDQ3	R5	IO	GV_{DD}	—
MEMC_MDQ4	W2	IO	GV_{DD}	—
MEMC_MDQ5	U3	IO	GV_{DD}	—
MEMC_MDQ6	U2	IO	GV_{DD}	—
MEMC_MDQ7	T3	IO	GV_{DD}	—
MEMC_MDQ8	H3	IO	GV_{DD}	—
MEMC_MDQ9	H4	IO	GV_{DD}	—
MEMC_MDQ10	G3	IO	GV_{DD}	—
MEMC_MDQ11	F3	IO	GV_{DD}	—
MEMC_MDQ12	G5	IO	GV_{DD}	—
MEMC_MDQ13	F4	IO	GV_{DD}	—
MEMC_MDQ14	F5	IO	GV_{DD}	—
MEMC_MDQ15	E3	IO	GV_{DD}	—
MEMC_MDQ16	V4	IO	GV_{DD}	—
MEMC_MDQ17	Y2	IO	GV_{DD}	—
MEMC_MDQ18	Y1	IO	GV_{DD}	—
MEMC_MDQ19	U4	IO	GV_{DD}	—
MEMC_MDQ20	V1	IO	GV_{DD}	—
MEMC_MDQ21	R4	IO	GV_{DD}	—
MEMC_MDQ22	U1	IO	GV_{DD}	—
MEMC_MDQ23	T2	IO	GV_{DD}	—
MEMC_MDQ24	J5	IO	GV_{DD}	—
MEMC_MDQ25	G2	IO	GV_{DD}	—
MEMC_MDQ26	G1	IO	GV_{DD}	—
MEMC_MDQ27	F1	IO	GV_{DD}	—
MEMC_MDQ28	E2	IO	GV_{DD}	—

MEMC_MDQ29	D2	IO	GV_{DD}	—
MEMC_MDQ30	C2	IO	GV_{DD}	—
MEMC_MDQ31	C1	IO	GV_{DD}	—
MEMC_MECC0	Y5	IO	GV_{DD}	—
MEMC_MECC1	AA4	IO	GV_{DD}	—
MEMC_MECC2	Y4	IO	GV_{DD}	—
MEMC_MECC3	AA3	IO	GV_{DD}	—
MEMC_MECC4	AC2	IO	GV_{DD}	—
MEMC_MECC5	AB2	IO	GV_{DD}	—
MEMC_MECC6	Y3	IO	GV_{DD}	—
MEMC_MECC7	AB1	IO	GV_{DD}	—
MEMC_MDM0	W1	O	GV_{DD}	—
MEMC_MDM1	E1	O	GV_{DD}	—
MEMC_MDM2	V3	O	GV_{DD}	—
MEMC_MDM3	D1	O	GV_{DD}	—
MEMC_MDM8	W5	O	GV_{DD}	—
MEMC_MDQS0	T5	IO	GV_{DD}	—
MEMC_MDQS1	H5	IO	GV_{DD}	—
MEMC_MDQS2	P5	IO	GV_{DD}	—
MEMC_MDQS3	E5	IO	GV_{DD}	-
MEMC_MDQS8	V5	IO	GV_{DD}	-
MEMC_MBA0	K2	O	GV_{DD}	-
MEMC_MBA1	K3	O	GV_{DD}	-
MEMC_MBA2	N5	O	GV_{DD}	-
MEMC_MA0	L3	O	GV_{DD}	-
MEMC_MA1	L5	O	GV_{DD}	-
MEMC_MA2	L2	O	GV_{DD}	-
MEMC_MA3	L1	O	GV_{DD}	-
MEMC_MA4	M3	O	GV_{DD}	-
MEMC_MA5	M4	O	GV_{DD}	-
MEMC_MA6	M1	O	GV_{DD}	-
MEMC_MA7	N1	O	GV_{DD}	-
MEMC_MA8	N2	O	GV_{DD}	-
MEMC_MA9	N3	O	GV_{DD}	-
MEMC_MA10	L4	O	GV_{DD}	-
MEMC_MA11	P2	O	GV_{DD}	-
MEMC_MA12	N4	O	GV_{DD}	-

MEMC_MA13	P1	O	GV_{DD}	-
MEMC_MWE_B	J1	O	GV_{DD}	-
MEMC_MRAS_B	K1	O	GV_{DD}	-
MEMC_MCAS_B	J3	O	GV_{DD}	-
MEMC_MCS_B0	J4	O	GV_{DD}	-
MEMC_MCS_B1	K5	O	GV_{DD}	-
MEMC_MCKE	P4	O	GV_{DD}	-
MEMC_MCK0	R1	O	GV_{DD}	-
MEMC_MCK1	R3	O	GV_{DD}	-
MEMC_MCK_B0	T1	O	GV_{DD}	-
MEMC_MCK_B1	P3	O	GV_{DD}	-
MEMC_MODT0	H1	O	GV_{DD}	-
MEMC_MODT1	H2	O	GV_{DD}	-
MEMC_MVREF	M6		GV_{DD}	-
Local Bus Controller Interface				
LAD0	B5	IO	OV_{DD}	-
LAD1	A4	IO	OV_{DD}	-
LAD2	C7	IO	OV_{DD}	-
LAD3	D9	IO	OV_{DD}	-
LAD4	A5	IO	OV_{DD}	-
LAD5	E10	IO	OV_{DD}	-
LAD6	A6	IO	OV_{DD}	-
LAD7	C8	IO	OV_{DD}	-
LAD8	D10	IO	OV_{DD}	-
LAD9	A7	IO	OV_{DD}	-
LAD10	B7	IO	OV_{DD}	-
LAD11	C9	IO	OV_{DD}	-
LAD12	E11	IO	OV_{DD}	-
LAD13	B8	IO	OV_{DD}	-
LAD14	A8	IO	OV_{DD}	-
LAD15	C10	IO	OV_{DD}	-
LA16	C11	IO	OV_{DD}	-
LA17	B10	O	OV_{DD}	-
LA18	D12	O	OV_{DD}	-
LA19	A9	O	OV_{DD}	-
LA20	E12	O	OV_{DD}	-
LA21	B11	O	OV_{DD}	-

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1 A20		IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

SPIMISO	E16	IO	OV_{DD}	-
SPICLK E17		IO	OV_{DD}	-
SPISEL	A19	I	OV_{DD}	-
SPISEL_BOOT_B	D18		OV_{DD}	-
JTAG				
TCK	A2	I	OV_{DD}	-
TDI	C5	I	OV_{DD}	2
TDO	A3	O	OV_{DD}	-
TMS	D7	I	OV_{DD}	2
TRST_B	E9	I	OV_{DD}	2
Test Interface				
TEST_MODE	C6	I	OV_{DD}	-
System Control Signals				
HRESET_B	W23	IO	OV_{DD}	1
PORESET_B	W22	I	OV_{DD}	-
Clock Interface				
QE_CLK_IN	R22	I	OV_{DD}	-
SYS_CLK_IN	R23	I	OV_{DD}	-
SYS_XTAL_IN	P23	I	OV_{DD}	-
SYS_XTAL_OUT	P19	O	OV_{DD}	-
PCI_SYNC_IN	T23	I	OV_{DD}	-
PCI_SYNC_OUT	R20	O	OV_{DD}	-
CFG_CLKIN_DIV_B	U23	I	OV_{DD}	-
RTC_PIT_CLOCK	V23	I		
Miscellaneous Signals				
QUIESCE_B	D6	O	OV_{DD}	-
THERM0	E8		OV_{DD}	-
GPIO				
GPIO_0/SD_CLK/MSRCID0 (DDR ID)	E4	IO	OV_{DD}	-
GPIO_1/SD_CMD/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	-
GPIO_2/SD_CD/MSRCID2 (DDR ID)	D3	IO	OV_{DD}	-
GPIO_3/SD_WP/MSRCID3 (DDR ID)	E7	IO	OV_{DD}	-
GPIO_4/SD_DAT0/MSRCID4 (DDR ID)	D4	IO	OV_{DD}	-
GPIO_5/SD_DAT1/MDVAL (DDR ID)	C4	IO	OV_{DD}	-
GPIO_6/SD_DAT2/QE_EXT_REQ_3	B2	IO	OV_{DD}	-
GPIO_7/SD_DAT3/QE_EXT_REQ_1	B3	IO	OV_{DD}	-
GPIO_8/RXCAN1/LSRCID0/LCS_B4	C16	IO	OV_{DD}	-

PCI_AD8/	E21	IO	OV_{DD}	-
PCI_AD9/	H20	IO	OV_{DD}	-
PCI_AD10/	D22	IO	OV_{DD}	-
PCI_AD11/	D23	IO	OV_{DD}	-
PCI_AD12/	J19	IO	OV_{DD}	-
PCI_AD13/	F21	IO	OV_{DD}	-
PCI_AD14/	G21	IO	OV_{DD}	-
PCI_AD15/	E22	IO	OV_{DD}	-
PCI_AD16/	E23	IO	OV_{DD}	-
PCI_AD17/	J20	IO	OV_{DD}	-
PCI_AD18/	F23	IO	OV_{DD}	-
PCI_AD19/	G23	IO	OV_{DD}	-
PCI_AD20	K19	IO	OV_{DD}	-
PCI_AD21	H21	IO	OV_{DD}	-
PCI_AD22	L19	IO	OV_{DD}	-
PCI_AD23	G22	IO	OV_{DD}	-
PCI_AD24	H23	IO	OV_{DD}	-
PCI_AD25	J21	IO	OV_{DD}	-
PCI_AD26	H22	IO	OV_{DD}	-
PCI_AD27	J23	IO	OV_{DD}	-
PCI_AD28	K18	IO	OV_{DD}	-
PCI_AD29	K21	IO	OV_{DD}	-
PCI_AD30	K22	IO	OV_{DD}	-
PCI_AD31	K23	IO	OV_{DD}	-
PCI_C_BE_B0 L20		IO	OV_{DD}	-
PCI_C_BE_B1	L23	IO	OV_{DD}	-
PCI_C_BE_B2 L22		IO	OV_{DD}	-
PCI_C_BE_B3 L21		IO	OV_{DD}	-
PCI_PAR	M19	IO	OV_{DD}	-
PCI_FRAME_B M20		IO	OV_{DD}	-
PCI_TRDY_B M23		IO	OV_{DD}	-
PCI_IRDY_B	M21	IO	OV_{DD}	-
PCI_STOP_B	N23	IO	OV_{DD}	-
PCI_DEVSEL_B N22		IO	OV_{DD}	-
PCI_IDSEL N21		IO	OV_{DD}	-
PCI_SERR_B	N19	IO	OV_{DD}	-
PCI_PERR_B P20		IO	OV_{DD}	-

23.1 Clocking in PCI host mode

When the MPC8309 is configured as a PCI host device (RCWH[PCIHOST] = 1), SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK multiplexors. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

23.1.1 PCI clock outputs (PCI_CLK[0:2])

When the MPC8309 is configured as a PCI host, it provides three separate clock output signals, PCI_CLK[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

23.2 Clocking in PCI agent mode

When the MPC8309 is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock. In agent mode, the SYS_CLK_IN signal should be tied to GND, and the clock output signals, PCI_CLK*n* and PCI_SYNC_OUT, are not used.

23.3 System clock domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF} \qquad \textit{Eqn. 1}$$

In PCI host mode,

$$PCI\_SYNC\_IN = SYS\_CLK\_IN \div (1 + \sim\overline{CFG\_CLKIN\_DIV}) . \qquad \textbf{Eqn. 2}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset

Table 58. e300 Core PLL configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

23.6 QUICC Engine PLL configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 59. QUICC Engine PLL multiplication factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 60. QUICC Engine PLL VCO divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved