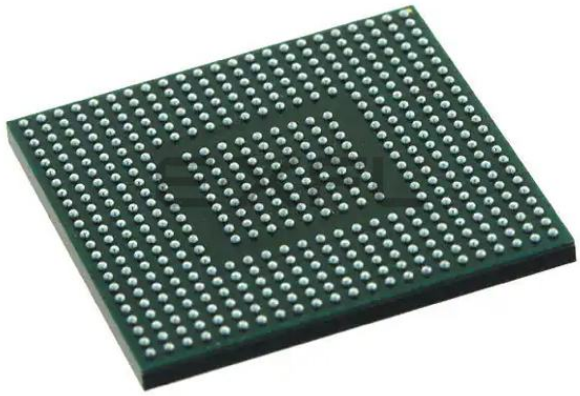

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309cvmagdca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

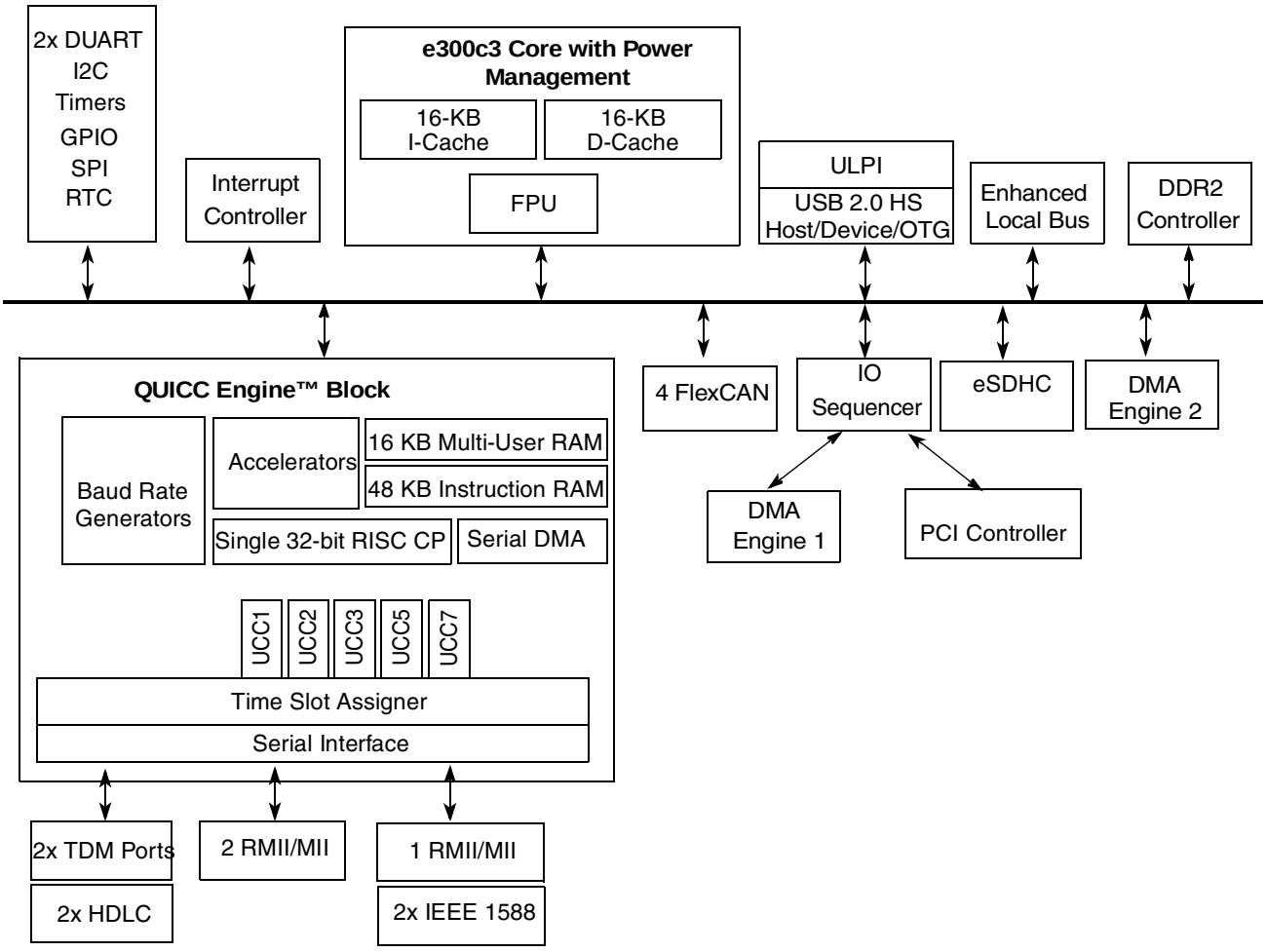

Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine1
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- IO Sequencer

- Direct memory access (DMA) controller (DMA Engine 2)
  - Four independent fully programmable DMA channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Misaligned transfer capability for source/destination address
  - Data chaining and direct mode
  - Interrupt on completed segment, error, and chain
- DUART
  - Supports 2 DUART
  - Each has two 2-wire interfaces (RxD, TxD)
    - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- Power management controller (PMC)
  - Supports core doze/nap/sleep/ power management
  - Exits low power state and returns to full-on mode when
    - The core internal time base unit invokes a request to exit low power state
    - The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
  - General-purpose I/O (GPIO)
    - 56 parallel I/O pins multiplexed on various chip interfaces
    - Interrupt capability
- System timers
  - Periodic interrupt timer
  - Software watchdog timer
  - Eight general-purpose timers
- Real time clock (RTC) module
  - Maintains a one-second count, unique over a period of thousands of years
  - Two possible clock sources:
    - External RTC clock (RTC_PIT_CLK)
    - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8309. The MPC8309 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC electrical characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute maximum ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

Table 9. RESET initialization timing specifications (continued)

Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL lock times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

5.1 Reset signals DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 reset signals mentioned in Table 9.

Table 11. Reset signals DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	— ±	5	µA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8309. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC electrical characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8309 when GV_{DD}(typ) = 1.8 V.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 16. DDR2 SDRAM output AC timing specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.4 2.5	 — 	ns	3
$\overline{MCS}$ output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.4 2.5	 — 	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.8 0.9	 — 	ns	5
MDQ/MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100	 — 	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

The following figure shows the RMII receive AC timing diagram.

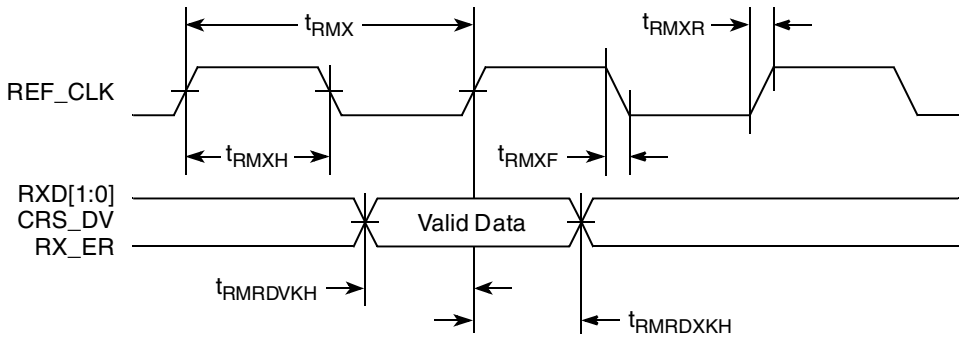

Figure 16. RMII receive AC timing diagram

8.3 Ethernet management interface electrical characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics."

8.3.1 MII management DC electrical characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII management DC electrical characteristics when powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII management AC electrical specifications

The following table provides the MII management AC timing specifications.

Table 25. MII management AC timing specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

Table 34. USB general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

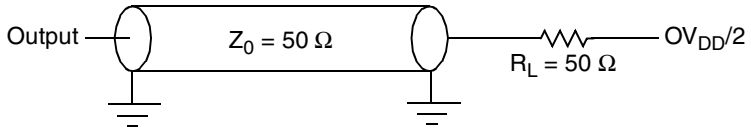

Figure 26. USB AC test load

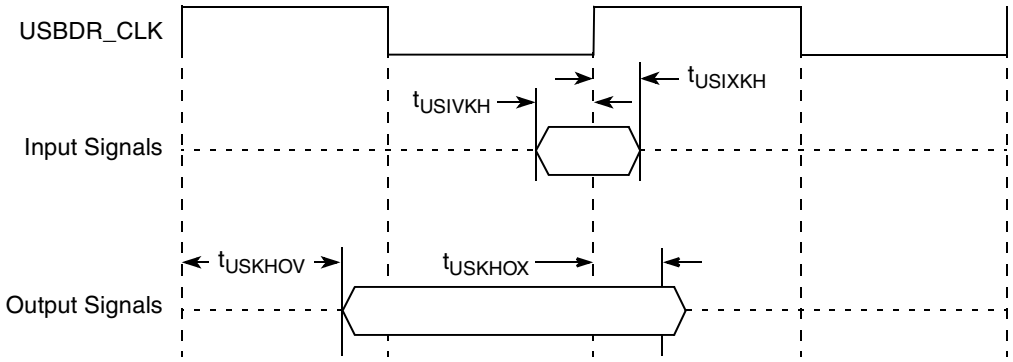

Figure 27. USB signals

14 eSDHC

This section describes the DC and AC electrical specifications for the eSDHC interface of the device.

14.1 eSDHC DC electrical characteristics

The following table provides the DC electrical characteristics for the eSDHC interface.

Table 37. eSDHC Interface DC electrical characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times OV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times OV_{DD}$	V	1
Output high voltage	V_{OH}	I_{OH} = –100 µA at OV_{DD} min	$0.75 \times OV_{DD}$	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 µA at OV_{DD} min	—	$0.125 \times OV_{DD}$	V	—
Output high voltage	V_{OH}	I_{OH} = –100 mA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	µA	—

Notes:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2..
2. Open drain mode for MMC cards only.

14.2 eSDHC AC timing specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 28 and Figure 29.

Table 38. eSDHC AC timing specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	25/33.25 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	4

15 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

15.1 FlexCAN DC electrical characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 39. FlexCAN DC electrical characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

15.2 FlexCAN AC timing specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 40. FlexCAN AC timing specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

Table 49. SPI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

20.2 SPI AC timing specifications

The following table and provide the SPI input and output AC timing specifications.

Table 50. SPI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8309_output_port spimosi_lpgl0(SPI Master mode)
4. Delay units must not be enabled for Slave mode.

The following figure provides the AC test load for the SPI.

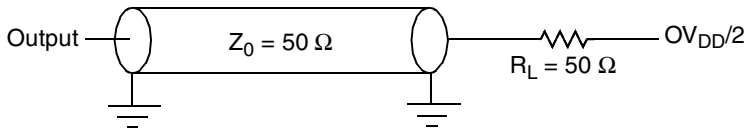

Figure 34. SPI AC test load

Figure 35 and Figure 36 represent the AC timing from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 52. JTAG AC timing specifications (independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	2	—		5
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 37). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8309.

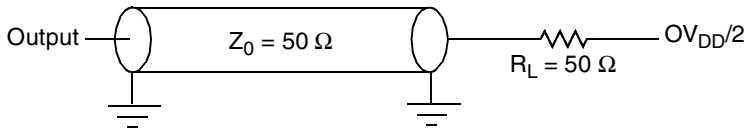

Figure 37. AC test load for the JTAG interface

The following figure provides the JTAG clock input timing diagram.

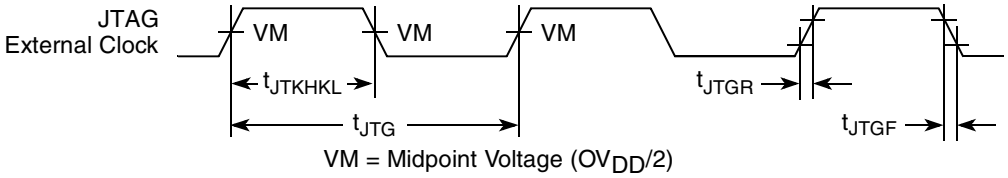

Figure 38. JTAG clock input timing diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

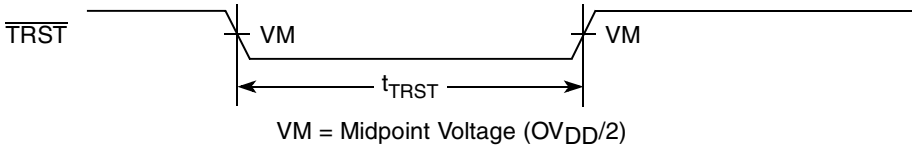

Figure 39. $\overline{\text{TRST}}$ timing diagram

22 Package and pin listings

This section details package parameters, pin assignments, and dimensions. The MPC8309 is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 22.1, “Package parameters for the MPC8309,” and Section 22.2, “Mechanical dimensions of the MPC8309 MAPBGA,” for information on the MAPBGA.

22.1 Package parameters for the MPC8309

The package parameters are as provided in the following list.

Package outline	19 mm × 19 mm
Package Type	MAPBGA
Interconnects	489
Pitch	0.80 mm
Module height (typical)	1.48 mm; Min = 1.31mm and Max 1.61mm
Solder Balls	96 Sn / 3.5 Ag / 0.5 Cu (VM package)
Ball diameter (typical)	0.40 mm

22.2 Mechanical dimensions of the MPC8309 MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8309, 489-MAPBGA package.

MEMC_MDQ29	D2	IO	GV_{DD}	—
MEMC_MDQ30	C2	IO	GV_{DD}	—
MEMC_MDQ31	C1	IO	GV_{DD}	—
MEMC_MECC0	Y5	IO	GV_{DD}	—
MEMC_MECC1	AA4	IO	GV_{DD}	—
MEMC_MECC2	Y4	IO	GV_{DD}	—
MEMC_MECC3	AA3	IO	GV_{DD}	—
MEMC_MECC4	AC2	IO	GV_{DD}	—
MEMC_MECC5	AB2	IO	GV_{DD}	—
MEMC_MECC6	Y3	IO	GV_{DD}	—
MEMC_MECC7	AB1	IO	GV_{DD}	—
MEMC_MDM0	W1	O	GV_{DD}	—
MEMC_MDM1	E1	O	GV_{DD}	—
MEMC_MDM2	V3	O	GV_{DD}	—
MEMC_MDM3	D1	O	GV_{DD}	—
MEMC_MDM8	W5	O	GV_{DD}	—
MEMC_MDQS0	T5	IO	GV_{DD}	—
MEMC_MDQS1	H5	IO	GV_{DD}	—
MEMC_MDQS2	P5	IO	GV_{DD}	—
MEMC_MDQS3	E5	IO	GV_{DD}	-
MEMC_MDQS8	V5	IO	GV_{DD}	-
MEMC_MBA0	K2	O	GV_{DD}	-
MEMC_MBA1	K3	O	GV_{DD}	-
MEMC_MBA2	N5	O	GV_{DD}	-
MEMC_MA0	L3	O	GV_{DD}	-
MEMC_MA1	L5	O	GV_{DD}	-
MEMC_MA2	L2	O	GV_{DD}	-
MEMC_MA3	L1	O	GV_{DD}	-
MEMC_MA4	M3	O	GV_{DD}	-
MEMC_MA5	M4	O	GV_{DD}	-
MEMC_MA6	M1	O	GV_{DD}	-
MEMC_MA7	N1	O	GV_{DD}	-
MEMC_MA8	N2	O	GV_{DD}	-
MEMC_MA9	N3	O	GV_{DD}	-
MEMC_MA10	L4	O	GV_{DD}	-
MEMC_MA11	P2	O	GV_{DD}	-
MEMC_MA12	N4	O	GV_{DD}	-

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1 A20		IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

GPIO_9/TXCAN1/LSRCID1/LCS_B5	C17	IO	OV_{DD}	-
GPIO_10/RXCAN2/LSRCID2/LCS_B6	E15	IO	OV_{DD}	-
GPIO_11/TXCAN2/LSRCID3/LCS_B7	A18	IO	OV_{DD}	-
GPIO_12/RXCAN3/LSRCID4/LCLK1	D15	IO	OV_{DD}	-
GPIO_13/TXCAN3/LDVAL	C18	IO	OV_{DD}	-
GPIO_14/RXCAN4	D16	IO	OV_{DD}	-
GPIO_15/TXCAN4	C19	IO	OV_{DD}	-
USB				
USBDR_PWRFAULT/CE_PIO_1	AA6	I	OV_{DD}	1
USBDR_CLK/UART2_SIN2/UART2_CTS_B1	AC9	I	OV_{DD}	-
USBDR_DIR	AA7	I	OV_{DD}	-
USBDR_NXT/UART2_SIN1/QE_EXT_REQ_4	AC5	I	OV_{DD}	-
USBDR_TXDRXD0/GPIO_32	Y6	IO	OV_{DD}	-
USBDR_TXDRXD1/GPIO_33	W9	IO	OV_{DD}	-
USBDR_TXDRXD2/GPIO_34/QE_BRG_1	AB5	IO	OV_{DD}	-
USBDR_TXDRXD3/GPIO_35/QE_BRG_2	AA5	IO	OV_{DD}	-
USBDR_TXDRXD4/GPIO_36/QE_BRG_3	Y8	IO	OV_{DD}	-
USBDR_TXDRXD5/GPIO_37/QE_BRG_4	AC4	IO	OV_{DD}	-
USBDR_TXDRXD6/GPIO_38/QE_BRG_9	AC3	IO	OV_{DD}	-
USBDR_TXDRXD7/GPIO_39/QE_BRG_11	AB3	IO	OV_{DD}	-
USBDR_PCTL0/UART2_SOUT1/LB_POR_CFG_BOOT_ECC	W8	O	OV_{DD}	-
USBDR_PCTL1/UART2_SOUT2/UART2_RTS_B1/LB_POR_BOOT_ERR	W7	O	OV_{DD}	-
USBDR_STP/QE_EXT_REQ_2	W6	O	OV_{DD}	-
PCI				
PCI_INTA_B	B22	O	OV_{DD}	-
PCI_RESET_OUT_B	F19	O	OV_{DD}	-
PCI_AD0	B23	IO	OV_{DD}	-
PCI_AD1	C21	IO	OV_{DD}	-
PCI_AD2	E20	IO	OV_{DD}	-
PCI_AD3	G19	IO	OV_{DD}	-
PCI_AD4	C23	IO	OV_{DD}	-
PCI_AD5	H19	IO	OV_{DD}	-
PCI_AD6/CE_PIO_0	D21	IO	OV_{DD}	-
PCI_AD7	F20	IO	OV_{DD}	-

Table 55. Operating Frequencies for MAPBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR2 memory bus frequency (MCLK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

23.4 System PLL configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

Table 56. System PLL multiplication factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 23, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 58. e300 Core PLL configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

23.6 QUICC Engine PLL configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 59. QUICC Engine PLL multiplication factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 60. QUICC Engine PLL VCO divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

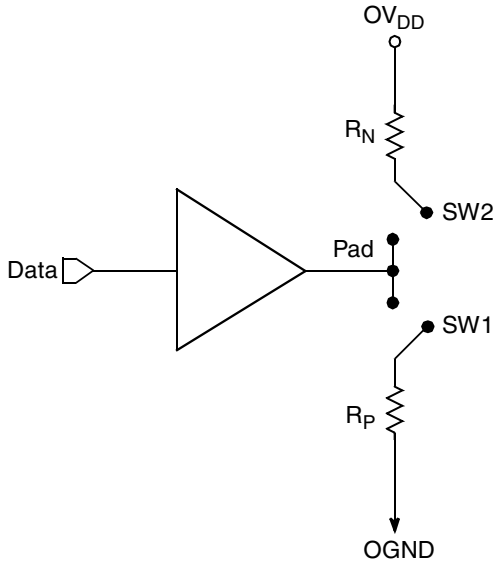

Figure 45. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

27 Document revision history

The following table provides a revision history for this document.

Table 66. Document revision history

Rev. No.	Date	Substantive Change(s)
2	09/2012	• In Table 53, swapped CLK13 and CLK14. • In Table 53, removed the following test signals, as there are no corresponding use cases: – ECID_TMODE_IN – BOOT_ROM_ADDR[2] to BOOT_ROM_ADDR[12] – BOOT_ROM_RDATA[0] to BOOT_ROM_RDATA[31] – BOOT_ROM_MOD_EN, BOOT_ROM_RWB, BOOT_ROM_XFR_WAIT, BOOT_ROM_XFR_ERR – UC1_RM, UC2_RM, UC3_RM, UC5_RM, UC7_RM, AND URM_TRIG – TPR_SYS_AAD[0] to TPR_SYS_AAD[15] – TPR_SYS_SYNC, TPR_SYS_DACK – QE_TRB_0, QE_TRB_1 – PLLCZ_CORE_CLKIN – JTAG_BISE, JTAG_PRPGPS, JTAG_BISR_TDO_EN – CLOCK_XLB_CLOCK_OUT – PD_XLB2MG_DDR_CLOCK • In Table 53, changed the following signal names as only QE-Based Fast Ethernet Controller is present in this device: – TSEC_TMR_TRIG1 to FEC_TMR_TRIG1 – TSEC_TMR_TRIG2 to FEC_TMR_TRIG2 – TSEC_TMR_CLK to FEC_TMR_CLK – TSEC_TMR_GCLK to FEC_TMR_GCLK – TSEC_TMR_PP1 to FEC_TMR_PP1 – TSEC_TMR_PP2 to FEC_TMR_PP2 – TSEC_TMR_PP3 to FEC_TMR_PP3 – TSEC_TMR_ALARM1 to FEC_TMR_ALARM1 – TSEC_TMR_ALARM2 to FEC_TMR_ALARM2 – FEC3_TMR_TX_ESFD to FEC2_TMR_TX_ESFD – FEC3_TMR_RX_ESFD to FEC2_TMR_RX_ESFD. • In Table 18, added parameteres $t_{LALEHOV}$,, $t_{LALETOT}$, and t_{LBOTOT} and made the corresponding updates in Figure 8 • In Figure 3, replaced "32 X tSYS_CLK_IN" with "32 X tSYS_CLK_IN/PCI_SYNC_IN.
1	08/2011	• Updated QUICC Engine frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 61. • Updated CEPMF and CEDF as per new QE frequency in Table 61. • Updated QUICC Engine frequency to 233 MHz in Table 64. • Corrected LCCR to LCRR for all instances.
0	03/2011	Initial Release.