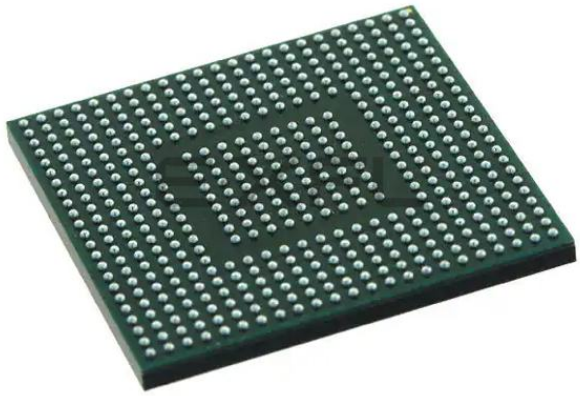

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	417MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309cvmahfca

2.1.2 Power supply voltage specification

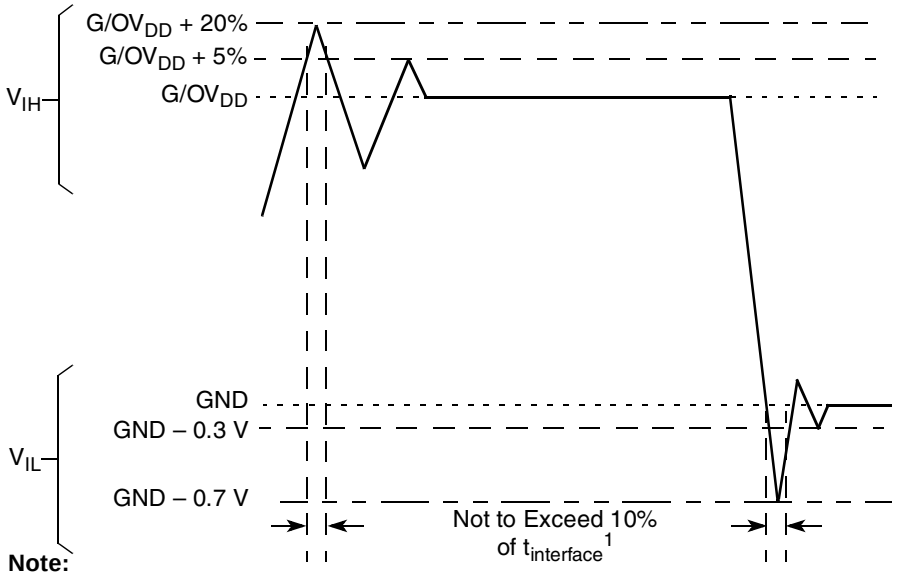
The following table provides the recommended operating conditions for the MPC8309. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	1.0 V ± 50 mV	V	1
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V ± 100 mV	V	1
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN,USB and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1, 3
Junction temperature	T_A/T_J	0 to 105	°C	2

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A(Ambient Temperature); maximum temperature is specified with T_J(Junction Temperature).
3. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8309



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot voltage for GV_{DD}/OV_{DD}

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O power dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.149	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.415	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, PCI, SPI, Timer output, FlexCAN, eSDHC				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock input timing

This section provides the clock input DC and AC electrical characteristics for the MPC8309.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC electrical characteristics

The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC electrical characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

Table 15. DDR2 SDRAM input AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the input timing diagram for the DDR controller.

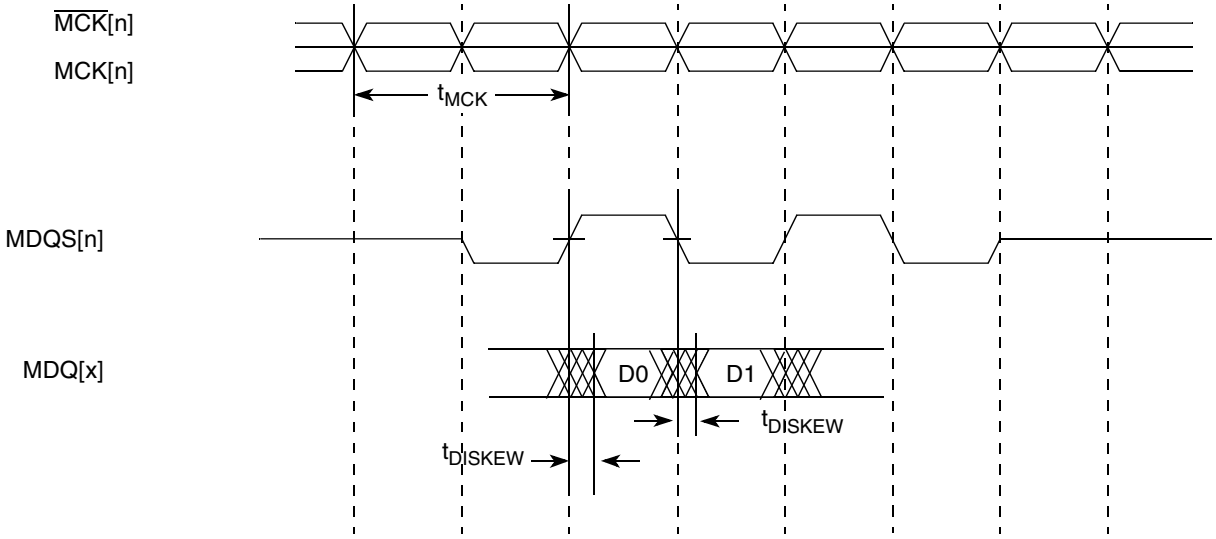


Figure 4. DDR input timing diagram

6.2.2 DDR2 SDRAM output AC timing specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM output AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK cycle time, (MCK/$\overline{MCK}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

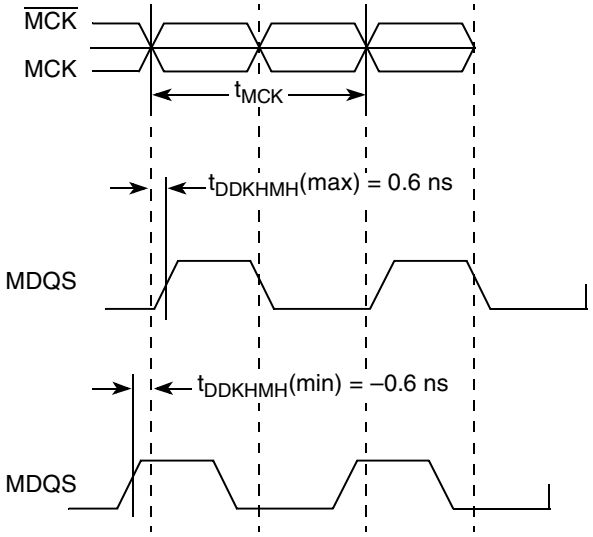


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

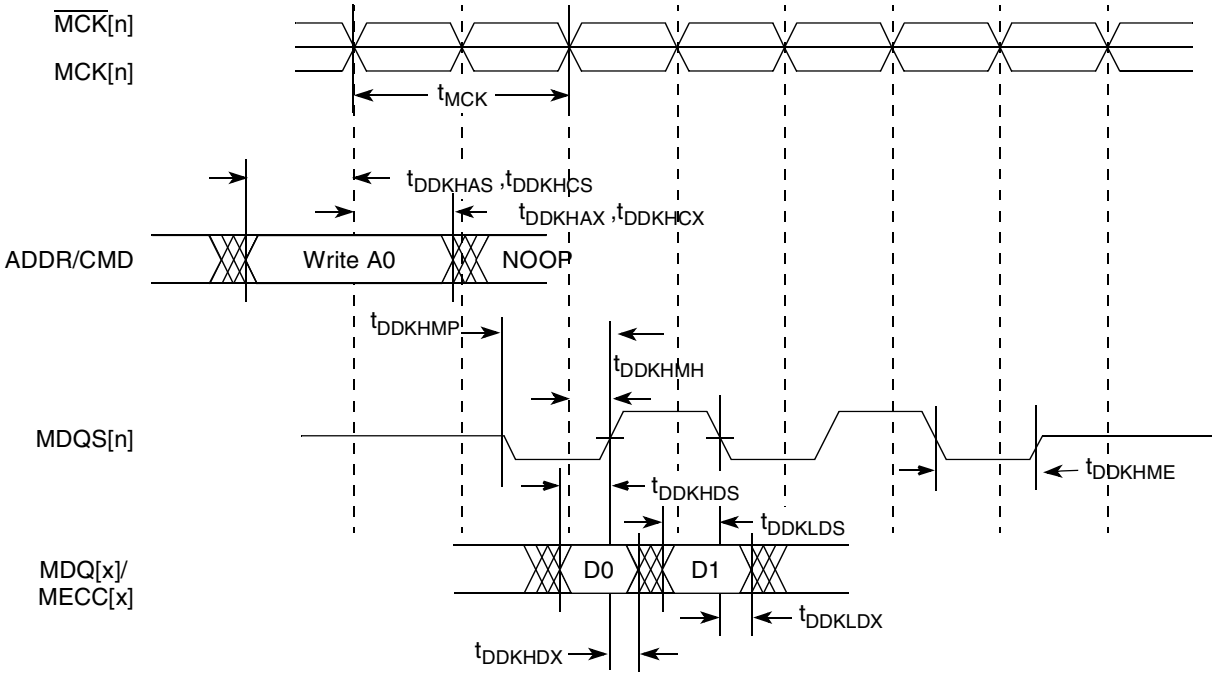


Figure 6. DDR2 SDRAM output timing diagram

Table 19. MII and RMII DC electrical characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC timing specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII transmit AC timing specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min) t	MTXF	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

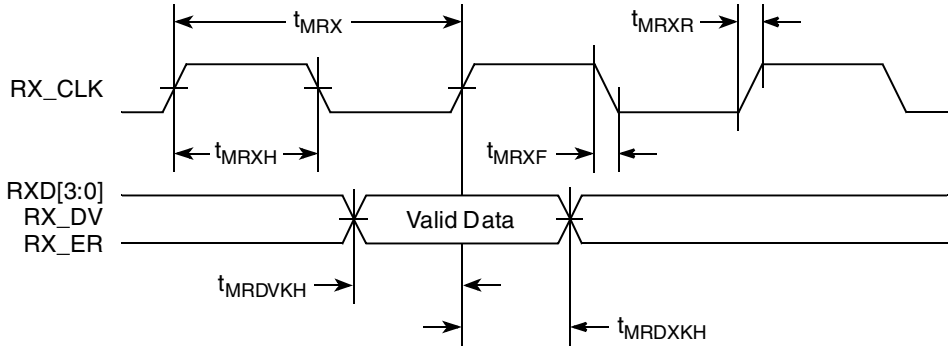


Figure 13. MII receive AC timing diagram

8.2.2 RMII AC timing specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII transmit AC timing specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13 ns	
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min) t	RMXF	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

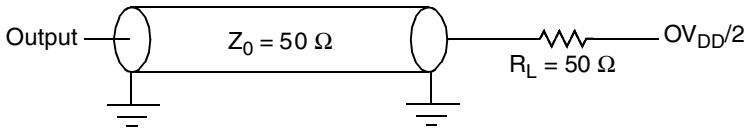


Figure 14. AC test load

The following figure shows the RMII receive AC timing diagram.

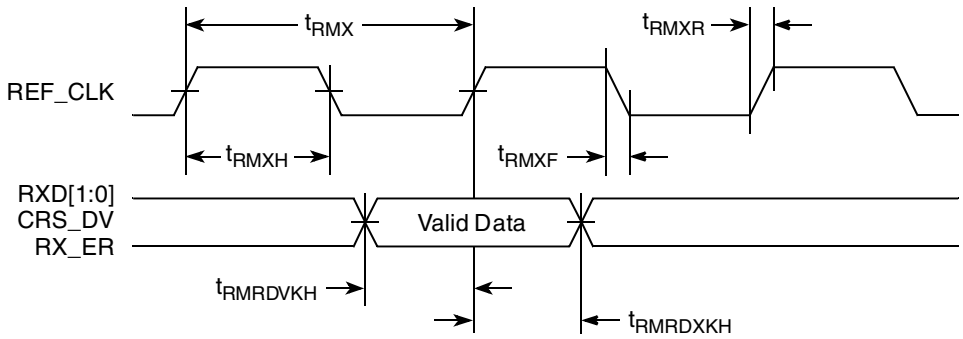


Figure 16. RMII receive AC timing diagram

8.3 Ethernet management interface electrical characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics."

8.3.1 MII management DC electrical characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII management DC electrical characteristics when powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII management AC electrical specifications

The following table provides the MII management AC timing specifications.

Table 25. MII management AC timing specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

Table 31. PCI AC timing specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Table 32. PCI AC timing specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 23 provides the AC test load for PCI.

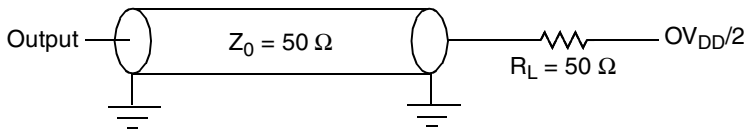


Figure 23. PCI AC test load

Figure 24 shows the PCI input AC timing conditions.

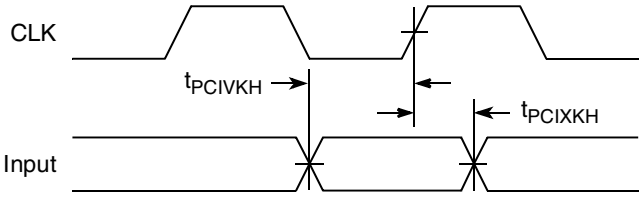


Figure 24. PCI input AC timing measurement conditions

Figure 25 shows the PCI output AC timing conditions.

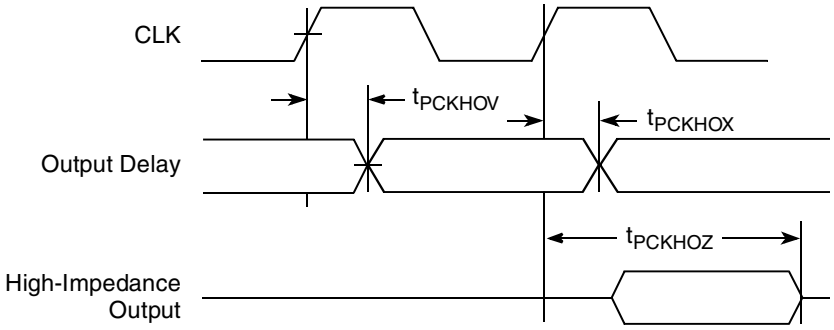


Figure 25. PCI output AC timing measurement condition

12 USB

12.1 USB controller

This section provides the AC and DC electrical specifications for the USB (ULPI) interface.

12.1.1 USB DC electrical characteristics

The following table provides the DC electrical characteristics for the USB interface.

Table 33. USB DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

12.1.2 USB AC electrical specifications

The following table describes the general timing parameters of the USB interface.

15 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

15.1 FlexCAN DC electrical characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 39. FlexCAN DC electrical characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

15.2 FlexCAN AC timing specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 40. FlexCAN AC timing specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8309.

18.1 GPIO DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 GPIO.

Table 45. GPIO DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

18.2 GPIO AC timing specifications

The following table provides the GPIO input and output AC timing specifications.

Table 46. GPIO input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

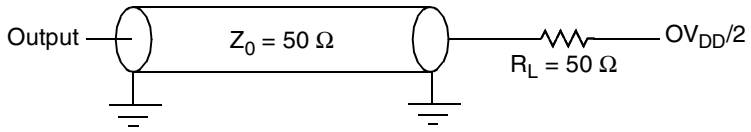


Figure 33. GPIO AC test load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8309.

19.1 IPIC DC electrical characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8309.

Table 47. IPIC DC electrical characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC timing specifications

The following table provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

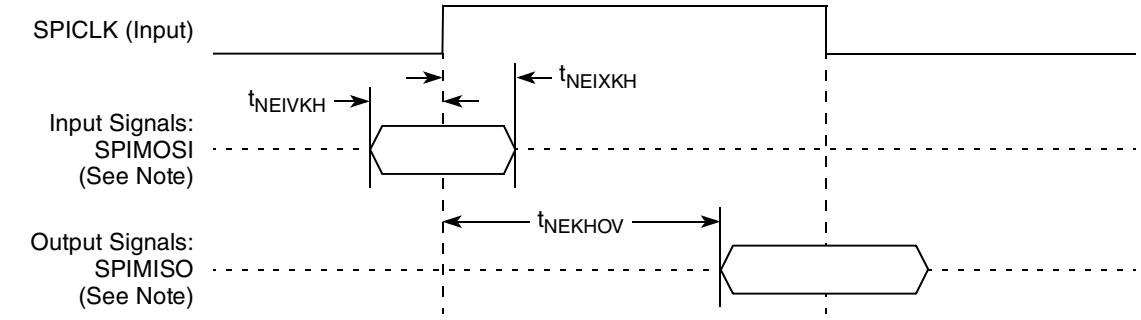
20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8309.

20.1 SPI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 SPI.

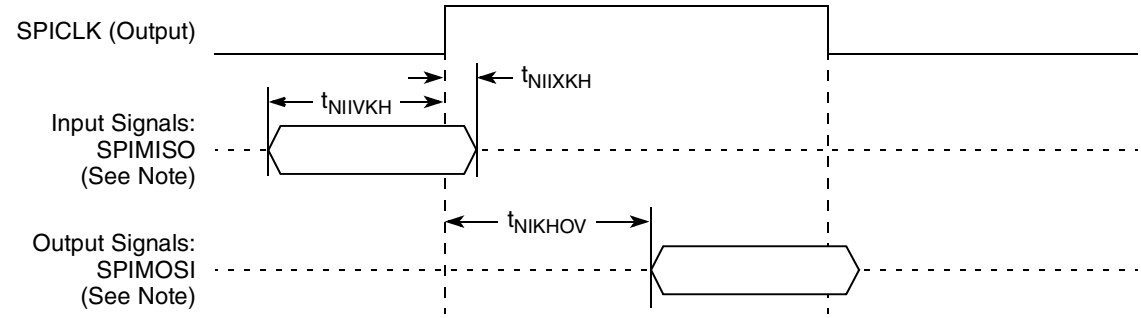
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in slave mode (external clock) diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC timing in master mode (internal clock) diagram

21 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8309.

21.1 JTAG DC electrical characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309.

Table 51. JTAG interface DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

SPIMISO	E16	IO	OV_{DD}	-
SPICLK E17		IO	OV_{DD}	-
SPISEL	A19	I	OV_{DD}	-
SPISEL_BOOT_B	D18		OV_{DD}	-
JTAG				
TCK	A2	I	OV_{DD}	-
TDI	C5	I	OV_{DD}	2
TDO	A3	O	OV_{DD}	-
TMS	D7	I	OV_{DD}	2
TRST_B	E9	I	OV_{DD}	2
Test Interface				
TEST_MODE	C6	I	OV_{DD}	-
System Control Signals				
HRESET_B	W23	IO	OV_{DD}	1
PORESET_B	W22	I	OV_{DD}	-
Clock Interface				
QE_CLK_IN	R22	I	OV_{DD}	-
SYS_CLK_IN	R23	I	OV_{DD}	-
SYS_XTAL_IN	P23	I	OV_{DD}	-
SYS_XTAL_OUT	P19	O	OV_{DD}	-
PCI_SYNC_IN	T23	I	OV_{DD}	-
PCI_SYNC_OUT	R20	O	OV_{DD}	-
CFG_CLKIN_DIV_B	U23	I	OV_{DD}	-
RTC_PIT_CLOCK	V23	I		
Miscellaneous Signals				
QUIESCE_B	D6	O	OV_{DD}	-
THERM0	E8		OV_{DD}	-
GPIO				
GPIO_0/SD_CLK/MSRCID0 (DDR ID)	E4	IO	OV_{DD}	-
GPIO_1/SD_CMD/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	-
GPIO_2/SD_CD/MSRCID2 (DDR ID)	D3	IO	OV_{DD}	-
GPIO_3/SD_WP/MSRCID3 (DDR ID)	E7	IO	OV_{DD}	-
GPIO_4/SD_DAT0/MSRCID4 (DDR ID)	D4	IO	OV_{DD}	-
GPIO_5/SD_DAT1/MDVAL (DDR ID)	C4	IO	OV_{DD}	-
GPIO_6/SD_DAT2/QE_EXT_REQ_3	B2	IO	OV_{DD}	-
GPIO_7/SD_DAT3/QE_EXT_REQ_1	B3	IO	OV_{DD}	-
GPIO_8/RXCAN1/LSRCID0/LCS_B4	C16	IO	OV_{DD}	-

FEC2_RX_CLK[CLK7]/GPIO_34	W14	IO	OV_{DD}	-
FEC2_RX_DV/GTM2_TIN2/GPIO_35	AB16	IO	OV_{DD}	-
FEC2_RX_ER/GTM2_TGATE2_B/GPIO_36	Y14	IO	OV_{DD}	-
FEC2_RXD0/GPIO_37	AA15	IO	OV_{DD}	-
FEC2_RXD1/GTM2_TIN3/GPIO_38	AC15	IO	OV_{DD}	-
FEC2_RXD2/GTM2_TGATE3_B/GPIO_39	AC16	IO	OV_{DD}	-
FEC2_RXD3/GPIO_40	AA14	IO	OV_{DD}	-
FEC2_TX_CLK[CLK8]/GTM2_TIN4/GPIO_41	W13	IO	OV_{DD}	-
FEC2_TX_EN/GTM2_TGATE4_B/GPIO_42	AB14	IO	OV_{DD}	-
FEC2_TX_ER/GTM2_TOUT4_B/GPIO_43	AC14	IO	OV_{DD}	-
FEC2_TXD0/GTM2_TOUT1_B/GPIO_44	Y12	IO	OV_{DD}	-
FEC2_TXD1/GTM2_TOUT2_B/GPIO_45	AA13	IO	OV_{DD}	-
FEC2_TXD2/GTM2_TOUT3_B/GPIO_46	AB13	IO	OV_{DD}	-
FEC2_TXD3/GPIO_47	AC13	IO	OV_{DD}	-
FEC3_COL/GPIO_48	AC12	IO	OV_{DD}	-
FEC3_CRS/GPIO_49	W11	IO	OV_{DD}	-
FEC3_RX_CLK[CLK11]/GPIO_50	W12	IO	OV_{DD}	-
FEC3_RX_DV/FEC1_TMR_TX_ESFD/GPIO_51	AA12	IO	OV_{DD}	-
FEC3_RX_ER/FEC1_TMR_RX_ESFD/GPIO_52	AB11	IO	OV_{DD}	-
FEC3_RXD0/FEC2_TMR_TX_ESFD/GPIO_53	AA11	IO	OV_{DD}	-
FEC3_RXD1/FEC2_TMR_RX_ESFD/GPIO_54	AC11	IO	OV_{DD}	-
FEC3_RXD2/FEC_TMR_TRIG1/GPIO_55	Y11	IO	OV_{DD}	-
FEC3_RXD3/FEC_TMR_TRIG2/GPIO_56	AB10	IO	OV_{DD}	-
FEC3_TX_CLK[CLK12]/FEC_TMR_CLK/GPIO_57	AC10	IO	OV_{DD}	-
FEC3_TX_EN/FEC_TMR_GCLK/GPIO_58	AA10	IO	OV_{DD}	-
FEC3_TX_ER/FEC_TMR_PP1/GPIO_59	AC8	IO	OV_{DD}	-
FEC3_TXD0/FEC_TMR_PP2/GPIO_60	AB8	IO	OV_{DD}	-
FEC3_TXD1/FEC_TMR_PP3/GPIO_61	AA9	IO	OV_{DD}	-
FEC3_TXD2/FEC_TMR_ALARM1/GPIO_62	AA8	IO	OV_{DD}	-
FEC3_TXD3/FEC_TMR_ALARM2/GPIO_63	AC7	IO	OV_{DD}	-

23 Clocking

The following figure shows the internal distribution of clocks within the MPC8309.

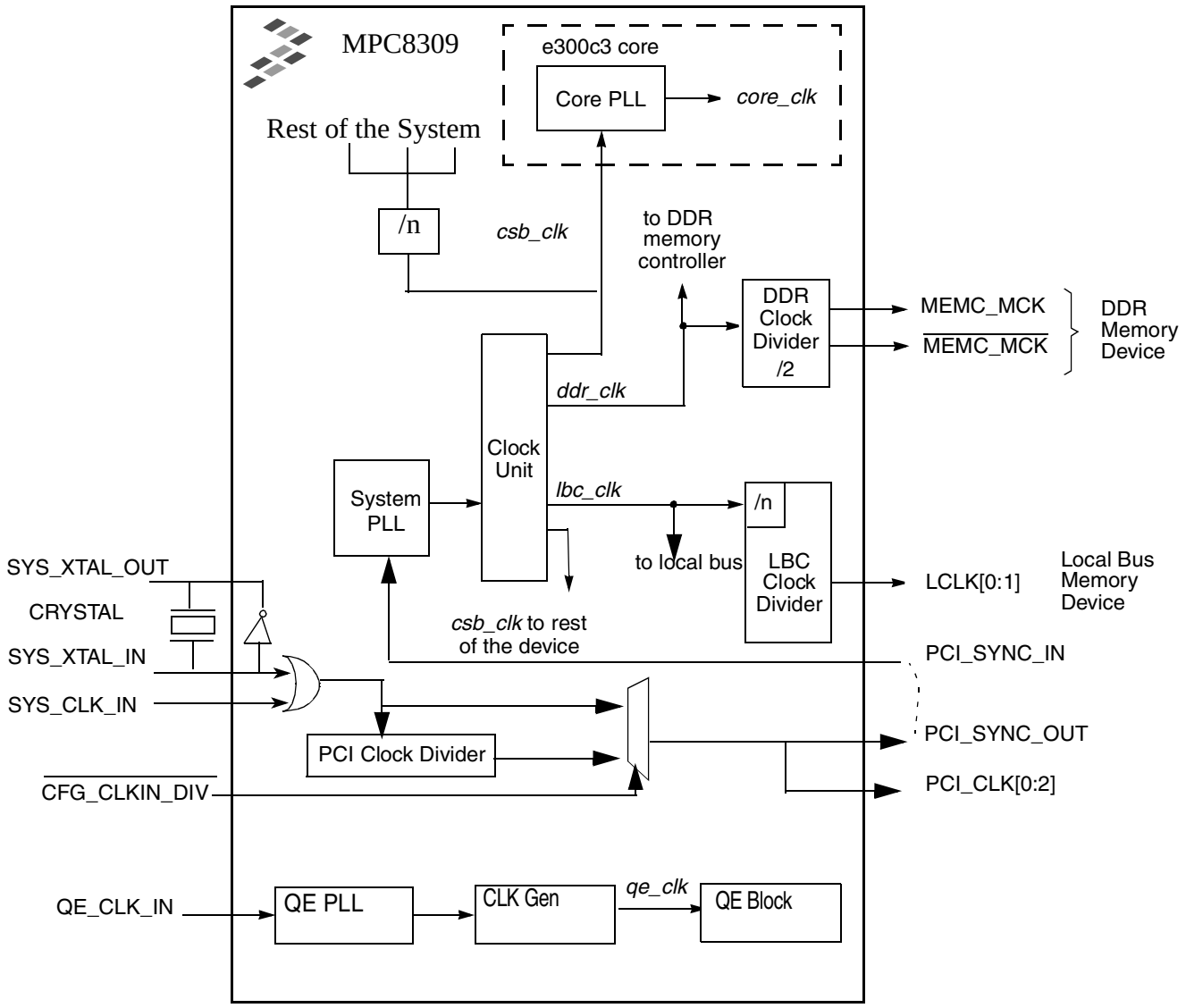


Figure 43. MPC8309 clock subsystem

The primary clock source for the MPC8309 can be one of three inputs,Crystal(SYS_XTAL_IN), SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

Table 57. CSB frequency options

SPMF	csb_clk : sys_clk_in Ratio	PCI_SYNC_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

23.5 Core PLL configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 58. e300 Core PLL configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

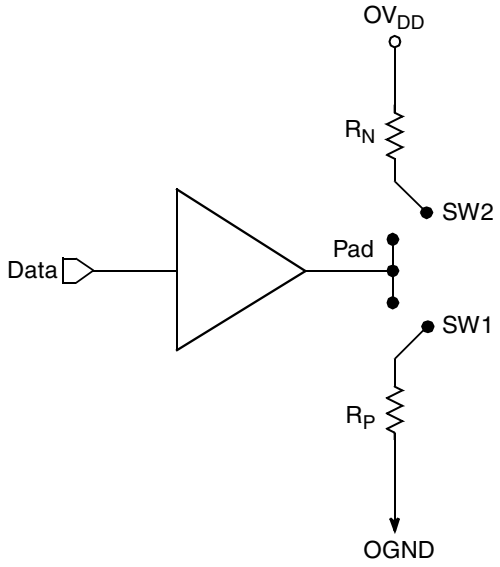


Figure 45. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

27 Document revision history

The following table provides a revision history for this document.

Table 66. Document revision history

Rev. No.	Date	Substantive Change(s)
2	09/2012	• In Table 53, swapped CLK13 and CLK14. • In Table 53, removed the following test signals, as there are no corresponding use cases: – ECID_TMODE_IN – BOOT_ROM_ADDR[2] to BOOT_ROM_ADDR[12] – BOOT_ROM_RDATA[0] to BOOT_ROM_RDATA[31] – BOOT_ROM_MOD_EN, BOOT_ROM_RWB, BOOT_ROM_XFR_WAIT, BOOT_ROM_XFR_ERR – UC1_RM, UC2_RM, UC3_RM, UC5_RM, UC7_RM, AND URM_TRIG – TPR_SYS_AAD[0] to TPR_SYS_AAD[15] – TPR_SYS_SYNC, TPR_SYS_DACK – QE_TRB_0, QE_TRB_1 – PLLCZ_CORE_CLKIN – JTAG_BISE, JTAG_PRPGPS, JTAG_BISR_TDO_EN – CLOCK_XLB_CLOCK_OUT – PD_XLB2MG_DDR_CLOCK • In Table 53, changed the following signal names as only QE-Based Fast Ethernet Controller is present in this device: – TSEC_TMR_TRIG1 to FEC_TMR_TRIG1 – TSEC_TMR_TRIG2 to FEC_TMR_TRIG2 – TSEC_TMR_CLK to FEC_TMR_CLK – TSEC_TMR_GCLK to FEC_TMR_GCLK – TSEC_TMR_PP1 to FEC_TMR_PP1 – TSEC_TMR_PP2 to FEC_TMR_PP2 – TSEC_TMR_PP3 to FEC_TMR_PP3 – TSEC_TMR_ALARM1 to FEC_TMR_ALARM1 – TSEC_TMR_ALARM2 to FEC_TMR_ALARM2 – FEC3_TMR_TX_ESFD to FEC2_TMR_TX_ESFD – FEC3_TMR_RX_ESFD to FEC2_TMR_RX_ESFD. • In Table 18, added parameteres $t_{LALEHOV}$,, $t_{LALETOT}$, and t_{LBOTOT} and made the corresponding updates in Figure 8 • In Figure 3, replaced "32 X tSYS_CLK_IN" with "32 X tSYS_CLK_IN/PCI_SYNC_IN.
1	08/2011	• Updated QUICC Engine frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 61. • Updated CEPMF and CEDF as per new QE frequency in Table 61. • Updated QUICC Engine frequency to 233 MHz in Table 64. • Corrected LCCR to LCRR for all instances.
0	03/2011	Initial Release.

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