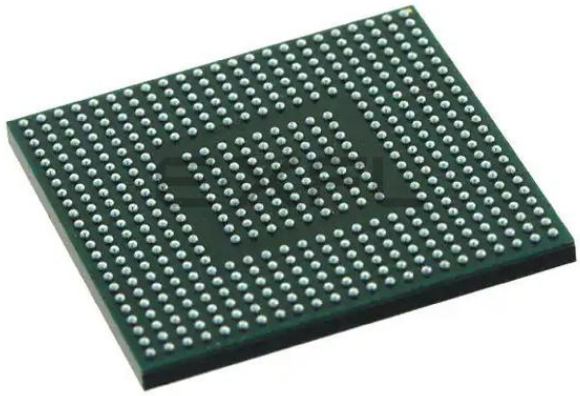

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309vmaddca

1.1 Features

The major features of the device are as follows:

- e300c3 Power Architecture processor core
  - Enhanced version of the MPC603e core
  - High-performance, superscalar processor core with a four-stage pipeline and low interrupt latency times
  - Floating-point, dual integer units, load/store, system register, and branch processing units
  - 16-KB instruction cache and 16-KB data cache with lockable capabilities
  - Dynamic power management
  - Enhanced hardware program debug features
  - Software-compatible with Freescale processor families implementing Power Architecture technology
  - Separate PLL that is clocked by the system bus clock
  - Performance monitor
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals with the following features:
    - One clock per instruction
    - Separate PLL for operating frequency that is independent of system's bus and e300 core frequency for power and performance optimization
    - 32-bit instruction object code
    - Executes code from internal IRAM
    - 32-bit arithmetic logic unit (ALU) data path
    - Modular architecture allowing for easy functional enhancements
    - Slave bus for CPU access of registers and multiuser RAM space
    - 48 KB of instruction RAM
    - 16 KB of multiuser data RAM
    - Serial DMA channel for receive and transmit on all serial channels
  - Five unified communication controllers (UCCs) supporting the following protocols and interfaces:
    - 10/100 Mbps Ethernet/IEEE Std. 802.3® through MII and RMII interfaces.
    - IEEE Std. 1588™ support
    - HDLC/Transparent (bit rate up to QUICC Engine operating frequency / 8)
    - HDLC Bus (bit rate up to 10 Mbps)
    - Asynchronous HDLC (bit rate up to 2 Mbps)
    - Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

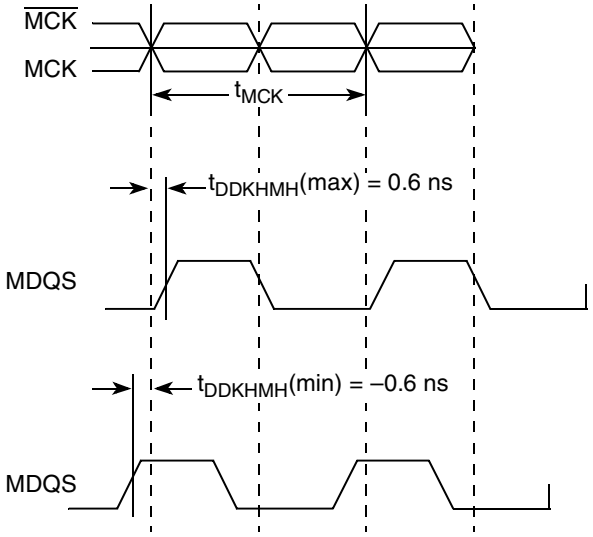


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

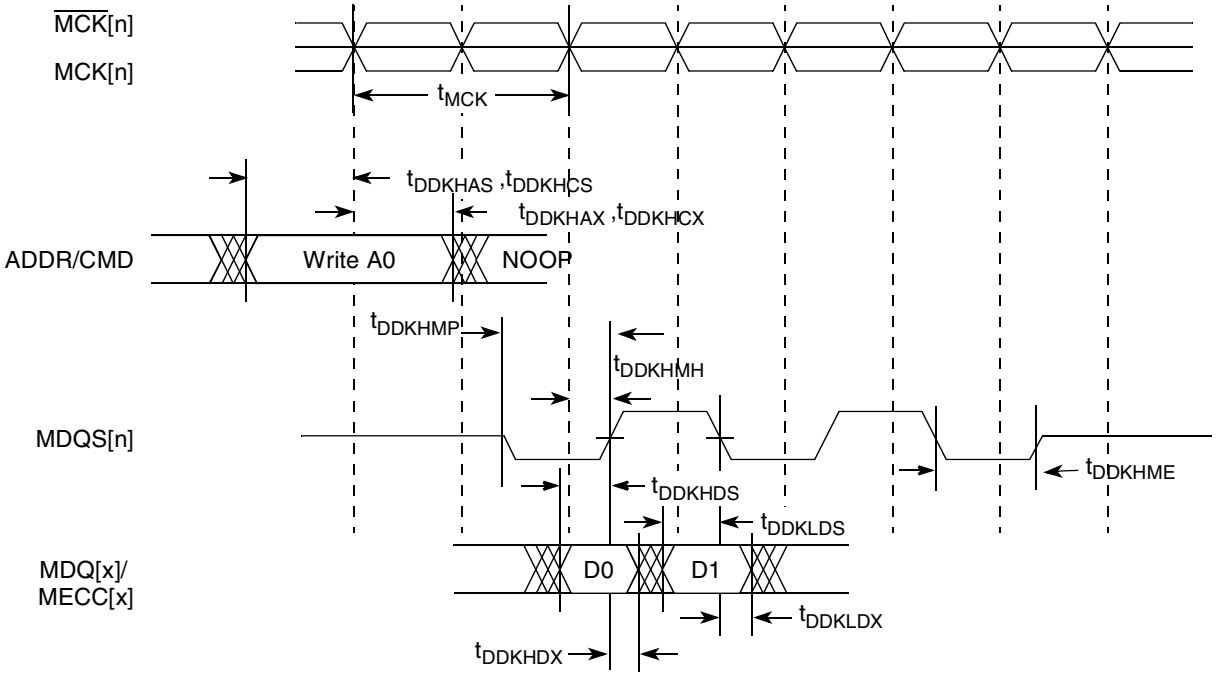


Figure 6. DDR2 SDRAM output timing diagram

The following figure provides the AC test load for the local bus.

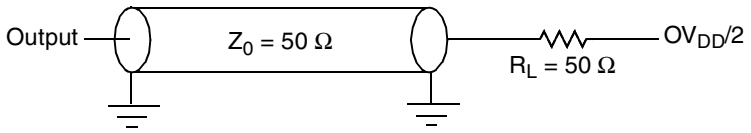


Figure 7. Enhanced local bus ac test load

The following figures show the local bus signals. These figures have been given indicate timing parameters only and do not reflect actual functional operation of interface.

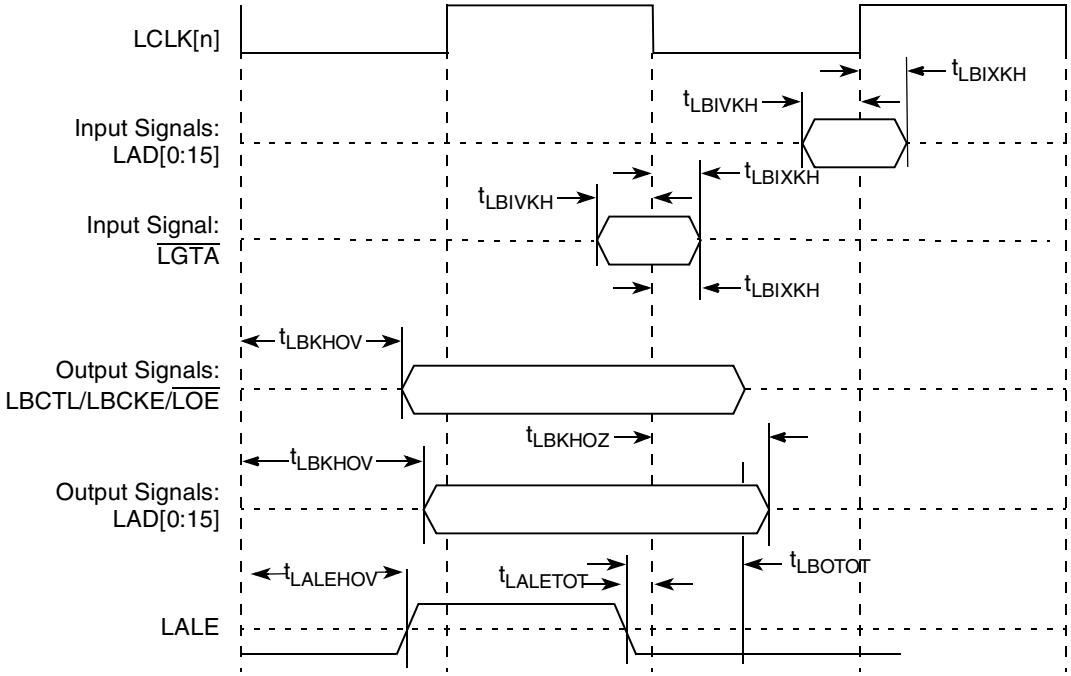


Figure 8. Enhanced local bus signals

The following figure shows the MII receive AC timing diagram.

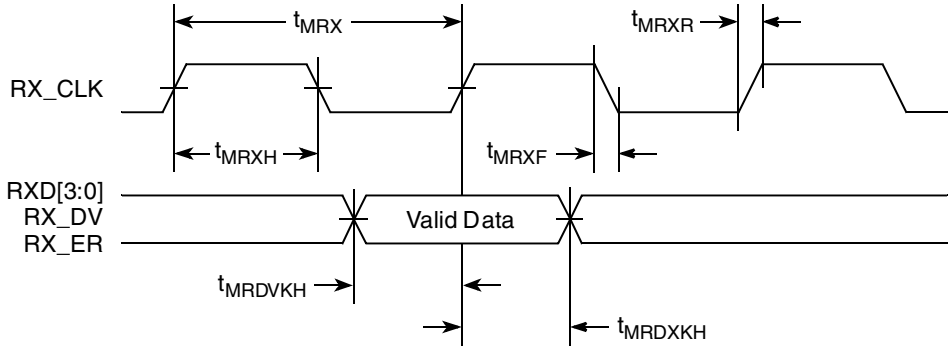


Figure 13. MII receive AC timing diagram

8.2.2 RMII AC timing specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII transmit AC timing specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13 ns	
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min) t	RMXF	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

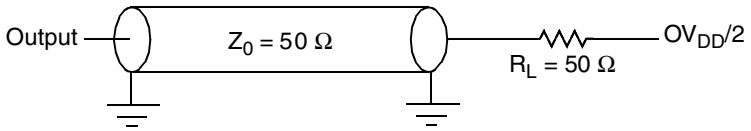


Figure 14. AC test load

The following figure shows the RMII receive AC timing diagram.

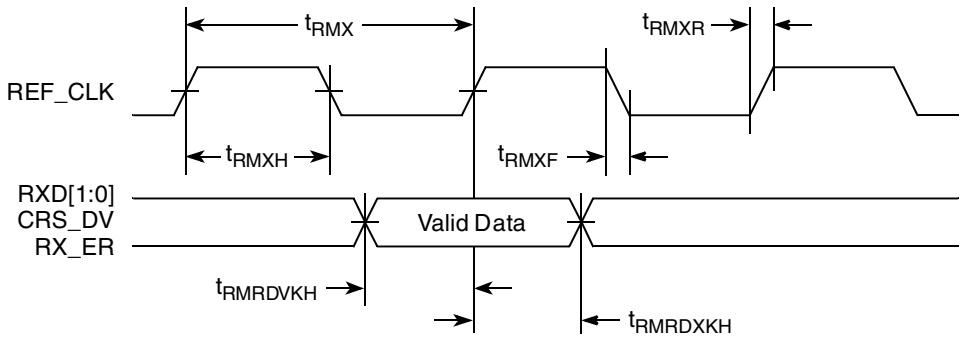


Figure 16. RMII receive AC timing diagram

8.3 Ethernet management interface electrical characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics."

8.3.1 MII management DC electrical characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII management DC electrical characteristics when powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII management AC electrical specifications

The following table provides the MII management AC timing specifications.

Table 25. MII management AC timing specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8309.

9.1 TDM/SI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 TDM/SI.

Table 26. TDM/SI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

9.2 TDM/SI AC timing specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 27. TDM/SI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

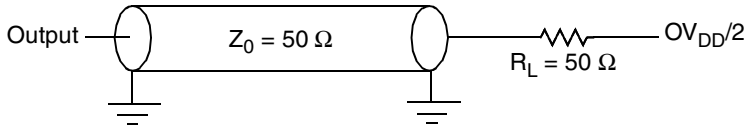


Figure 18. TDM/SI AC test load

Table 29. HDLC AC timing specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	9	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

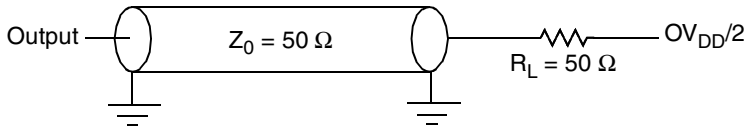
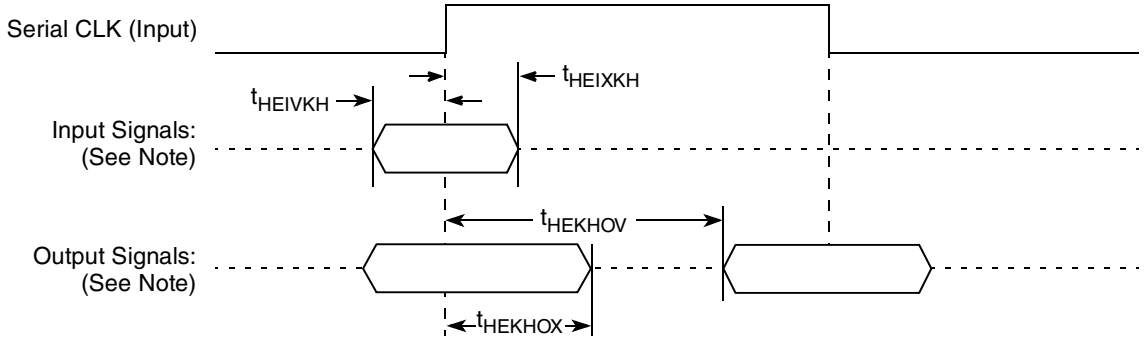


Figure 20. AC test load

Figure 21 and Figure 22 represent the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 21. AC timing (external clock) diagram

Table 34. USB general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

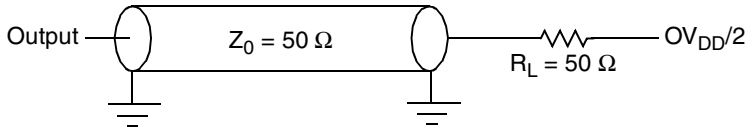


Figure 26. USB AC test load

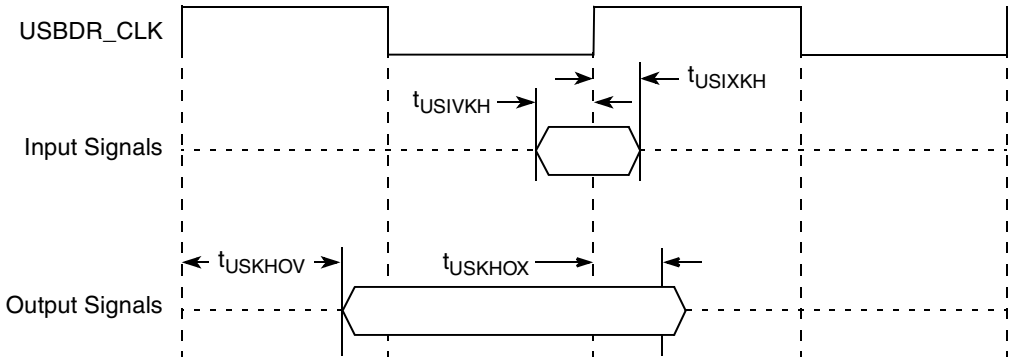


Figure 27. USB signals

14 eSDHC

This section describes the DC and AC electrical specifications for the eSDHC interface of the device.

14.1 eSDHC DC electrical characteristics

The following table provides the DC electrical characteristics for the eSDHC interface.

Table 37. eSDHC Interface DC electrical characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times OV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times OV_{DD}$	V	1
Output high voltage	V_{OH}	I_{OH} = –100 µA at OV_{DD} min	$0.75 \times OV_{DD}$	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 µA at OV_{DD} min	—	$0.125 \times OV_{DD}$	V	—
Output high voltage	V_{OH}	I_{OH} = –100 mA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	µA	—

Notes:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2..
2. Open drain mode for MMC cards only.

14.2 eSDHC AC timing specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 28 and Figure 29.

Table 38. eSDHC AC timing specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	25/33.25 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	4

16 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8309.

16.1 I²C DC electrical characteristics

The following table provides the DC electrical characteristics for the I²C interface of the MPC8309.

Table 41. I²C DC electrical characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

16.2 I²C AC electrical specifications

The following table provides the AC timing parameters for the I²C interface of the MPC8309.

Table 42. I²C AC electrical specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 41).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	300	0.9[3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$[4]	300	ns

Table 42. I²C AC electrical specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 41).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8309 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

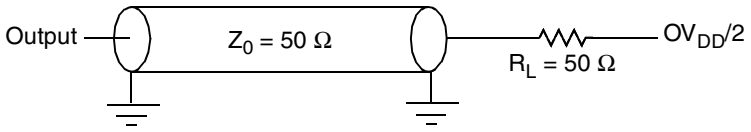


Figure 30. I²C AC test load

The following figure shows the AC timing diagram for the I²C bus.

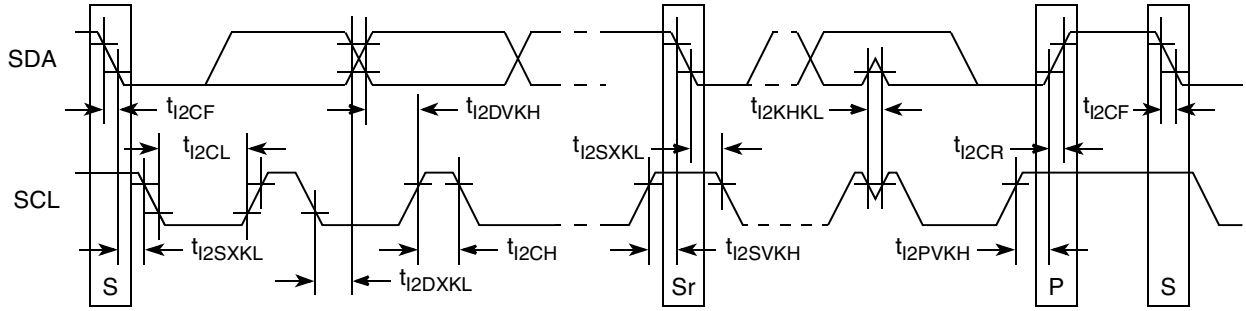


Figure 31. I²C bus AC timing diagram

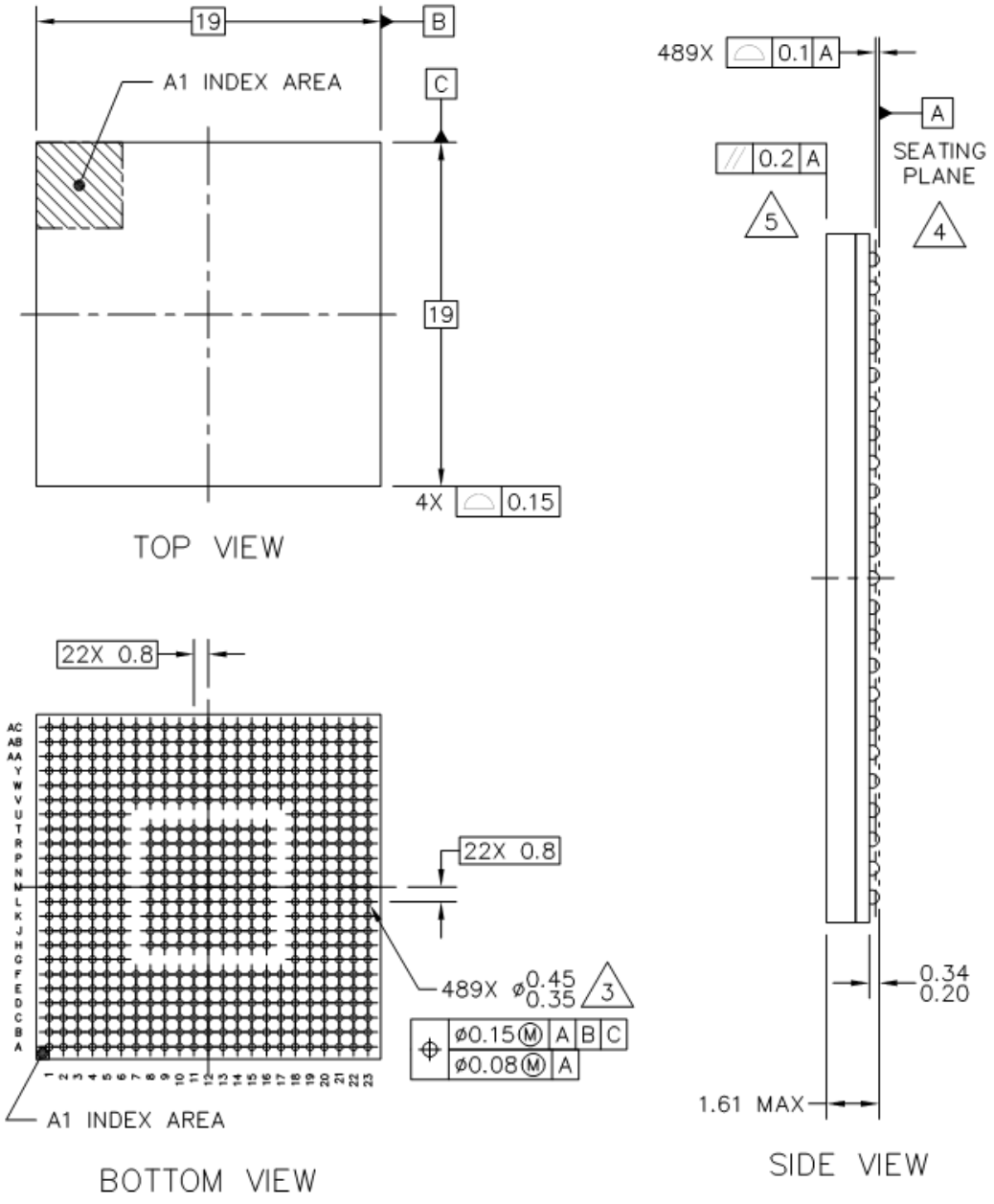


Figure 42. Mechanical dimensions and bottom surface nomenclature of the MPC8309 MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

22.3 Pinout listings

Following table shows the pin list of the MPC8309.

Table 53. MPC8309 pinout listing

Signal	Terminal	Pad Dir	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	U5	IO	GV_{DD}	—
MEMC_MDQ1	AA1	IO	GV_{DD}	—
MEMC_MDQ2	W3	IO	GV_{DD}	—
MEMC_MDQ3	R5	IO	GV_{DD}	—
MEMC_MDQ4	W2	IO	GV_{DD}	—
MEMC_MDQ5	U3	IO	GV_{DD}	—
MEMC_MDQ6	U2	IO	GV_{DD}	—
MEMC_MDQ7	T3	IO	GV_{DD}	—
MEMC_MDQ8	H3	IO	GV_{DD}	—
MEMC_MDQ9	H4	IO	GV_{DD}	—
MEMC_MDQ10	G3	IO	GV_{DD}	—
MEMC_MDQ11	F3	IO	GV_{DD}	—
MEMC_MDQ12	G5	IO	GV_{DD}	—
MEMC_MDQ13	F4	IO	GV_{DD}	—
MEMC_MDQ14	F5	IO	GV_{DD}	—
MEMC_MDQ15	E3	IO	GV_{DD}	—
MEMC_MDQ16	V4	IO	GV_{DD}	—
MEMC_MDQ17	Y2	IO	GV_{DD}	—
MEMC_MDQ18	Y1	IO	GV_{DD}	—
MEMC_MDQ19	U4	IO	GV_{DD}	—
MEMC_MDQ20	V1	IO	GV_{DD}	—
MEMC_MDQ21	R4	IO	GV_{DD}	—
MEMC_MDQ22	U1	IO	GV_{DD}	—
MEMC_MDQ23	T2	IO	GV_{DD}	—
MEMC_MDQ24	J5	IO	GV_{DD}	—
MEMC_MDQ25	G2	IO	GV_{DD}	—
MEMC_MDQ26	G1	IO	GV_{DD}	—
MEMC_MDQ27	F1	IO	GV_{DD}	—
MEMC_MDQ28	E2	IO	GV_{DD}	—

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1 A20		IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

23.1 Clocking in PCI host mode

When the MPC8309 is configured as a PCI host device (RCWH[PCIHOST] = 1), SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK multiplexors. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

23.1.1 PCI clock outputs (PCI_CLK[0:2])

When the MPC8309 is configured as a PCI host, it provides three separate clock output signals, PCI_CLK[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

23.2 Clocking in PCI agent mode

When the MPC8309 is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock. In agent mode, the SYS_CLK_IN signal should be tied to GND, and the clock output signals, PCI_CLK*n* and PCI_SYNC_OUT, are not used.

23.3 System clock domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF} \qquad \textit{Eqn. 1}$$

In PCI host mode,

$$PCI\_SYNC\_IN = SYS\_CLK\_IN \div (1 + \sim\overline{CFG\_CLKIN\_DIV}) . \qquad \textbf{Eqn. 2}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset

24 Thermal

This section describes the thermal specifications of the MPC8309.

24.1 Thermal characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8309.

Table 62. Package thermal characteristics for MAPBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	40	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	25	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	33	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	15	°C/W	4
Junction-to-case —		$R_{\theta JC}$	9	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.1.1 Thermal management information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.1.2 Estimation of junction temperature with junction-to-ambient thermal resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where,

T_J = junction temperature (°C)

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

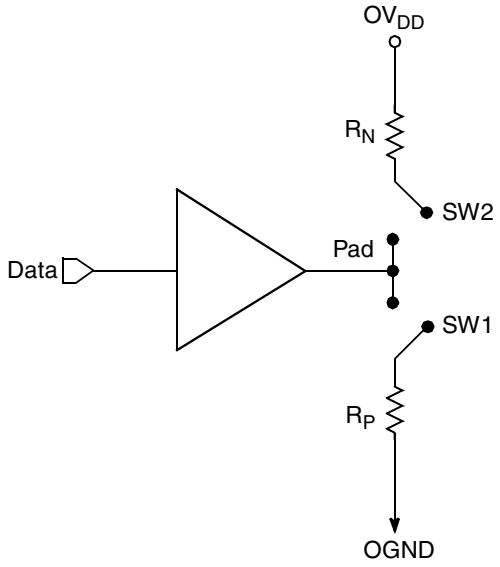


Figure 45. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 63. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	?
R_P	42 Target	20 Target	Z_0	?
Differential	NA	NA	Z_{DIFF}	?

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

27 Document revision history

The following table provides a revision history for this document.

Table 66. Document revision history

Rev. No.	Date	Substantive Change(s)
2	09/2012	• In Table 53, swapped CLK13 and CLK14. • In Table 53, removed the following test signals, as there are no corresponding use cases: – ECID_TMODE_IN – BOOT_ROM_ADDR[2] to BOOT_ROM_ADDR[12] – BOOT_ROM_RDATA[0] to BOOT_ROM_RDATA[31] – BOOT_ROM_MOD_EN, BOOT_ROM_RWB, BOOT_ROM_XFR_WAIT, BOOT_ROM_XFR_ERR – UC1_RM, UC2_RM, UC3_RM, UC5_RM, UC7_RM, AND URM_TRIG – TPR_SYS_AAD[0] to TPR_SYS_AAD[15] – TPR_SYS_SYNC, TPR_SYS_DACK – QE_TRB_0, QE_TRB_1 – PLLCZ_CORE_CLKIN – JTAG_BISE, JTAG_PRPGPS, JTAG_BISR_TDO_EN – CLOCK_XLB_CLOCK_OUT – PD_XLB2MG_DDR_CLOCK • In Table 53, changed the following signal names as only QE-Based Fast Ethernet Controller is present in this device: – TSEC_TMR_TRIG1 to FEC_TMR_TRIG1 – TSEC_TMR_TRIG2 to FEC_TMR_TRIG2 – TSEC_TMR_CLK to FEC_TMR_CLK – TSEC_TMR_GCLK to FEC_TMR_GCLK – TSEC_TMR_PP1 to FEC_TMR_PP1 – TSEC_TMR_PP2 to FEC_TMR_PP2 – TSEC_TMR_PP3 to FEC_TMR_PP3 – TSEC_TMR_ALARM1 to FEC_TMR_ALARM1 – TSEC_TMR_ALARM2 to FEC_TMR_ALARM2 – FEC3_TMR_TX_ESFD to FEC2_TMR_TX_ESFD – FEC3_TMR_RX_ESFD to FEC2_TMR_RX_ESFD. • In Table 18, added parameteres $t_{LALEHOV}$,, $t_{LALETOT}$, and t_{LBOTOT} and made the corresponding updates in Figure 8 • In Figure 3, replaced "32 X tSYS_CLK_IN" with "32 X tSYS_CLK_IN/PCI_SYNC_IN.
1	08/2011	• Updated QUICC Engine frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 61. • Updated CEPMF and CEDF as per new QE frequency in Table 61. • Updated QUICC Engine frequency to 233 MHz in Table 64. • Corrected LCCR to LCRR for all instances.
0	03/2011	Initial Release.

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