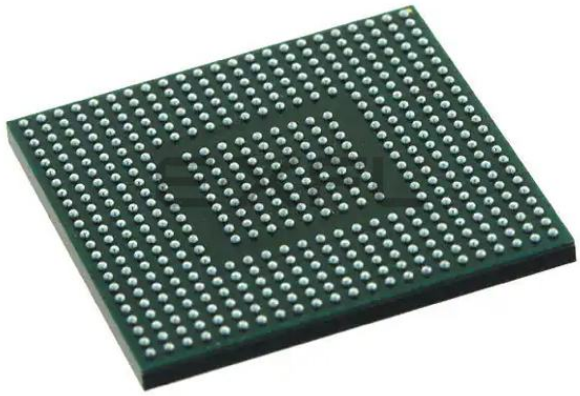

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8309vmafdca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

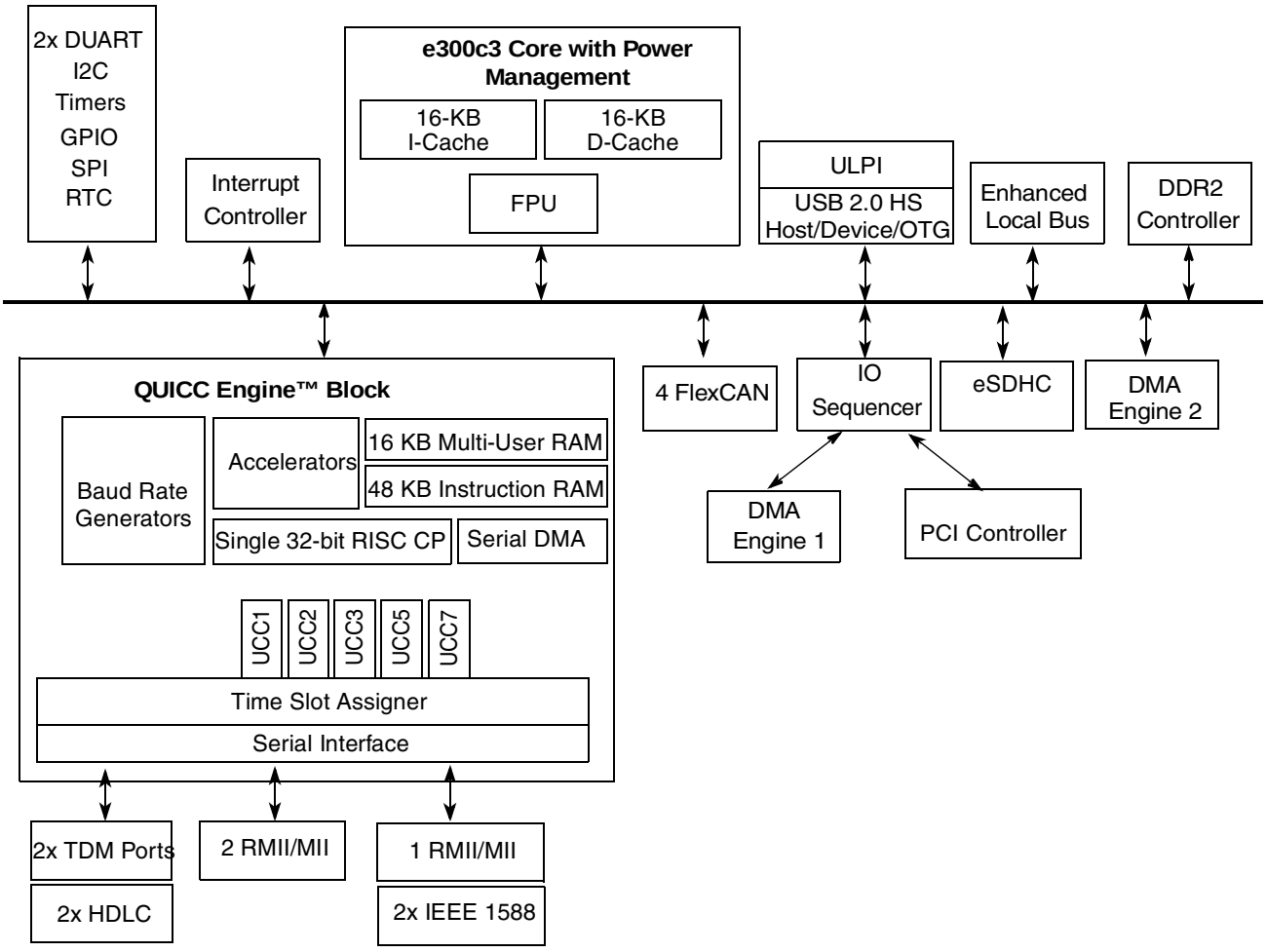


Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine1
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- IO Sequencer

2.1 Overall DC electrical characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute maximum ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

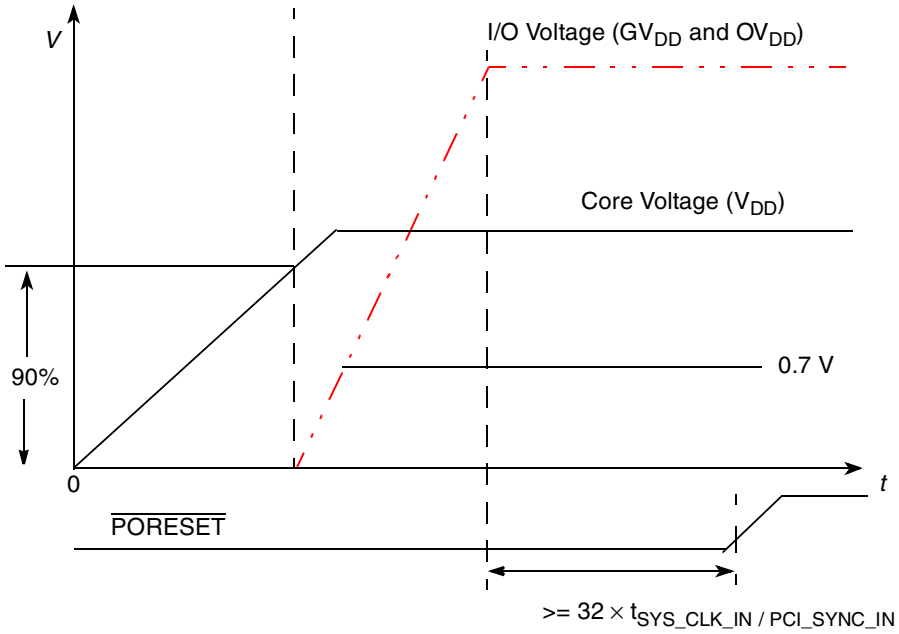


Figure 3. MPC8309 Power-Up sequencing example

3 Power characteristics

The typical power dissipation for this family of MPC8309 devices is shown in the following table.

Table 5. MPC8309 Power dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
266	233	133	0.341	0.920	W	1, 2, 3
333	233	133	0.361	0.938	W	1, 2, 3
400	233	133	0.381	0.969	W	1,2,3
417	233	167	0.429	1.003	W	1,2,3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, WC process, a junction T_J = 105°C, and a smoke test code.

4.2 AC electrical characteristics

The primary clock source for the MPC8309 can be one of two inputs, SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or agent mode. The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) AC timing specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC timing specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24 —		66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
PCI_SYNC_IN rise and fall time	t_{PCH}, t_{PCL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8309. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET initialization timing specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN or PCI_SYNC_IN (in agent mode)	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

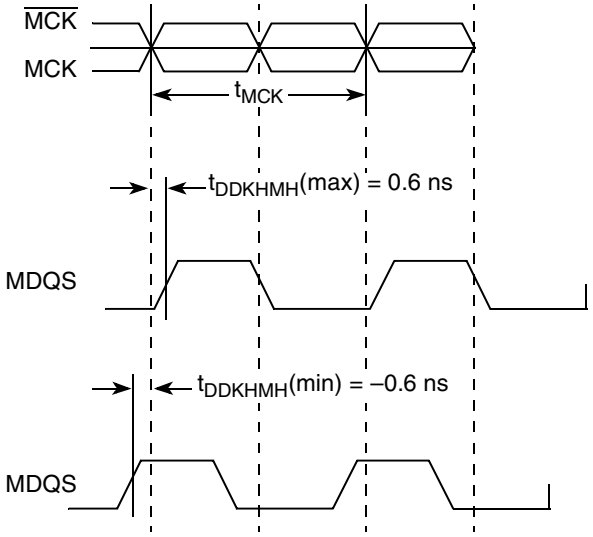


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

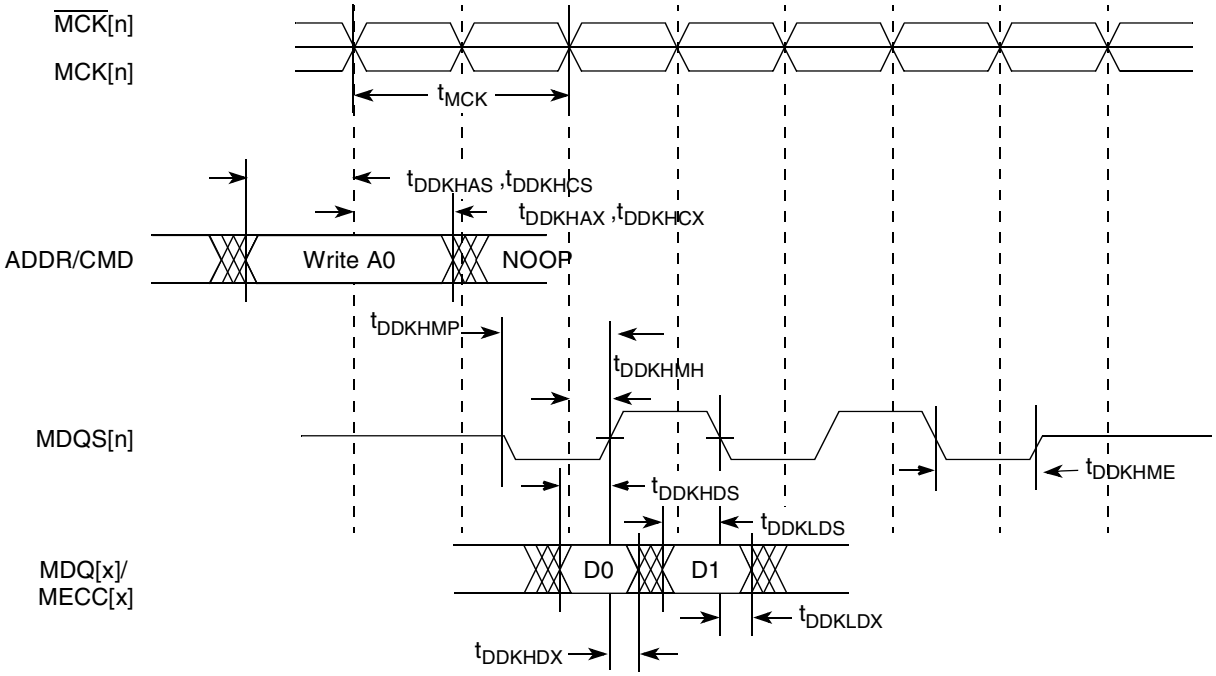


Figure 6. DDR2 SDRAM output timing diagram

The following figure provides the AC test load for the local bus.

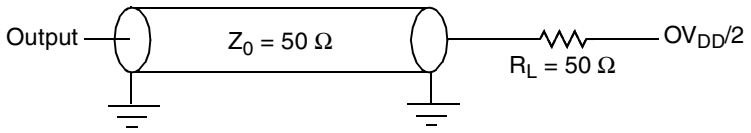


Figure 7. Enhanced local bus ac test load

The following figures show the local bus signals. These figures have been given indicate timing parameters only and do not reflect actual functional operation of interface.

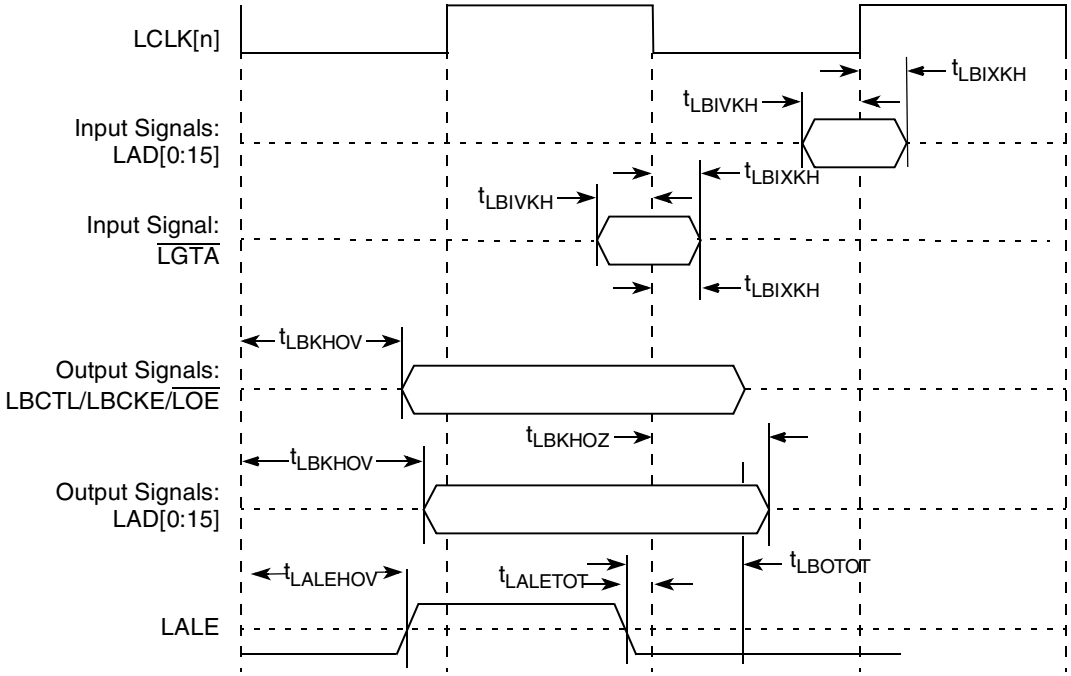


Figure 8. Enhanced local bus signals

Table 19. MII and RMII DC electrical characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC timing specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII transmit AC timing specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min) t	MTXF	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 29. HDLC AC timing specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	9	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

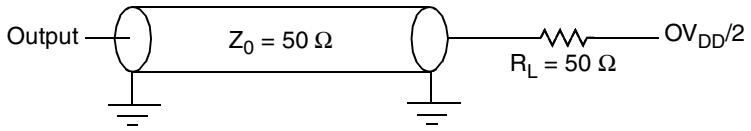
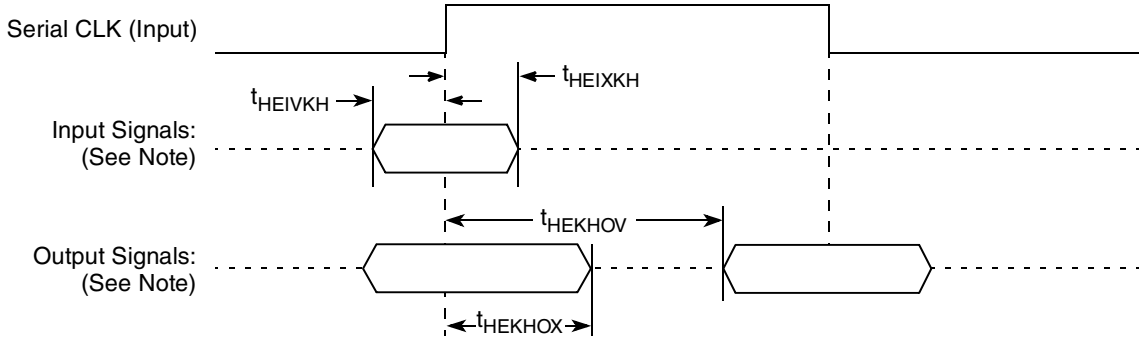


Figure 20. AC test load

Figure 21 and Figure 22 represent the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 21. AC timing (external clock) diagram

14 eSDHC

This section describes the DC and AC electrical specifications for the eSDHC interface of the device.

14.1 eSDHC DC electrical characteristics

The following table provides the DC electrical characteristics for the eSDHC interface.

Table 37. eSDHC Interface DC electrical characteristics

At recommended operating conditions with OV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times OV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times OV_{DD}$	V	1
Output high voltage	V_{OH}	I_{OH} = –100 µA at OV_{DD} min	$0.75 \times OV_{DD}$	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100 µA at OV_{DD} min	—	$0.125 \times OV_{DD}$	V	—
Output high voltage	V_{OH}	I_{OH} = –100 mA	OV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	µA	—

Notes:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2..
2. Open drain mode for MMC cards only.

14.2 eSDHC AC timing specifications

The following table provides the eSDHC AC timing specifications as defined in Figure 28 and Figure 29.

Table 38. eSDHC AC timing specifications

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SHSCK}	0	25/33.25 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	4

Table 49. SPI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

20.2 SPI AC timing specifications

The following table and provide the SPI input and output AC timing specifications.

Table 50. SPI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
3. All units of output delay must be enabled for 8309_output_port spimosi_lpgl0(SPI Master mode)
4. Delay units must not be enabled for Slave mode.

The following figure provides the AC test load for the SPI.

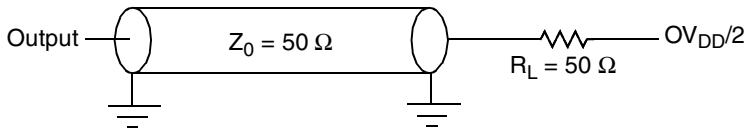


Figure 34. SPI AC test load

Figure 35 and Figure 36 represent the AC timing from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 51. JTAG interface DC electrical characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

21.2 JTAG AC electrical characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309. The following table provides the JTAG AC timing specifications as defined in Figure 38 through Figure 41.

Table 52. JTAG AC timing specifications (independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5

Table 52. JTAG AC timing specifications (independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	2	—		5
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 37). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8309.

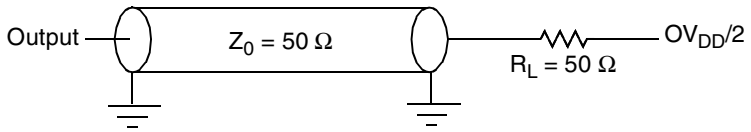


Figure 37. AC test load for the JTAG interface

The following figure provides the JTAG clock input timing diagram.

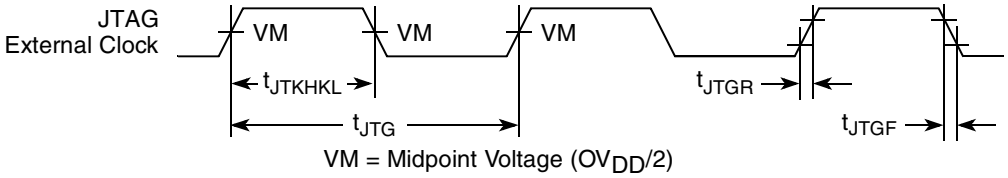


Figure 38. JTAG clock input timing diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

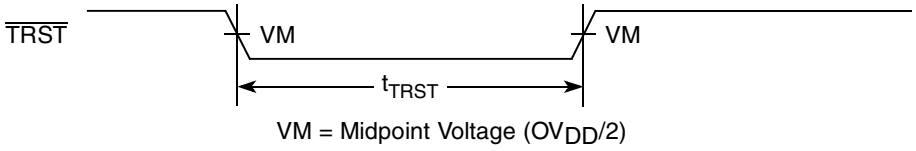


Figure 39. $\overline{\text{TRST}}$ timing diagram

22.3 Pinout listings

Following table shows the pin list of the MPC8309.

Table 53. MPC8309 pinout listing

Signal	Terminal	Pad Dir	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	U5	IO	GV_{DD}	—
MEMC_MDQ1	AA1	IO	GV_{DD}	—
MEMC_MDQ2	W3	IO	GV_{DD}	—
MEMC_MDQ3	R5	IO	GV_{DD}	—
MEMC_MDQ4	W2	IO	GV_{DD}	—
MEMC_MDQ5	U3	IO	GV_{DD}	—
MEMC_MDQ6	U2	IO	GV_{DD}	—
MEMC_MDQ7	T3	IO	GV_{DD}	—
MEMC_MDQ8	H3	IO	GV_{DD}	—
MEMC_MDQ9	H4	IO	GV_{DD}	—
MEMC_MDQ10	G3	IO	GV_{DD}	—
MEMC_MDQ11	F3	IO	GV_{DD}	—
MEMC_MDQ12	G5	IO	GV_{DD}	—
MEMC_MDQ13	F4	IO	GV_{DD}	—
MEMC_MDQ14	F5	IO	GV_{DD}	—
MEMC_MDQ15	E3	IO	GV_{DD}	—
MEMC_MDQ16	V4	IO	GV_{DD}	—
MEMC_MDQ17	Y2	IO	GV_{DD}	—
MEMC_MDQ18	Y1	IO	GV_{DD}	—
MEMC_MDQ19	U4	IO	GV_{DD}	—
MEMC_MDQ20	V1	IO	GV_{DD}	—
MEMC_MDQ21	R4	IO	GV_{DD}	—
MEMC_MDQ22	U1	IO	GV_{DD}	—
MEMC_MDQ23	T2	IO	GV_{DD}	—
MEMC_MDQ24	J5	IO	GV_{DD}	—
MEMC_MDQ25	G2	IO	GV_{DD}	—
MEMC_MDQ26	G1	IO	GV_{DD}	—
MEMC_MDQ27	F1	IO	GV_{DD}	—
MEMC_MDQ28	E2	IO	GV_{DD}	—

Table 57. CSB frequency options

SPMF	csb_clk : sys_clk_in Ratio	PCI_SYNC_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

23.5 Core PLL configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 58. e300 Core PLL configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.1.5 Heat sinks and junction-to-case thermal resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance as shown in the following equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

24.2 Heat sink attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

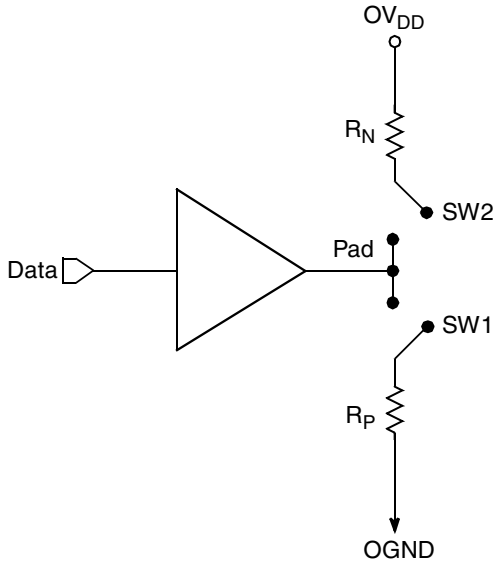


Figure 45. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 63. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	?
R_P	42 Target	20 Target	Z_0	?
Differential	NA	NA	Z_{DIFF}	?

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

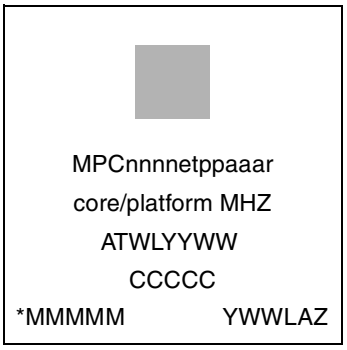
Table 64. Part numbering nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8309	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AD = 266 MHz AF = 333 MHz AG = 400 MHz AH = 417MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 22, "Package and pin listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

26.2 Part marking

Parts are marked as in the example shown in the following figure.



MAPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 46. Freescale part marking for MAPBGA devices

The following table shows the SVR Settings.

Table 65. SVR settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8309	MAPBGA	0x8110_0010	0x8110_0011
Note: PVR = 0x8085_0020			

27 Document revision history

The following table provides a revision history for this document.

Table 66. Document revision history

Rev. No.	Date	Substantive Change(s)
2	09/2012	• In Table 53, swapped CLK13 and CLK14. • In Table 53, removed the following test signals, as there are no corresponding use cases: – ECID_TMODE_IN – BOOT_ROM_ADDR[2] to BOOT_ROM_ADDR[12] – BOOT_ROM_RDATA[0] to BOOT_ROM_RDATA[31] – BOOT_ROM_MOD_EN, BOOT_ROM_RWB, BOOT_ROM_XFR_WAIT, BOOT_ROM_XFR_ERR – UC1_RM, UC2_RM, UC3_RM, UC5_RM, UC7_RM, AND URM_TRIG – TPR_SYS_AAD[0] to TPR_SYS_AAD[15] – TPR_SYS_SYNC, TPR_SYS_DACK – QE_TRB_0, QE_TRB_1 – PLLCZ_CORE_CLKIN – JTAG_BISE, JTAG_PRPGPS, JTAG_BISR_TDO_EN – CLOCK_XLB_CLOCK_OUT – PD_XLB2MG_DDR_CLOCK • In Table 53, changed the following signal names as only QE-Based Fast Ethernet Controller is present in this device: – TSEC_TMR_TRIG1 to FEC_TMR_TRIG1 – TSEC_TMR_TRIG2 to FEC_TMR_TRIG2 – TSEC_TMR_CLK to FEC_TMR_CLK – TSEC_TMR_GCLK to FEC_TMR_GCLK – TSEC_TMR_PP1 to FEC_TMR_PP1 – TSEC_TMR_PP2 to FEC_TMR_PP2 – TSEC_TMR_PP3 to FEC_TMR_PP3 – TSEC_TMR_ALARM1 to FEC_TMR_ALARM1 – TSEC_TMR_ALARM2 to FEC_TMR_ALARM2 – FEC3_TMR_TX_ESFD to FEC2_TMR_TX_ESFD – FEC3_TMR_RX_ESFD to FEC2_TMR_RX_ESFD. • In Table 18, added parameteres $t_{LALEHOV}$,, $t_{LALETOT}$, and t_{LBOTOT} and made the corresponding updates in Figure 8 • In Figure 3, replaced "32 X tSYS_CLK_IN" with "32 X tSYS_CLK_IN/PCI_SYNC_IN.
1	08/2011	• Updated QUICC Engine frequency in Table 5. • Updated QUICC Engine frequency from 200 MHz to 233 MHz in Table 61. • Updated CEPMF and CEDF as per new QE frequency in Table 61. • Updated QUICC Engine frequency to 233 MHz in Table 64. • Corrected LCCR to LCRR for all instances.
0	03/2011	Initial Release.