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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	417MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	489-LFBGA
Supplier Device Package	489-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8309vmahfca

  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine1
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- IO Sequencer

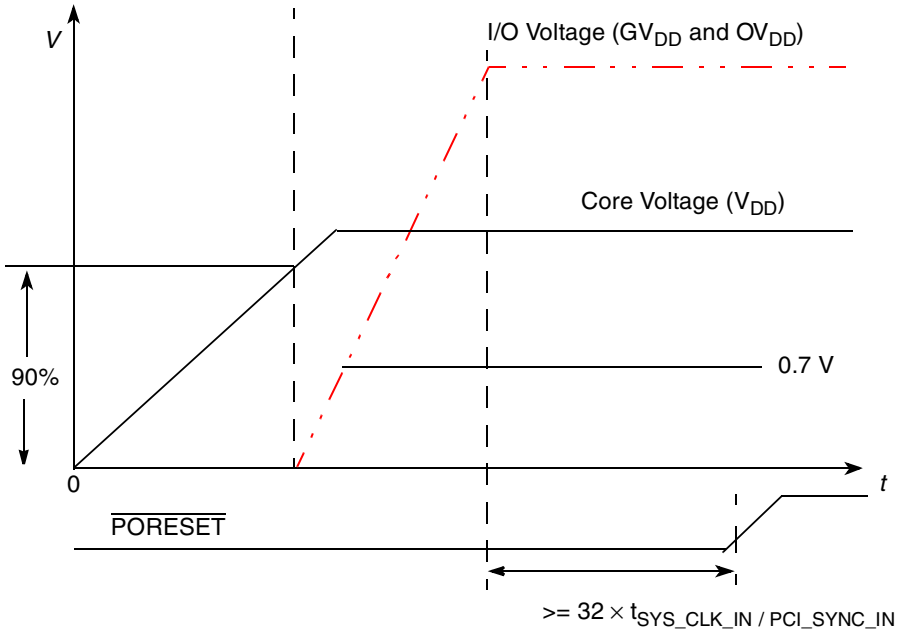


Figure 3. MPC8309 Power-Up sequencing example

3 Power characteristics

The typical power dissipation for this family of MPC8309 devices is shown in the following table.

Table 5. MPC8309 Power dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
266	233	133	0.341	0.920	W	1, 2, 3
333	233	133	0.361	0.938	W	1, 2, 3
400	233	133	0.381	0.969	W	1,2,3
417	233	167	0.429	1.003	W	1,2,3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, WC process, a junction T_J = 105°C, and a smoke test code.

4.2 AC electrical characteristics

The primary clock source for the MPC8309 can be one of two inputs, SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or agent mode. The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) AC timing specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC timing specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24 —		66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
PCI_SYNC_IN rise and fall time	t_{PCH}, t_{PCL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8309. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET initialization timing specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN or PCI_SYNC_IN (in agent mode)	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1

Table 12. DDR2 SDRAM DC electrical characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

Table 13. DDR2 SDRAM capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC electrical characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM input AC timing specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM input AC timing specifications for 1.8-V interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

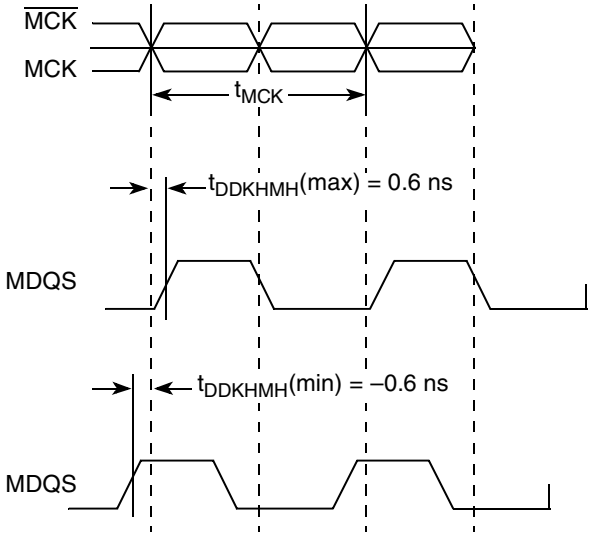


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

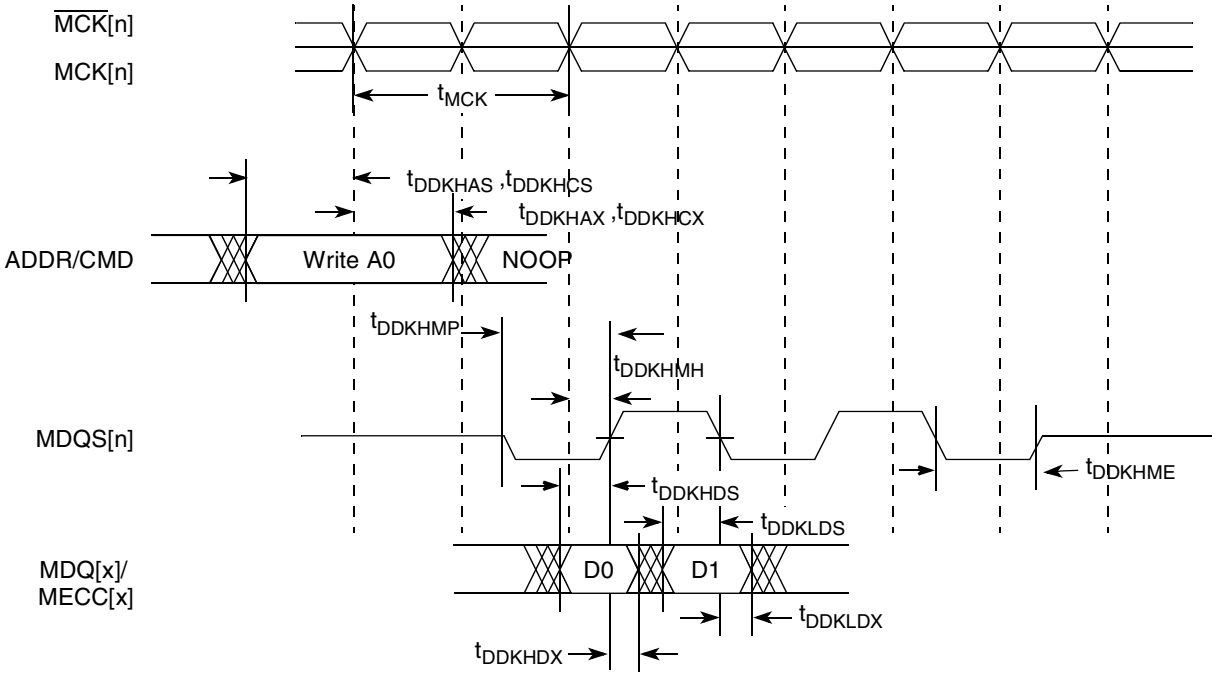


Figure 6. DDR2 SDRAM output timing diagram

7 Enhanced local bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface of the MPC8309.

7.1 Enhanced local bus DC electrical characteristics

The following table provides the DC electrical characteristics for the enhanced local bus interface.

Table 17. Enhanced local bus DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

7.2 Enhanced local bus AC electrical specifications

The following table describes the general timing parameters of the enhanced local bus interface of MPC8309.

Table 18. Enhanced local bus general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t_{LBOTOT}	3	—	ns	—
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3	ns	—
LALE output fall to LCLK negative edge	$t_{LALETOT}$	–5.0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 24 shows the PCI input AC timing conditions.

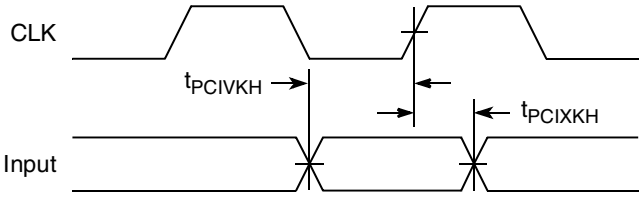


Figure 24. PCI input AC timing measurement conditions

Figure 25 shows the PCI output AC timing conditions.

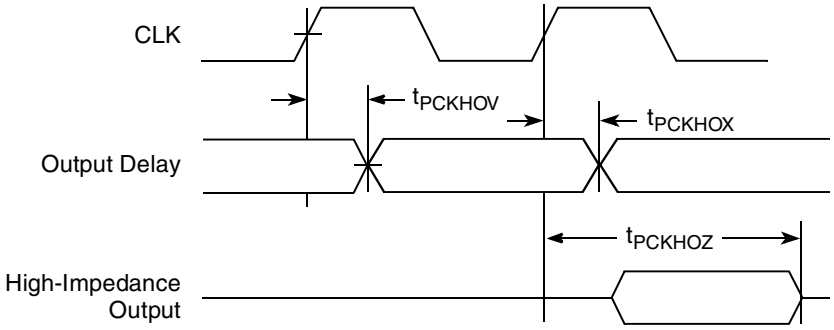


Figure 25. PCI output AC timing measurement condition

12 USB

12.1 USB controller

This section provides the AC and DC electrical specifications for the USB (ULPI) interface.

12.1.1 USB DC electrical characteristics

The following table provides the DC electrical characteristics for the USB interface.

Table 33. USB DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

12.1.2 USB AC electrical specifications

The following table describes the general timing parameters of the USB interface.

Table 34. USB general timing parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	—
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	—
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	—
USB clock to output valid—all outputs (except USBDR_STP_USBDR_STP)	t_{USKHOV}	—	7	ns	—
USB clock to output valid—USBDR_STP	t_{USKHOV}	—	7.5	ns	—
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	—

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following figures provide the AC test load and signals for the USB, respectively.

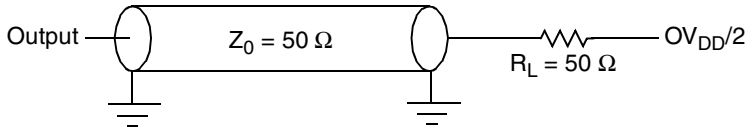


Figure 26. USB AC test load

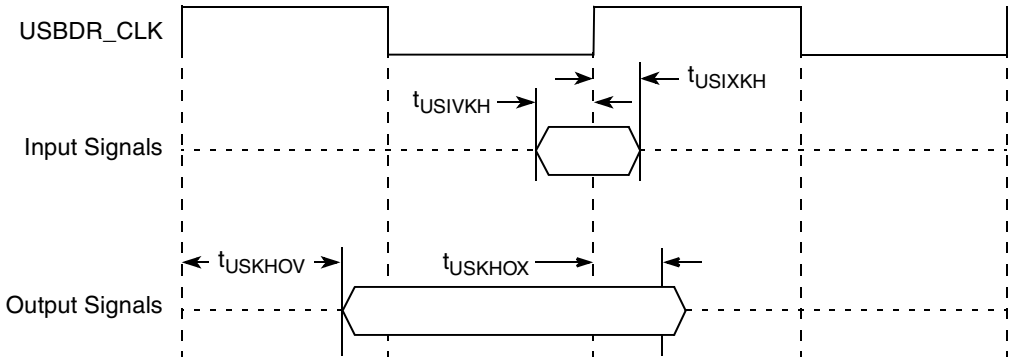


Figure 27. USB signals

13 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8309.

13.1 DUART DC electrical characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8309.

Table 35. DUART DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 DUART AC electrical specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8309.

Table 36. DUART AC timing specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Table 42. I²C AC electrical specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 41).

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_B[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8309 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

The following figure provides the AC test load for the I²C.

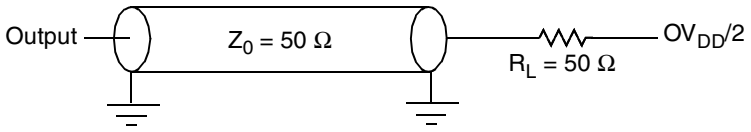


Figure 30. I²C AC test load

The following figure shows the AC timing diagram for the I²C bus.

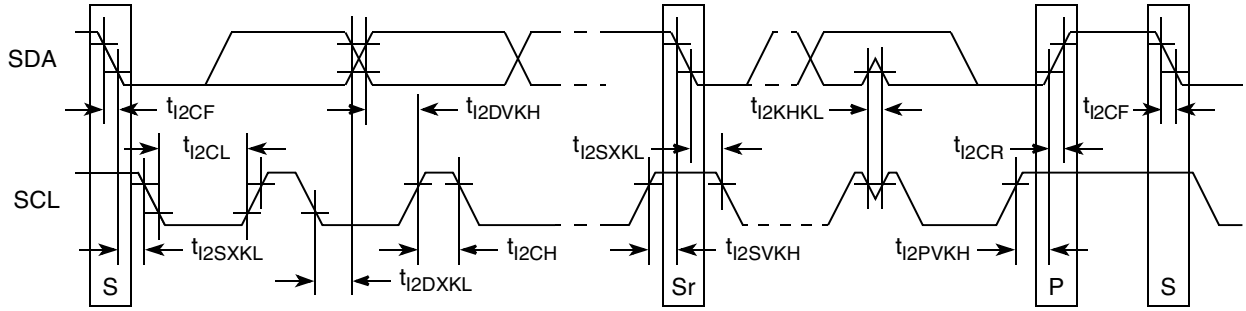


Figure 31. I²C bus AC timing diagram

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8309.

18.1 GPIO DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 GPIO.

Table 45. GPIO DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

18.2 GPIO AC timing specifications

The following table provides the GPIO input and output AC timing specifications.

Table 46. GPIO input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

The following figure provides the AC test load for the GPIO.

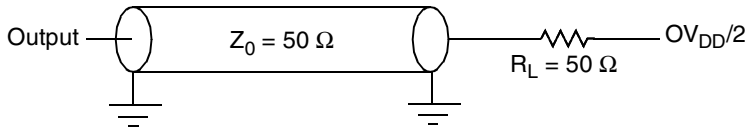
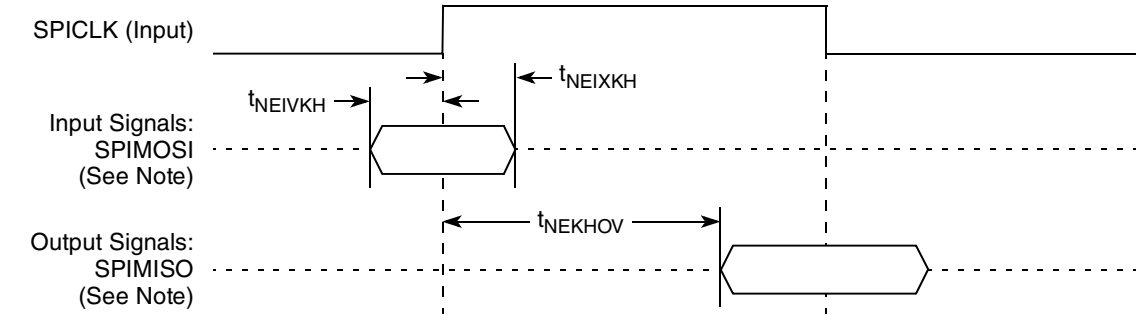


Figure 33. GPIO AC test load

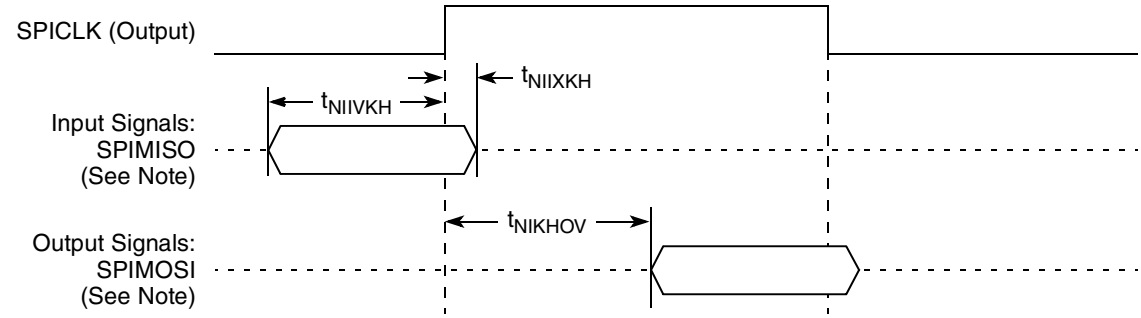
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in slave mode (external clock) diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC timing in master mode (internal clock) diagram

21 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8309.

21.1 JTAG DC electrical characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8309.

Table 51. JTAG interface DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 52. JTAG AC timing specifications (independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	2	—		5
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 37). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

The following figure provides the AC test load for TDO and the boundary-scan outputs of the MPC8309.

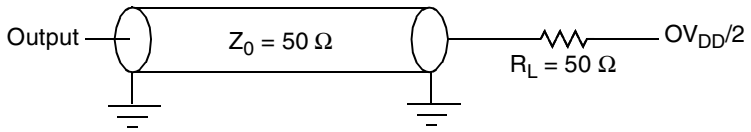


Figure 37. AC test load for the JTAG interface

The following figure provides the JTAG clock input timing diagram.

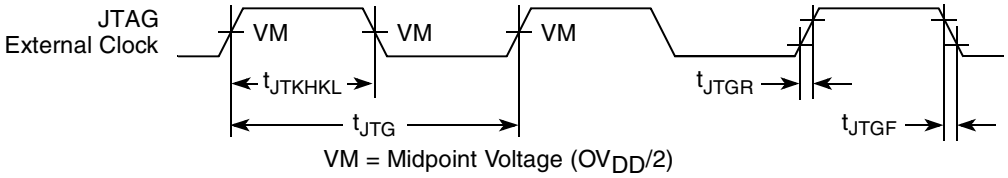


Figure 38. JTAG clock input timing diagram

The following figure provides the $\overline{\text{TRST}}$ timing diagram.

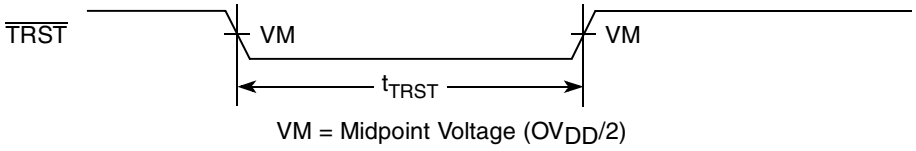


Figure 39. $\overline{\text{TRST}}$ timing diagram

22 Package and pin listings

This section details package parameters, pin assignments, and dimensions. The MPC8309 is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 22.1, “Package parameters for the MPC8309,” and Section 22.2, “Mechanical dimensions of the MPC8309 MAPBGA,” for information on the MAPBGA.

22.1 Package parameters for the MPC8309

The package parameters are as provided in the following list.

Package outline	19 mm × 19 mm
Package Type	MAPBGA
Interconnects	489
Pitch	0.80 mm
Module height (typical)	1.48 mm; Min = 1.31mm and Max 1.61mm
Solder Balls	96 Sn / 3.5 Ag / 0.5 Cu (VM package)
Ball diameter (typical)	0.40 mm

22.2 Mechanical dimensions of the MPC8309 MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8309, 489-MAPBGA package.

GPIO_9/TXCAN1/LSRCID1/LCS_B5	C17	IO	OV_{DD}	-
GPIO_10/RXCAN2/LSRCID2/LCS_B6	E15	IO	OV_{DD}	-
GPIO_11/TXCAN2/LSRCID3/LCS_B7	A18	IO	OV_{DD}	-
GPIO_12/RXCAN3/LSRCID4/LCLK1	D15	IO	OV_{DD}	-
GPIO_13/TXCAN3/LDVAL	C18	IO	OV_{DD}	-
GPIO_14/RXCAN4	D16	IO	OV_{DD}	-
GPIO_15/TXCAN4	C19	IO	OV_{DD}	-
USB				
USBDR_PWRFAULT/CE_PIO_1	AA6	I	OV_{DD}	1
USBDR_CLK/UART2_SIN2/UART2_CTS_B1	AC9	I	OV_{DD}	-
USBDR_DIR	AA7	I	OV_{DD}	-
USBDR_NXT/UART2_SIN1/QE_EXT_REQ_4	AC5	I	OV_{DD}	-
USBDR_TXDRXD0/GPIO_32	Y6	IO	OV_{DD}	-
USBDR_TXDRXD1/GPIO_33	W9	IO	OV_{DD}	-
USBDR_TXDRXD2/GPIO_34/QE_BRG_1	AB5	IO	OV_{DD}	-
USBDR_TXDRXD3/GPIO_35/QE_BRG_2	AA5	IO	OV_{DD}	-
USBDR_TXDRXD4/GPIO_36/QE_BRG_3	Y8	IO	OV_{DD}	-
USBDR_TXDRXD5/GPIO_37/QE_BRG_4	AC4	IO	OV_{DD}	-
USBDR_TXDRXD6/GPIO_38/QE_BRG_9	AC3	IO	OV_{DD}	-
USBDR_TXDRXD7/GPIO_39/QE_BRG_11	AB3	IO	OV_{DD}	-
USBDR_PCTL0/UART2_SOUT1/LB_POR_CFG_BOOT_ECC	W8	O	OV_{DD}	-
USBDR_PCTL1/UART2_SOUT2/UART2_RTS_B1/LB_POR_BOOT_ERR	W7	O	OV_{DD}	-
USBDR_STP/QE_EXT_REQ_2	W6	O	OV_{DD}	-
PCI				
PCI_INTA_B	B22	O	OV_{DD}	-
PCI_RESET_OUT_B	F19	O	OV_{DD}	-
PCI_AD0	B23	IO	OV_{DD}	-
PCI_AD1	C21	IO	OV_{DD}	-
PCI_AD2	E20	IO	OV_{DD}	-
PCI_AD3	G19	IO	OV_{DD}	-
PCI_AD4	C23	IO	OV_{DD}	-
PCI_AD5	H19	IO	OV_{DD}	-
PCI_AD6/CE_PIO_0	D21	IO	OV_{DD}	-
PCI_AD7	F20	IO	OV_{DD}	-

VDD	H8,H9,H10,H11,H12,M8, H13,N16,H14,H15,H16, P16,P8,L8,K16,J16,K8,J 8,R8,T16,R16,T8,T9,T11 ,T10,T12,T13,T14,T15	-	-	-
VSS	A1, C3, F22, J14, K14, M15, L15, N20, R9, Y21, T20, AB21, B1, C22,G4, K15, J15, M2, M22, P9, R10, V2, AA2, AC1, B4,D5, G20, J22, K20, M5, N9, P10, R11, V22, AA22,AC23, B6, D8, J2, K4, M9,L9, N10, P11, R12, W4, AB4, D11, B9, J9, K9, L10,M10, N11, P12, R13, Y7,AB6, B12, D14, J10, K10, L11, M11, P13, N12, R14, Y10,AB9, B15, D17, J11, K11, D20, B18, J12, K12, L13, L12, L14, K13, J13, F2, B21, M14, M13, M12, Y19, Y16, AB15, AB12, Y13, N13, N14, N15, P14, P15, R2, AB18, R15, R21, T4	-	-	-
NC	A23	-	-	-

Notes

1. This pin is an open drain signal. A weak pull-up resistor should be placed on this pin to OV_{DD}

2 This pin has weak pull-up that is always enabled.

4. OVDD here refers to NVDDA, NVDDB,NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.

23.1 Clocking in PCI host mode

When the MPC8309 is configured as a PCI host device (RCWH[PCIHOST] = 1), SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK multiplexors. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

23.1.1 PCI clock outputs (PCI_CLK[0:2])

When the MPC8309 is configured as a PCI host, it provides three separate clock output signals, PCI_CLK[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

23.2 Clocking in PCI agent mode

When the MPC8309 is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock. In agent mode, the SYS_CLK_IN signal should be tied to GND, and the clock output signals, PCI_CLK*n* and PCI_SYNC_OUT, are not used.

23.3 System clock domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create four major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*qe_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lbc_clk*)

The *csb_clk* frequency is derived from the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF} \qquad \textit{Eqn. 1}$$

In PCI host mode,

$$PCI\_SYNC\_IN = SYS\_CLK\_IN \div (1 + \sim\overline{CFG\_CLKIN\_DIV}) . \qquad \textbf{Eqn. 2}$$

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. For more information, see the Reset

Table 57. CSB frequency options

SPMF	csb_clk : sys_clk_in Ratio	PCI_SYNC_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

23.5 Core PLL configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 58. e300 Core PLL configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2

Table 58. e300 Core PLL configuration (continued)

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
01	0011	0	3:1	÷ 4
10	0011	0	3:1	÷ 8
11	0011	0	3:1	÷ 8

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

23.6 QUICC Engine PLL configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

Table 59. QUICC Engine PLL multiplication factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in the following table.

Table 60. QUICC Engine PLL VCO divider

RCWL[CEVCOD]	VCO Divider
00	2
01	4
10	8
11	Reserved

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

24.2.1 Experimental determination of the junction temperature with a heat sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

25 System design information

This section provides electrical and thermal design recommendations for successful application of the MPC8309.

25.1 System clocking

The MPC8309 includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 23.4, “System PLL configuration.”
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 23.5, “Core PLL configuration.”
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.