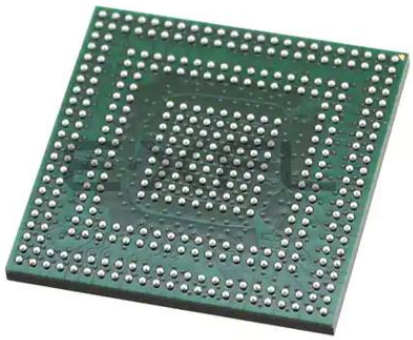

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8309cvmafdca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

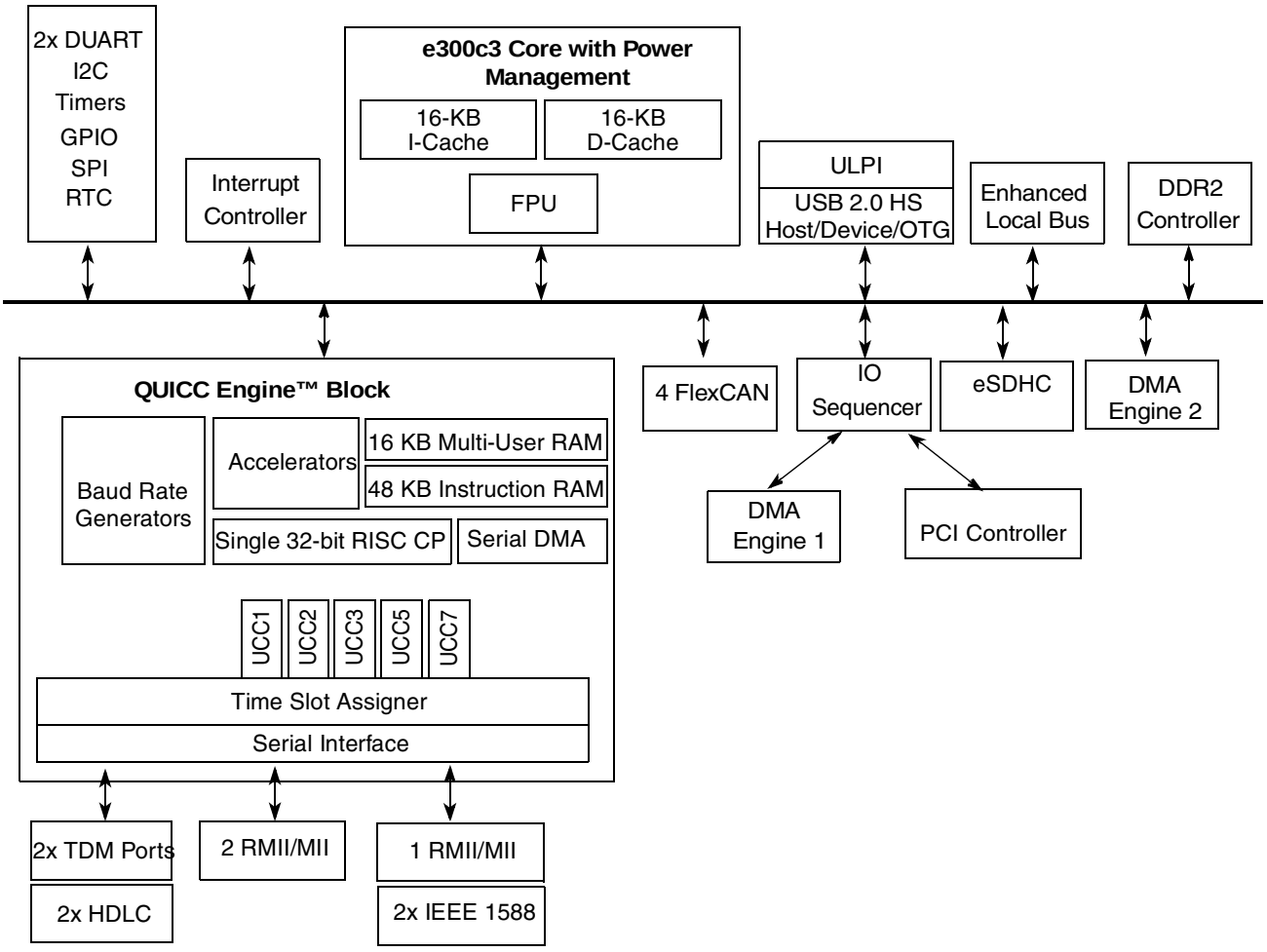

Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

  - External and internal interrupts directed to host processor
  - Unique vector number for each interrupt source
- PCI interface
  - Designed to comply with *PCI Local Bus Specification, Revision 2.3*
  - 32-bit PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - Not 5-V compatible
  - Support for host and agent modes
  - Support for PCI-to-memory and memory-to-PCI streaming
  - Memory pre-fetching of PCI read accesses and support for delayed read transactions
  - Support for posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration, supporting three masters on PCI
  - Arbiter support for two-level priority request/grant signal pairs
  - Support for accesses to all PCI address spaces
  - Support for parity
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Mapping from an external 32-/64-bit address space to the internal 32-bit local space
  - Support for dual address cycle (DAC) (as a target only)
  - Internal configuration registers accessible from PCI
  - Selectable snooping for inbound transactions
  - Four outbound Translation Address Windows
    - Support for mapping 32-bit internal local memory space to an external 32-bit PCI address space and translating that address within the PCI space
  - Four inbound Translation Address Windows corresponding to defined PCI BARs
    - The first BAR is 32-bits and dedicated to on-chip register access
    - The second BAR is 32-bits for general use
    - The remaining two BARs may be 32- or 64-bits and are also for general use
- Enhanced secure digital host controller (eSDHC)
  - Compatible with the *SD Host Controller Standard Specification Version 2.0* with test event register support
  - Compatible with the *MMC System Specification Version 4.2*
  - Compatible with the *SD Memory Card Specification Version 2.0* and supports the high capacity SD memory card
  - Compatible with the *SD Input/Output (SDIO) Card Specification, Version 2.0*
  - Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, and RS-MMC cards
  - Card bus clock frequency up to 33.33 MHz.

- Direct memory access (DMA) controller (DMA Engine 2)
  - Four independent fully programmable DMA channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Misaligned transfer capability for source/destination address
  - Data chaining and direct mode
  - Interrupt on completed segment, error, and chain
- DUART
  - Supports 2 DUART
  - Each has two 2-wire interfaces (RxD, TxD)
    - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- Power management controller (PMC)
  - Supports core doze/nap/sleep/ power management
  - Exits low power state and returns to full-on mode when
    - The core internal time base unit invokes a request to exit low power state
    - The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
  - General-purpose I/O (GPIO)
    - 56 parallel I/O pins multiplexed on various chip interfaces
    - Interrupt capability
- System timers
  - Periodic interrupt timer
  - Software watchdog timer
  - Eight general-purpose timers
- Real time clock (RTC) module
  - Maintains a one-second count, unique over a period of thousands of years
  - Two possible clock sources:
    - External RTC clock (RTC_PIT_CLK)
    - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8309. The MPC8309 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC electrical characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute maximum ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD1} AV_{DD2} AV_{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 1.98	V	—
PCI, Local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, eSDHC, FlexCAN, USB and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	2
Input voltage	DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	3
	DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	4
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

Table 9. RESET initialization timing specifications (continued)

Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL lock times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

5.1 Reset signals DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 reset signals mentioned in Table 9.

Table 11. Reset signals DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	— ±	5	µA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8309. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC electrical characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8309 when GV_{DD}(typ) = 1.8 V.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 16. DDR2 SDRAM output AC timing specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
$\overline{MCS}$ output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.4 2.5	 — 	ns	3
$\overline{MCS}$ output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.4 2.5	 — 	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.8 0.9	 — 	ns	5
MDQ/MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100	 — 	ps	5
MDQS preamble start	t_{DDKHMP}	0.75 x t_{MCK}	—	ns	6
MDQS epilogue end	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. t_{DDKHMP} follows the symbol conventions described in note 1.

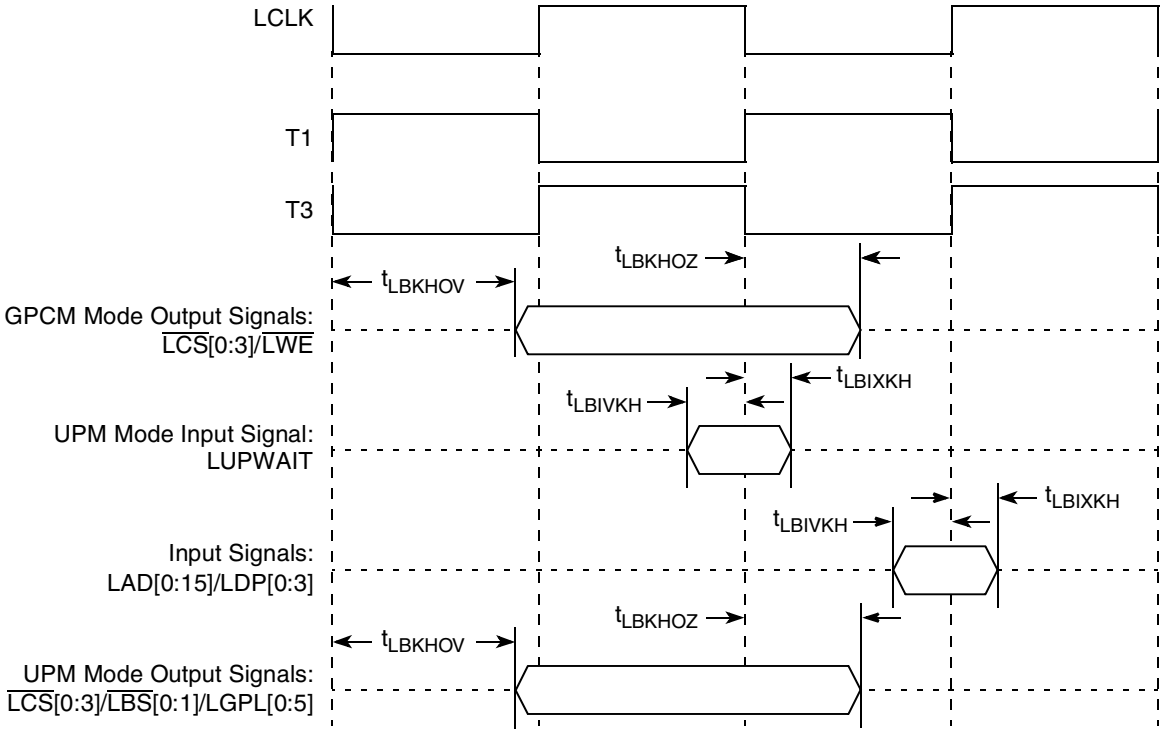

Figure 9. Enhanced local bus signals, GPCM/UPM signals for LCRR[CLKDIV] = 2

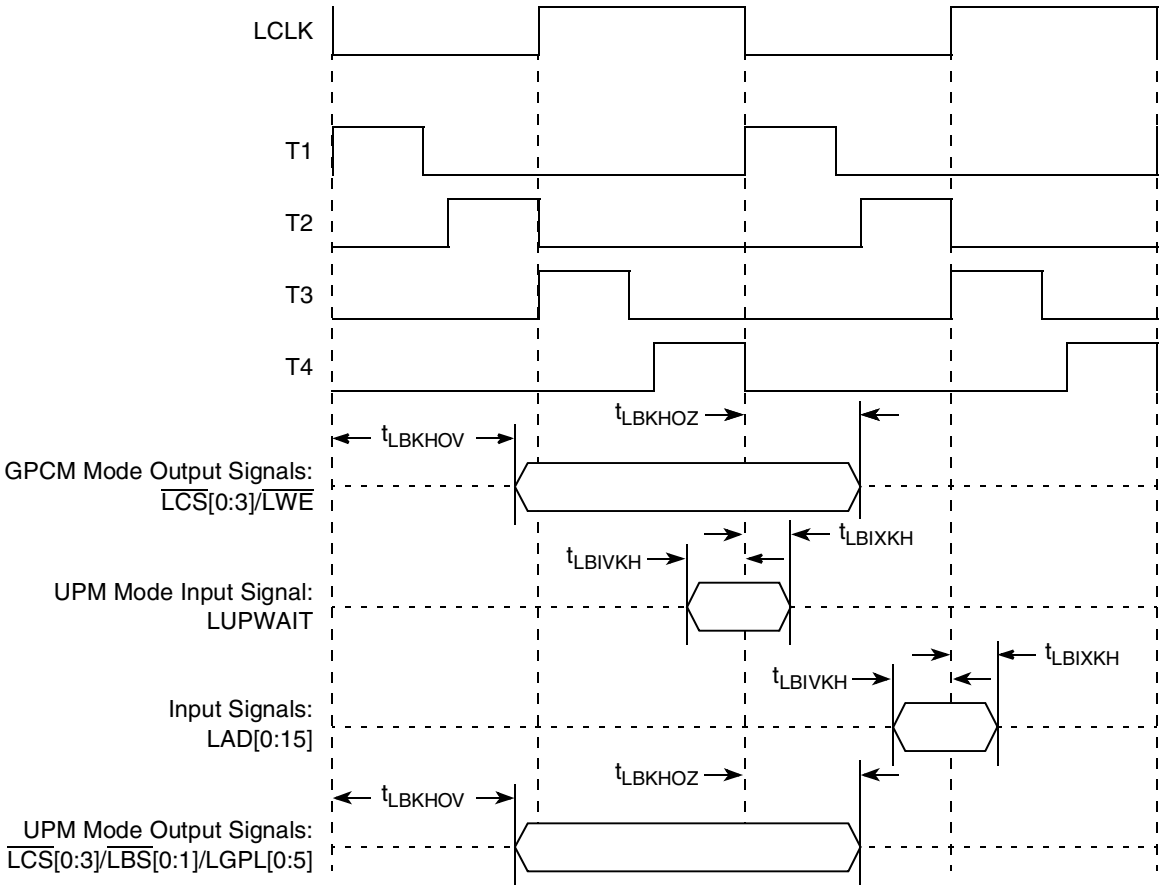

Figure 10. Enhanced local bus signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

8 Ethernet and MII management

This section provides the AC and DC electrical characteristics for Ethernet interfaces.

8.1 Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC (management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet management interface electrical characteristics."

8.1.1 DC electrical characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in the following table.

The following figure shows the RMII receive AC timing diagram.

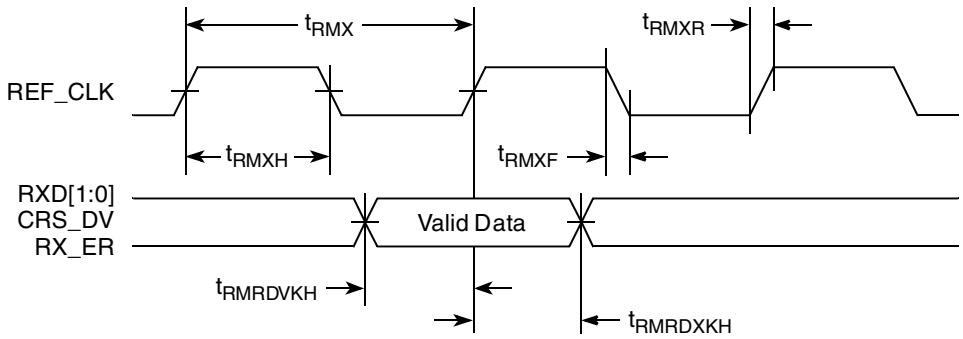

Figure 16. RMII receive AC timing diagram

8.3 Ethernet management interface electrical characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet controller (10/100 Mbps)—MII/RMII electrical characteristics."

8.3.1 MII management DC electrical characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in the following table.

Table 24. MII management DC electrical characteristics when powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII management AC electrical specifications

The following table provides the MII management AC timing specifications.

Table 25. MII management AC timing specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—

Table 25. MII management AC timing specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

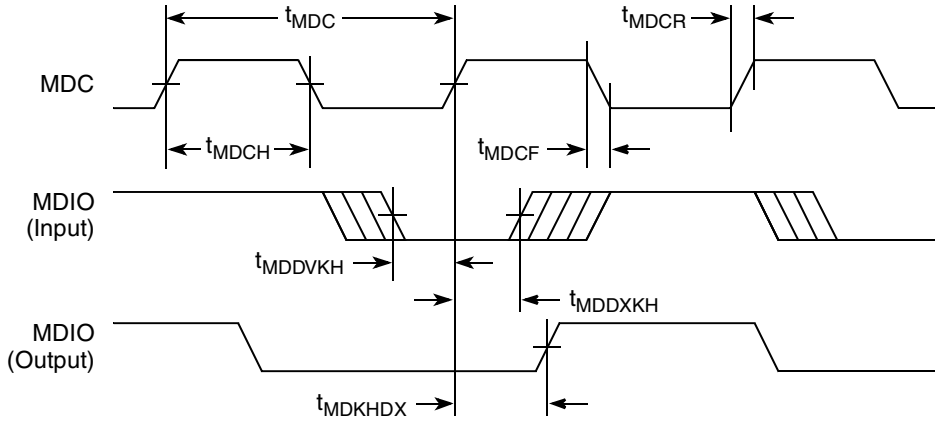

Figure 17. MII management interface timing diagram

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8309.

9.1 TDM/SI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 TDM/SI.

Table 26. TDM/SI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

9.2 TDM/SI AC timing specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 27. TDM/SI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

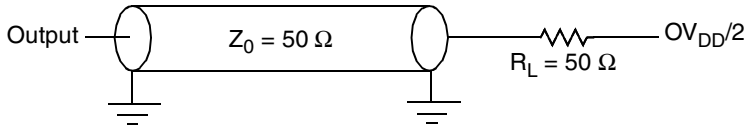

Figure 18. TDM/SI AC test load

15 FlexCAN

This section describes the DC and AC electrical specifications for the FlexCAN interface.

15.1 FlexCAN DC electrical characteristics

The following table provides the DC electrical characteristics for the FlexCAN interface.

Table 39. FlexCAN DC electrical characteristics (3.3V)

For recommended operating conditions, see Table 2

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 2.
2. OV_{IN} represents the input voltage of the supply. It is referenced in Table 2.

15.2 FlexCAN AC timing specifications

The following table provides the AC timing specifications for the FlexCAN interface.

Table 40. FlexCAN AC timing specifications

For recommended operating conditions, see Table 2

Parameter	Min	Max	Unit	Notes
Baud rate	10	1000	Kbps	—

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8309.

19.1 IPIC DC electrical characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8309.

Table 47. IPIC DC electrical characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC timing specifications

The following table provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8309.

20.1 SPI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 SPI.

22.3 Pinout listings

Following table shows the pin list of the MPC8309.

Table 53. MPC8309 pinout listing

Signal	Terminal	Pad Dir	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	U5	IO	GV_{DD}	—
MEMC_MDQ1	AA1	IO	GV_{DD}	—
MEMC_MDQ2	W3	IO	GV_{DD}	—
MEMC_MDQ3	R5	IO	GV_{DD}	—
MEMC_MDQ4	W2	IO	GV_{DD}	—
MEMC_MDQ5	U3	IO	GV_{DD}	—
MEMC_MDQ6	U2	IO	GV_{DD}	—
MEMC_MDQ7	T3	IO	GV_{DD}	—
MEMC_MDQ8	H3	IO	GV_{DD}	—
MEMC_MDQ9	H4	IO	GV_{DD}	—
MEMC_MDQ10	G3	IO	GV_{DD}	—
MEMC_MDQ11	F3	IO	GV_{DD}	—
MEMC_MDQ12	G5	IO	GV_{DD}	—
MEMC_MDQ13	F4	IO	GV_{DD}	—
MEMC_MDQ14	F5	IO	GV_{DD}	—
MEMC_MDQ15	E3	IO	GV_{DD}	—
MEMC_MDQ16	V4	IO	GV_{DD}	—
MEMC_MDQ17	Y2	IO	GV_{DD}	—
MEMC_MDQ18	Y1	IO	GV_{DD}	—
MEMC_MDQ19	U4	IO	GV_{DD}	—
MEMC_MDQ20	V1	IO	GV_{DD}	—
MEMC_MDQ21	R4	IO	GV_{DD}	—
MEMC_MDQ22	U1	IO	GV_{DD}	—
MEMC_MDQ23	T2	IO	GV_{DD}	—
MEMC_MDQ24	J5	IO	GV_{DD}	—
MEMC_MDQ25	G2	IO	GV_{DD}	—
MEMC_MDQ26	G1	IO	GV_{DD}	—
MEMC_MDQ27	F1	IO	GV_{DD}	—
MEMC_MDQ28	E2	IO	GV_{DD}	—

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1 A20		IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

HDLC/TDM/GPIO				
HDLC1_TXCLK[CLK16]/GPIO_0/QE_BRG_5/TDM1_TCK[CLK4]	AA20	IO	OV_{DD}	-
HDLC1_RXCLK[CLK15]/GPIO_1/TDM1_RCK[CLK3]	AA21	IO	OV_{DD}	-
HDLC1_TXD/GPIO_2/TDM1_TD/CFG_RESET_SOURCE[0]	AB22	IO	OV_{DD}	1
HDLC1_RXD/GPIO_3/TDM1_RD	AB23	IO	OV_{DD}	-
HDLC1_CD_B/GPIO_4/TDM1_TFS	W19	IO	OV_{DD}	-
HDLC1_CTS_B/GPIO_5/TDM1_RFS	V19	IO	OV_{DD}	-
HDLC1_RTS_B/GPIO_6/TDM1_STROBE_B/CFG_RESET_SOURCE[1]	AA23	IO	OV_{DD}	-
HDLC2_TXCLK[CLK14]/GPIO_16/QE_BRG_7/TDM2_TCK[CLK6]	Y20	IO	OV_{DD}	-
HDLC2_RXCLK[CLK13]/GPIO_17/TDM2_RCK[CLK5]/QE_BRG_8	Y22	IO	OV_{DD}	-
HDLC2_TXD/GPIO_18/TDM2_TD/CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	1
HDLC2_RXD/GPIO_19/TDM2_RD	W21	IO	OV_{DD}	-
HDLC2_CD_B/GPIO_20/TDM2_TFS	V20	IO	OV_{DD}	-
HDLC2_CTS_B/GPIO_21/TDM2_RFS	Y23	IO	OV_{DD}	-
HDLC2_RTS_B/GPIO_22/TDM2_STROBE_B/CFG_RESET_SOURCE[3]	U20	IO	OV_{DD}	-
Power				
AVDD1	L16	-	-	-
AVDD2	M16	-	-	-
AVDD3	N8	-	-	-
GVDD	F6, G6, H6, J6, K6, L6, N6, P6, R6, T6, U6, V6, V7	-	-	-
NVDD	F7, F8, F9, F10, F11, F12, F13,F14, F15, F16, F17, F18, G18,H18, J18, L18, M18, N18, P18,R18, T18, U18, V8, V9, V10, V11, V12, V13,V14, V15, V16, V17, V18	-	-	-

Table 55. Operating Frequencies for MAPBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR2 memory bus frequency (MCLK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

23.4 System PLL configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

Table 56. System PLL multiplication factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 23, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

qe_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QUICC Engine VCO Frequency = *qe_clk* × VCO divider × (1 + CEPDF)

23.7 Suggested PLL configurations

To simplify the PLL configurations, the MPC8309 might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs is configured separately.

The following table shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 61. Suggested PLL configurations

Conf No.	SPMF	Core PLL	CEPMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0111	0	33.33	133.33	266.66	233
2	0010	0000100	0111	1	66.67	133.33	266.66	233
3	0100	0000101	0111	0	33.33	133.33	333.33	233
4	0101	0000101	1001	0	25	125	312.5	225
5	0010	0000101	0111	1	66.67	133.33	333.33	233
6	0100	0000110	0111	0	33.33	133.33	399.96	233
7	0101	0000110	1000	0	25	125	375	225
8	0010	0000110	0011	0	66.67	133.33	399.96	233
9	0101	0000101	0111	0	33.33	166.67	416.67	233

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 63. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	?
R_P	42 Target	20 Target	Z_0	?
Differential	NA	NA	Z_{DIFF}	?

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: MPC8309EC
Rev. 2
09/2012