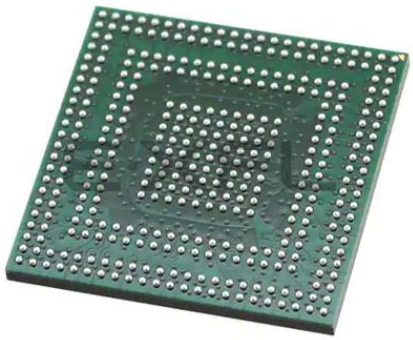

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8309vmaddca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

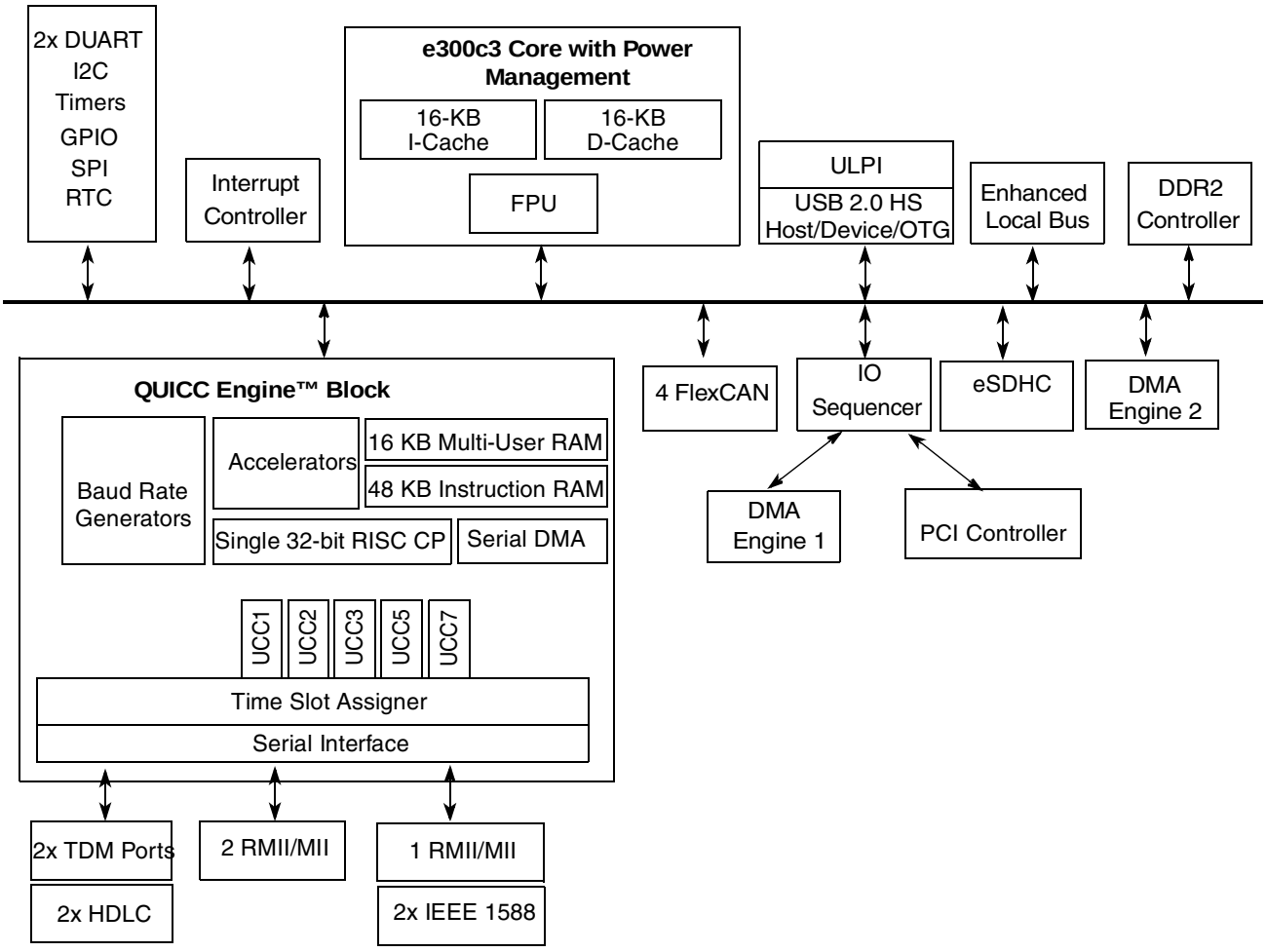


Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking.*

- DDR SDRAM memory controller
  - Programmable timing supporting DDR2 SDRAM
  - Integrated SDRAM clock generation
  - Supports 8-bit ECC
  - 16/32-bit data interface, up to 333-MHz data rate
  - 14 address lines
  - The following SDRAM configurations are supported:
    - Up to two physical banks (chip selects), 512-MB addressable space for 32 bit data interface
    - 64-Mbit to 2-Gbit devices with x8/x16/x32 data ports (no direct x4 support)
  - One 16-bit device or two 8-bit devices on a 16-bit bus, or two 16-bit devices or four 8-bit devices on a 32-bit bus Support for up to 16 simultaneous open pages for DDR2
  - Two clock pair to support up to 4 DRAM devices
  - Supports auto refresh
  - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
  - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
  - Eight chip selects supporting eight external slaves
    - Four chip selects dedicated
    - Four chip selects offered as multiplexed option
  - Supports boot from parallel NOR Flash and parallel NAND Flash
  - Supports programmable clock ratio dividers
  - Up to eight-beat burst transfers
  - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - NAND Flash control machine (FCM)
  - Variable memory block sizes for FCM, GPCM, and UPM mode
  - Default boot ROM chip select with configurable bus width (8 or 16)
  - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for external and internal discrete interrupt sources
  - Programmable highest priority request
  - Six groups of interrupts with programmable priority

  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine1
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- IO Sequencer

4.2 AC electrical characteristics

The primary clock source for the MPC8309 can be one of two inputs, SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or agent mode. The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) AC timing specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC timing specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{SYS\_CLK\_IN}$	24 —		66.67	MHz	1
SYS_CLK_IN cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	1.1	—	2.8	ns	2
PCI_SYNC_IN rise and fall time	t_{PCH}, t_{PCL}	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8309. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET initialization timing specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{SYS\_CLK\_IN}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN or PCI_SYNC_IN (in agent mode)	32	—	$t_{SYS\_CLK\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{SYS\_CLK\_IN}$	1

Table 9. RESET initialization timing specifications (continued)

Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{SYS\_CLK\_IN}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:
1. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
2. POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL lock times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

5.1 Reset signals DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 reset signals mentioned in Table 9.

Table 11. Reset signals DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	— ±	5	µA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8309. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC electrical characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8309 when GV_{DD}(typ) = 1.8 V.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

The following figure shows the RMII transmit AC timing diagram.

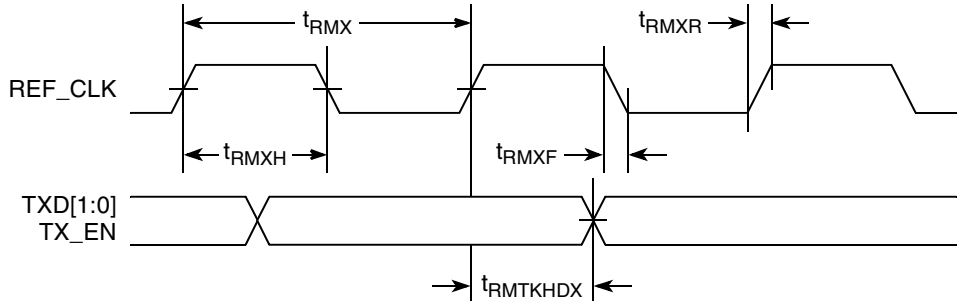


Figure 15. RMII transmit AC timing diagram

8.2.2.2 RMII receive AC timing specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8309.

9.1 TDM/SI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 TDM/SI.

Table 26. TDM/SI DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

9.2 TDM/SI AC timing specifications

The following table provides the TDM/SI input and output AC timing specifications.

Table 27. TDM/SI AC timing specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	14	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

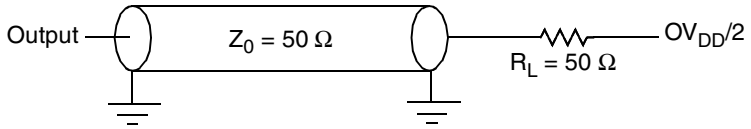


Figure 18. TDM/SI AC test load

13 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8309.

13.1 DUART DC electrical characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8309.

Table 35. DUART DC electrical characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

13.2 DUART AC electrical specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8309.

Table 36. DUART AC timing specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Table 38. eSDHC AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD/SDIO card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–33.25 MHz for an SD/SDIO card and 0–52 MHz for an MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

The following figure provides the eSDHC clock input timing diagram.

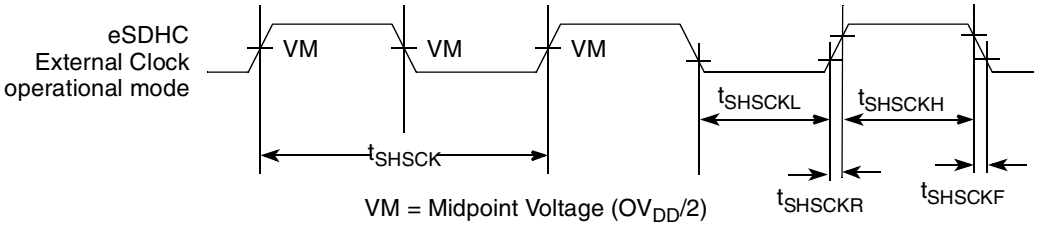


Figure 28. eSDHC clock input timing diagram

The following figure provides the data and command input/output timing diagram.

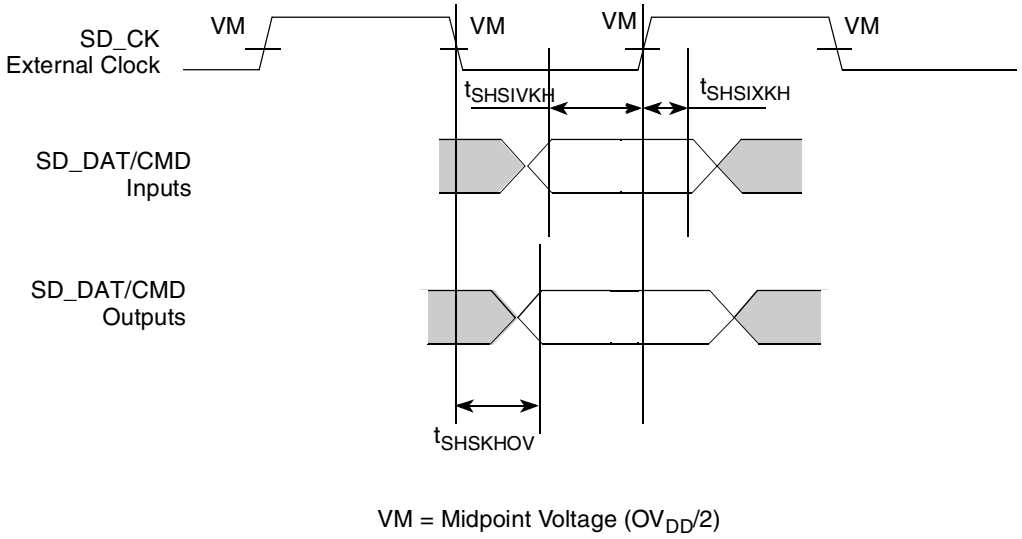


Figure 29. eSDHC data and command input/output timing diagram referenced to clock

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8309.

17.1 Timer DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 43. Timer DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

17.2 Timer AC timing specifications

The following table provides the timer input and output AC timing specifications.

Table 44. Timer input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

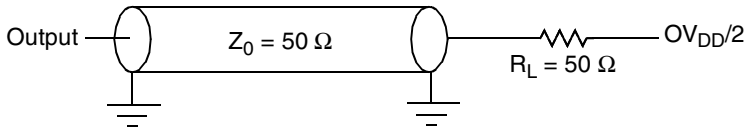


Figure 32. Timers AC test load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8309.

19.1 IPIC DC electrical characteristics

The following table provides the DC electrical characteristics for the external interrupt pins of the MPC8309.

Table 47. IPIC DC electrical characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output High Voltage	V_{OH}	I_{OL} = -8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$, $\overline{\text{MCP\_OUT}}$, and QE ports Interrupts.
2. $\overline{\text{MCP\_OUT}}$ is open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC timing specifications

The following table provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8309.

20.1 SPI DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 SPI.

FEC2_RX_CLK[CLK7]/GPIO_34	W14	IO	OV_{DD}	-
FEC2_RX_DV/GTM2_TIN2/GPIO_35	AB16	IO	OV_{DD}	-
FEC2_RX_ER/GTM2_TGATE2_B/GPIO_36	Y14	IO	OV_{DD}	-
FEC2_RXD0/GPIO_37	AA15	IO	OV_{DD}	-
FEC2_RXD1/GTM2_TIN3/GPIO_38	AC15	IO	OV_{DD}	-
FEC2_RXD2/GTM2_TGATE3_B/GPIO_39	AC16	IO	OV_{DD}	-
FEC2_RXD3/GPIO_40	AA14	IO	OV_{DD}	-
FEC2_TX_CLK[CLK8]/GTM2_TIN4/GPIO_41	W13	IO	OV_{DD}	-
FEC2_TX_EN/GTM2_TGATE4_B/GPIO_42	AB14	IO	OV_{DD}	-
FEC2_TX_ER/GTM2_TOUT4_B/GPIO_43	AC14	IO	OV_{DD}	-
FEC2_TXD0/GTM2_TOUT1_B/GPIO_44	Y12	IO	OV_{DD}	-
FEC2_TXD1/GTM2_TOUT2_B/GPIO_45	AA13	IO	OV_{DD}	-
FEC2_TXD2/GTM2_TOUT3_B/GPIO_46	AB13	IO	OV_{DD}	-
FEC2_TXD3/GPIO_47	AC13	IO	OV_{DD}	-
FEC3_COL/GPIO_48	AC12	IO	OV_{DD}	-
FEC3_CRS/GPIO_49	W11	IO	OV_{DD}	-
FEC3_RX_CLK[CLK11]/GPIO_50	W12	IO	OV_{DD}	-
FEC3_RX_DV/FEC1_TMR_TX_ESFD/GPIO_51	AA12	IO	OV_{DD}	-
FEC3_RX_ER/FEC1_TMR_RX_ESFD/GPIO_52	AB11	IO	OV_{DD}	-
FEC3_RXD0/FEC2_TMR_TX_ESFD/GPIO_53	AA11	IO	OV_{DD}	-
FEC3_RXD1/FEC2_TMR_RX_ESFD/GPIO_54	AC11	IO	OV_{DD}	-
FEC3_RXD2/FEC_TMR_TRIG1/GPIO_55	Y11	IO	OV_{DD}	-
FEC3_RXD3/FEC_TMR_TRIG2/GPIO_56	AB10	IO	OV_{DD}	-
FEC3_TX_CLK[CLK12]/FEC_TMR_CLK/GPIO_57	AC10	IO	OV_{DD}	-
FEC3_TX_EN/FEC_TMR_GCLK/GPIO_58	AA10	IO	OV_{DD}	-
FEC3_TX_ER/FEC_TMR_PP1/GPIO_59	AC8	IO	OV_{DD}	-
FEC3_TXD0/FEC_TMR_PP2/GPIO_60	AB8	IO	OV_{DD}	-
FEC3_TXD1/FEC_TMR_PP3/GPIO_61	AA9	IO	OV_{DD}	-
FEC3_TXD2/FEC_TMR_ALARM1/GPIO_62	AA8	IO	OV_{DD}	-
FEC3_TXD3/FEC_TMR_ALARM2/GPIO_63	AC7	IO	OV_{DD}	-

HDLC/TDM/GPIO				
HDLC1_TXCLK[CLK16]/GPIO_0/QE_BRG_5/TDM1_TCK[CLK4]	AA20	IO	OV_{DD}	-
HDLC1_RXCLK[CLK15]/GPIO_1/TDM1_RCK[CLK3]	AA21	IO	OV_{DD}	-
HDLC1_TXD/GPIO_2/TDM1_TD/CFG_RESET_SOURCE[0]	AB22	IO	OV_{DD}	1
HDLC1_RXD/GPIO_3/TDM1_RD	AB23	IO	OV_{DD}	-
HDLC1_CD_B/GPIO_4/TDM1_TFS	W19	IO	OV_{DD}	-
HDLC1_CTS_B/GPIO_5/TDM1_RFS	V19	IO	OV_{DD}	-
HDLC1_RTS_B/GPIO_6/TDM1_STROBE_B/CFG_RESET_SOURCE[1]	AA23	IO	OV_{DD}	-
HDLC2_TXCLK[CLK14]/GPIO_16/QE_BRG_7/TDM2_TCK[CLK6]	Y20	IO	OV_{DD}	-
HDLC2_RXCLK[CLK13]/GPIO_17/TDM2_RCK[CLK5]/QE_BRG_8	Y22	IO	OV_{DD}	-
HDLC2_TXD/GPIO_18/TDM2_TD/CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	1
HDLC2_RXD/GPIO_19/TDM2_RD	W21	IO	OV_{DD}	-
HDLC2_CD_B/GPIO_20/TDM2_TFS	V20	IO	OV_{DD}	-
HDLC2_CTS_B/GPIO_21/TDM2_RFS	Y23	IO	OV_{DD}	-
HDLC2_RTS_B/GPIO_22/TDM2_STROBE_B/CFG_RESET_SOURCE[3]	U20	IO	OV_{DD}	-
Power				
AVDD1	L16	-	-	-
AVDD2	M16	-	-	-
AVDD3	N8	-	-	-
GVDD	F6, G6, H6, J6, K6, L6, N6, P6, R6, T6, U6, V6, V7	-	-	-
NVDD	F7, F8, F9, F10, F11, F12, F13,F14, F15, F16, F17, F18, G18,H18, J18, L18, M18, N18, P18,R18, T18, U18, V8, V9, V10, V11, V12, V13,V14, V15, V16, V17, V18	-	-	-

23 Clocking

The following figure shows the internal distribution of clocks within the MPC8309.

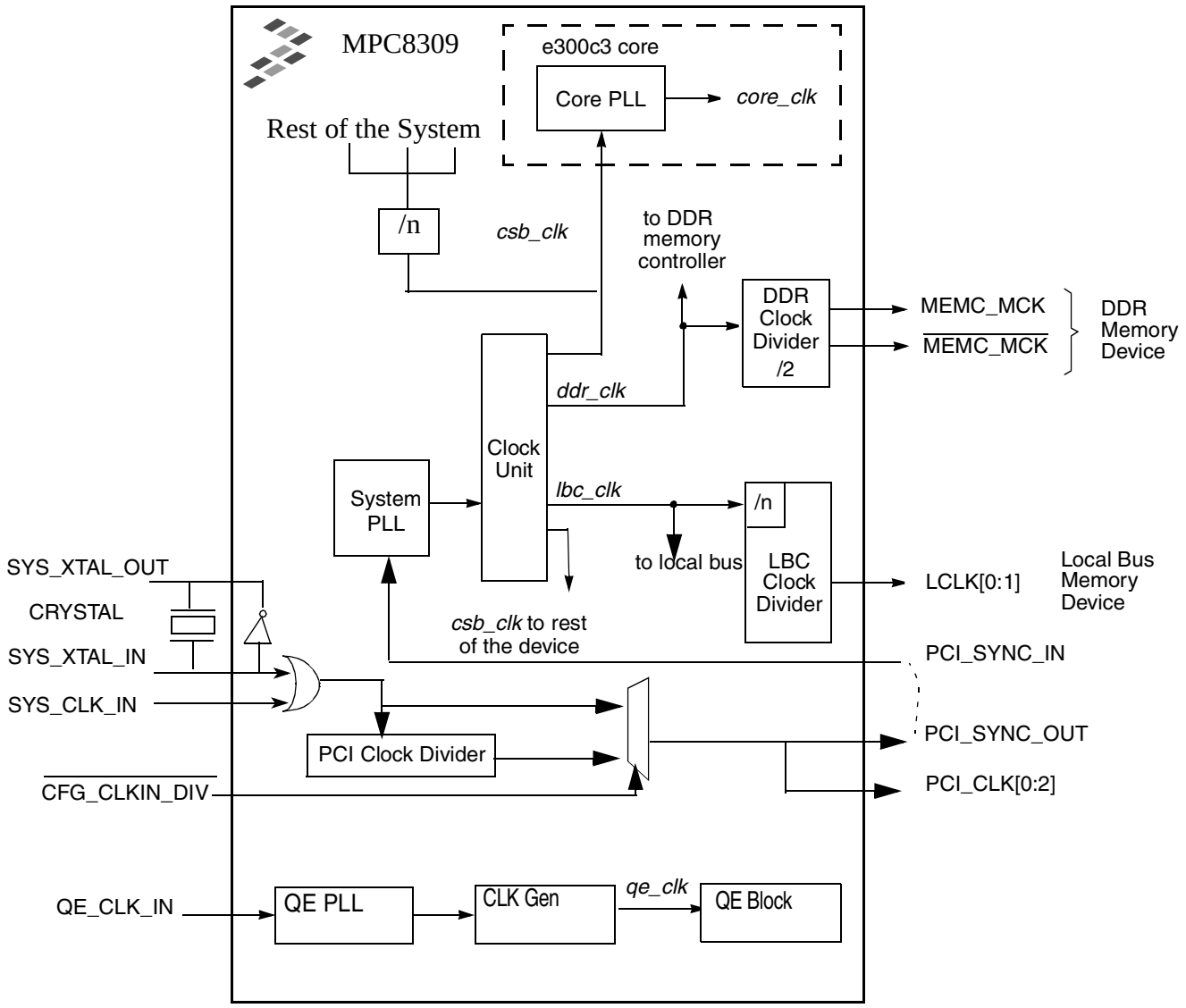


Figure 43. MPC8309 clock subsystem

The primary clock source for the MPC8309 can be one of three inputs,Crystal(SYS_XTAL_IN), SYS_CLK_IN or PCI_SYNC_IN, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

Table 55. Operating Frequencies for MAPBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR2 memory bus frequency (MCLK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz

Notes:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting csb_clk, MCLK, LCLK, and core_clk frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR2 data rate is 2× the DDR2 memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the lb_clk frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the csb_clk frequency (depending on RCWL[LBCM]).

23.4 System PLL configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider). The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

Table 56. System PLL multiplication factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 23, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low select the ratio between the primary clock input (*SYS_CLK_IN)* and the internal coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 57. CSB frequency options

SPMF	csb_clk : sys_clk_in Ratio	PCI_SYNC_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

23.5 Core PLL configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 58. e300 Core PLL configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷ 2
01	0001	1	1.5:1	÷ 4
10	0001	1	1.5:1	÷ 8
11	0001	1	1.5:1	÷ 8
00	0010	0	2:1	÷ 2
01	0010	0	2:1	÷ 4
10	0010	0	2:1	÷ 8
11	0010	0	2:1	÷ 8
00	0010	1	2.5:1	÷ 2
01	0010	1	2.5:1	÷ 4
10	0010	1	2.5:1	÷ 8
11	0010	1	2.5:1	÷ 8
00	0011	0	3:1	÷ 2

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.1.5 Heat sinks and junction-to-case thermal resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance as shown in the following equation:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

24.2 Heat sink attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint

lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

24.2.1 Experimental determination of the junction temperature with a heat sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface.

From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance using the following equation:

$$T_J = T_C + (R_{\theta JC} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

25 System design information

This section provides electrical and thermal design recommendations for successful application of the MPC8309.

25.1 System clocking

The MPC8309 includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied SYS_CLK_IN input. The frequency ratio between the system and SYS_CLK_IN is selected using the system PLL ratio configuration bits as described in Section 23.4, “System PLL configuration.”
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 23.5, “Core PLL configuration.”
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 63. Impedance characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration and Power Management	DDR DRAM	Symbol	Unit
R_N	42 Target	20 Target	Z_0	?
R_P	42 Target	20 Target	Z_0	?
Differential	NA	NA	Z_{DIFF}	?

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.5 Configuration pin multiplexing

The MPC8309 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

26 Ordering information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 26.1, "Part numbers fully addressed by this document."

26.1 Part numbers fully addressed by this document

The following table provides the Freescale part numbering nomenclature for the MPC8309 family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

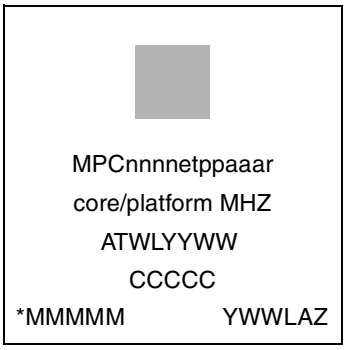
Table 64. Part numbering nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8309	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AD = 266 MHz AF = 333 MHz AG = 400 MHz AH = 417MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 22, "Package and pin listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

26.2 Part marking

Parts are marked as in the example shown in the following figure.



MAPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 46. Freescale part marking for MAPBGA devices

The following table shows the SVR Settings.

Table 65. SVR settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8309	MAPBGA	0x8110_0010	0x8110_0011
Note: PVR = 0x8085_0020			