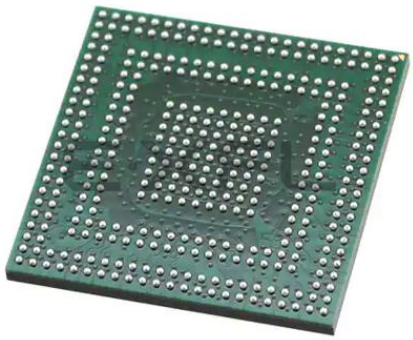

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8309vmafdca

1 Overview

The MPC8309 incorporates the e300c3 (MPC 6 03e-based) core built on Power Architecture® technology, which includes 16 KB of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8309 also includes a 32-bit PCI controller, two DMA engines and a 16/32-bit DDR2 memory controller with 8-bit ECC.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8309. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8309 is shown in the following figure.

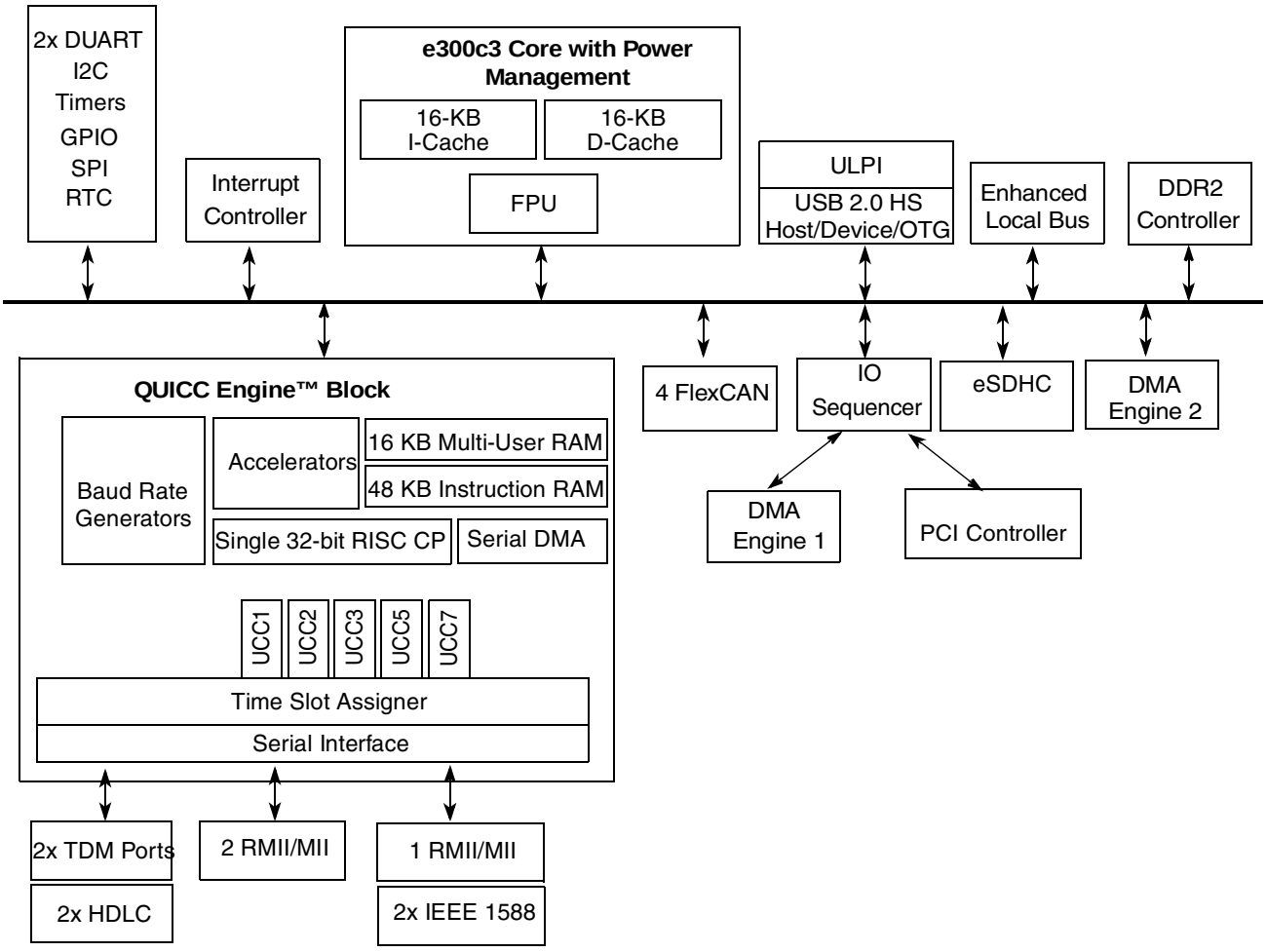


Figure 1. MPC8309 block diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8309 provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

  - Supports 1-/4-bit SD and SDIO modes, 1-/4-bit modes
    - Up to 133 Mbps data transfer for SD/SDIO/MMC cards using 4 parallel data lines
  - Supports block sizes of 1 ~ 4096 bytes
- Universal serial bus (USB) dual-role controller
  - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
  - Supports operation as a stand-alone USB host controller
  - Supports operation as a stand-alone USB device
  - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
  - Up to 64 flexible message buffers of zero to eight bytes data length
  - Powerful Rx FIFO ID filtering, capable of matching incoming IDs
  - Selectable backwards compatibility with previous FlexCAN module version
  - Programmable loop-back mode supporting self-test operation
  - Global network time, synchronized by a specific message
  - Independent of the transmission medium (an external transceiver is required)
  - Short latency time due to an arbitration scheme for high-priority messages
- Dual I^2C interfaces
  - Two-wire interface
  - Multiple-master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - I^2C1 can be used as the boot sequencer
- DMA Engine1
  - Support for the DMA engine with the following features:
    - Sixteen DMA channels
    - All data movement via dual-address transfers: read from source, write to destination
    - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
    - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
      - Explicit software initiation
      - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
    - Support for fixed-priority and round-robin channel arbitration
    - Channel completion reported via optional interrupt requests
  - Support for scatter/gather DMA processing
- IO Sequencer

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O power dissipation

Interface	Parameter	GV_{DD} (1.8 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 16 bits	0.149	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.415	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, PCI, SPI, Timer output, FlexCAN, eSDHC				

Note:
1. Typical I/O power is based on a nominal voltage of V_{DD} = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock input timing

This section provides the clock input DC and AC electrical characteristics for the MPC8309.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of OV_{DD}; fall time refers to transitions from 90% to 10% of OV_{DD}.

4.1 DC electrical characteristics

The following table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC specifications for the MPC8309. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC electrical characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±5	μA
SYS_CLK_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

Table 15. DDR2 SDRAM input AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

The following figure shows the input timing diagram for the DDR controller.

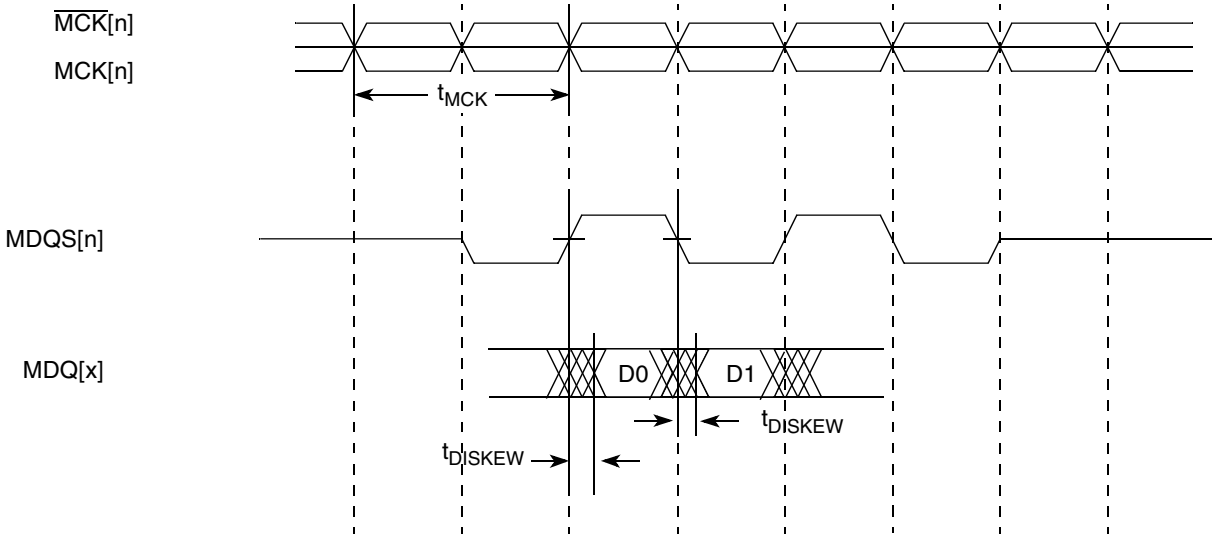


Figure 4. DDR input timing diagram

6.2.2 DDR2 SDRAM output AC timing specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM output AC timing specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK cycle time, (MCK/$\overline{MCK}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
333 MHz		2.4	—		
266 MHz		2.5			

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

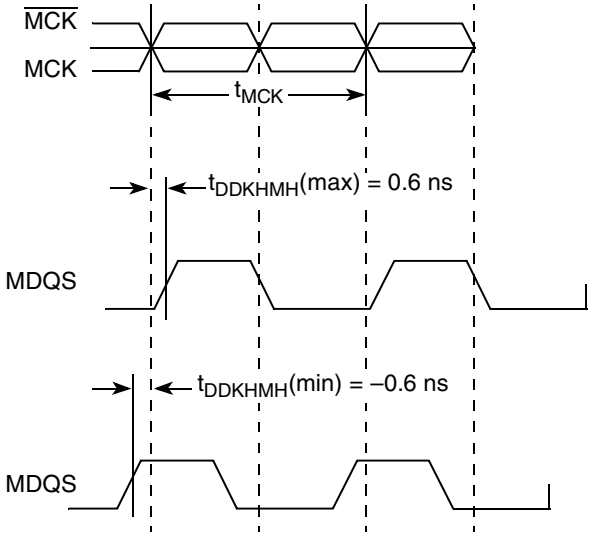


Figure 5. Timing diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

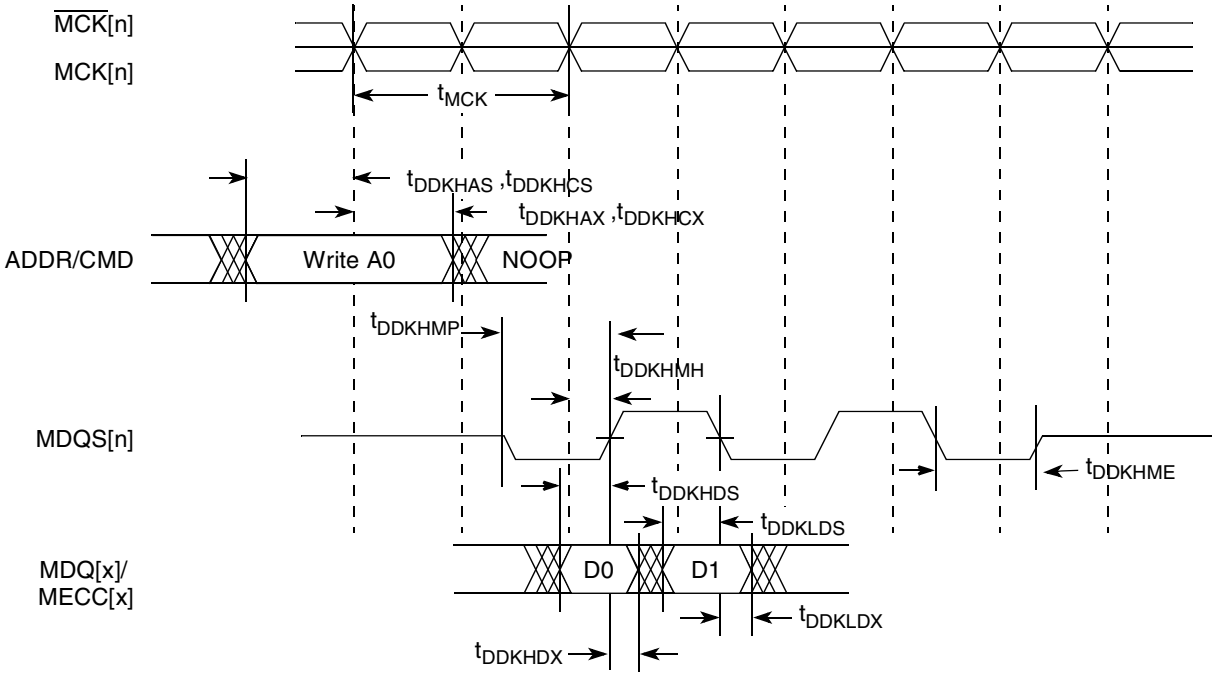


Figure 6. DDR2 SDRAM output timing diagram

Table 19. MII and RMII DC electrical characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND 0.	50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC timing specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII transmit AC timing specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII transmit AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min) t	MTXF	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

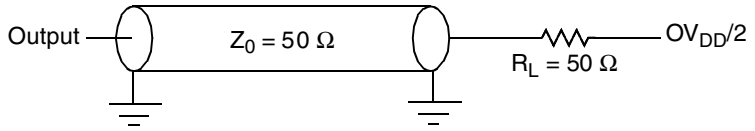


Figure 11. AC test load

The following figure shows the MII transmit AC timing diagram.

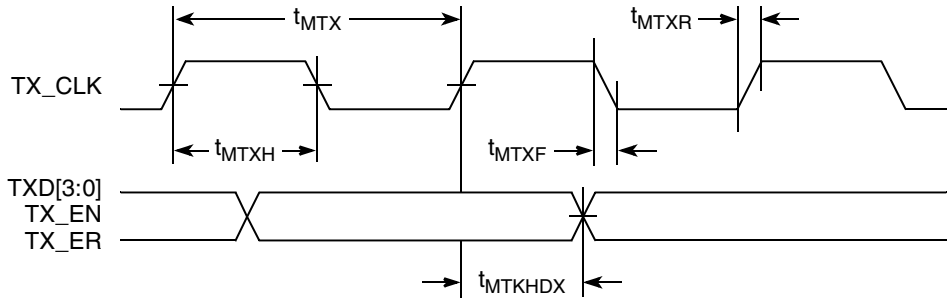


Figure 12. MII transmit AC timing diagram

8.2.1.2 MII receive AC timing specifications

The following table provides the MII receive AC timing specifications.

Table 21. MII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the RMII transmit AC timing diagram.

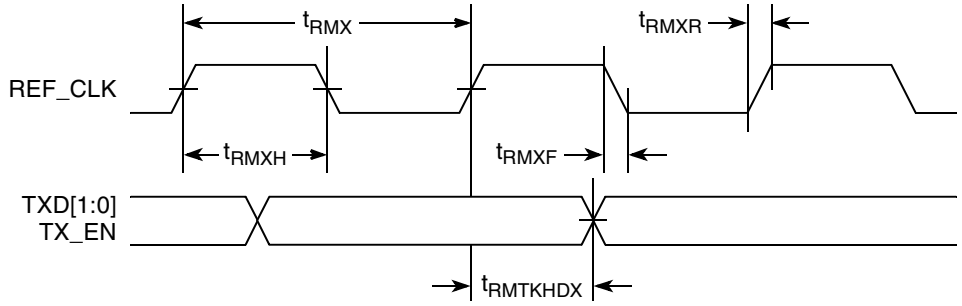


Figure 15. RMII transmit AC timing diagram

8.2.2.2 RMII receive AC timing specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII receive AC timing specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 25. MII management AC timing specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	8.5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII management AC timing diagram.

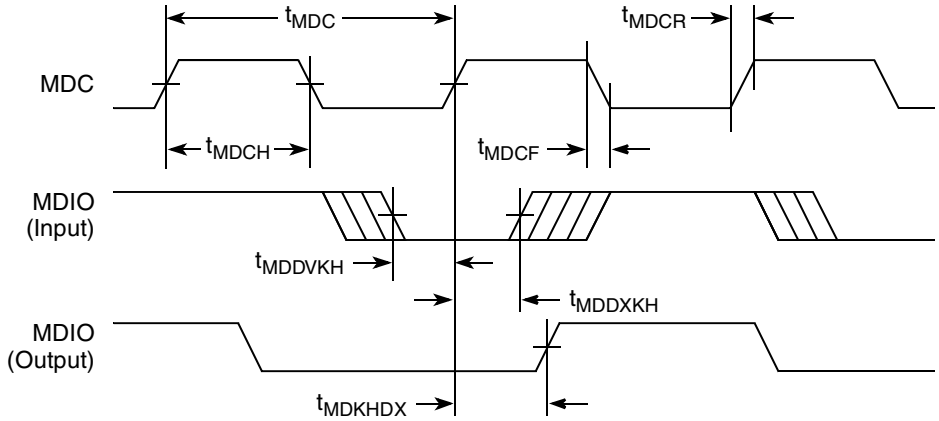


Figure 17. MII management interface timing diagram

Table 29. HDLC AC timing specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	9	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

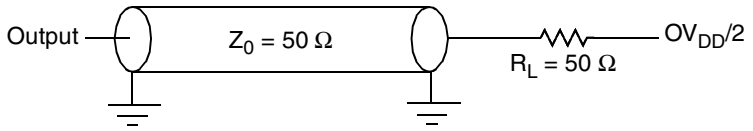
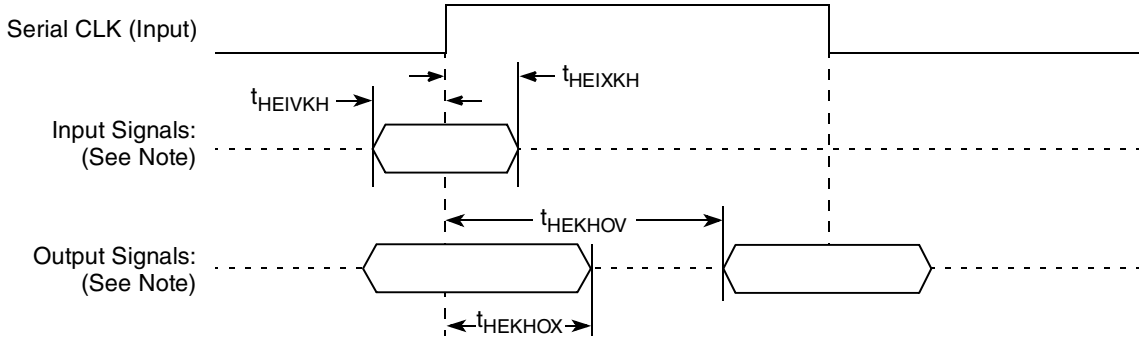


Figure 20. AC test load

Figure 21 and Figure 22 represent the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

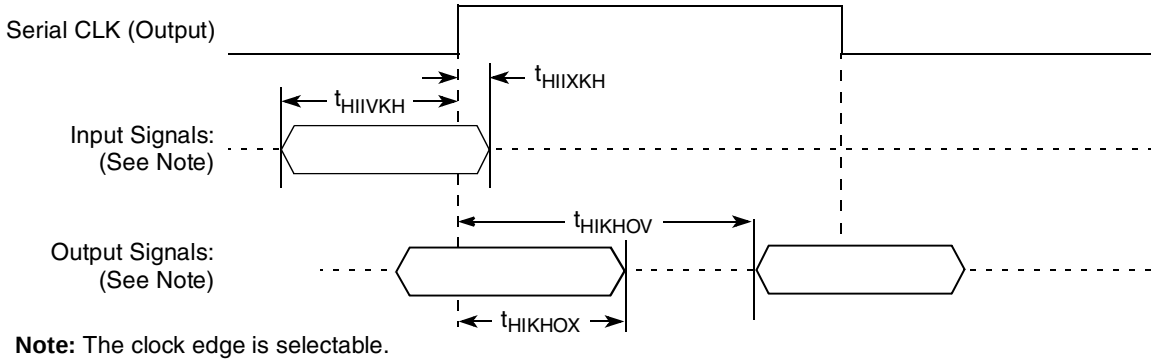
The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 21. AC timing (external clock) diagram

The following figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 22. AC timing (internal clock) diagram

11 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8309.

11.1 PCI DC electrical characteristics

Table 30 provides the DC electrical characteristics for the PCI interface of the MPC8309.

Table 30. PCI DC electrical characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications.*

11.2 PCI AC electrical specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8309. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8309 is configured as a host or agent device. Table 31 shows the PCI AC timing specifications at 66 MHz.

Table 32 shows the PCI AC timing specifications at 33 MHz.

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8309.

17.1 Timer DC electrical characteristics

The following table provides the DC electrical characteristics for the MPC8309 timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_PIT_CLK.

Table 43. Timer DC electrical characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA 2.	4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	— ±	5	μA

17.2 Timer AC timing specifications

The following table provides the timer input and output AC timing specifications.

Table 44. Timer input AC timing specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

The following figure provides the AC test load for the timers.

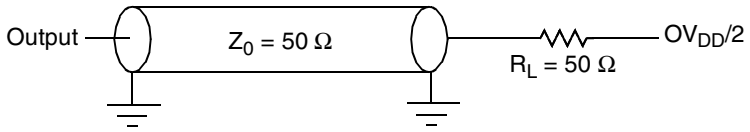


Figure 32. Timers AC test load

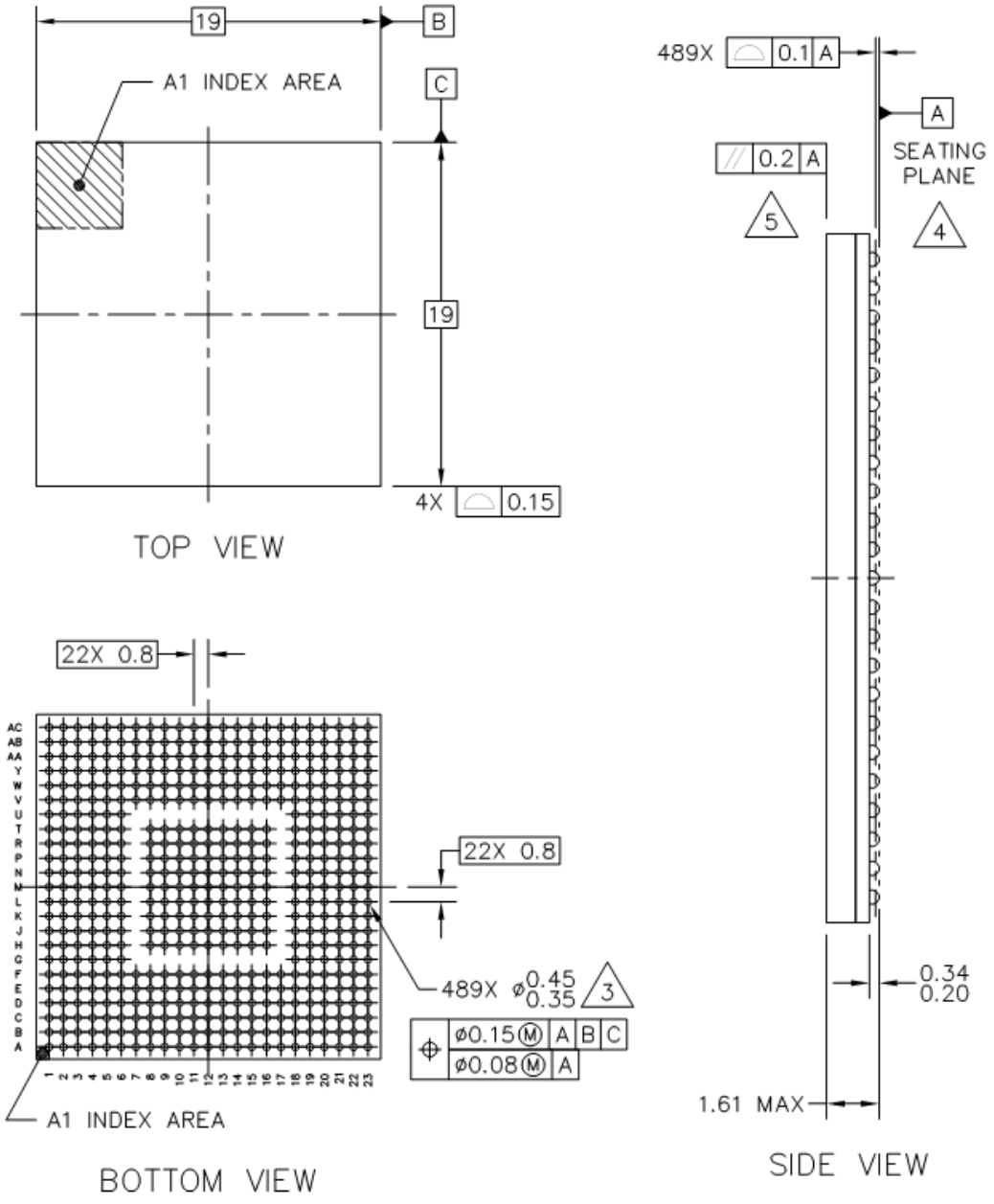


Figure 42. Mechanical dimensions and bottom surface nomenclature of the MPC8309 MAPBGA

Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

MEMC_MDQ29	D2	IO	GV_{DD}	—
MEMC_MDQ30	C2	IO	GV_{DD}	—
MEMC_MDQ31	C1	IO	GV_{DD}	—
MEMC_MECC0	Y5	IO	GV_{DD}	—
MEMC_MECC1	AA4	IO	GV_{DD}	—
MEMC_MECC2	Y4	IO	GV_{DD}	—
MEMC_MECC3	AA3	IO	GV_{DD}	—
MEMC_MECC4	AC2	IO	GV_{DD}	—
MEMC_MECC5	AB2	IO	GV_{DD}	—
MEMC_MECC6	Y3	IO	GV_{DD}	—
MEMC_MECC7	AB1	IO	GV_{DD}	—
MEMC_MDM0	W1	O	GV_{DD}	—
MEMC_MDM1	E1	O	GV_{DD}	—
MEMC_MDM2	V3	O	GV_{DD}	—
MEMC_MDM3	D1	O	GV_{DD}	—
MEMC_MDM8	W5	O	GV_{DD}	—
MEMC_MDQS0	T5	IO	GV_{DD}	—
MEMC_MDQS1	H5	IO	GV_{DD}	—
MEMC_MDQS2	P5	IO	GV_{DD}	—
MEMC_MDQS3	E5	IO	GV_{DD}	-
MEMC_MDQS8	V5	IO	GV_{DD}	-
MEMC_MBA0	K2	O	GV_{DD}	-
MEMC_MBA1	K3	O	GV_{DD}	-
MEMC_MBA2	N5	O	GV_{DD}	-
MEMC_MA0	L3	O	GV_{DD}	-
MEMC_MA1	L5	O	GV_{DD}	-
MEMC_MA2	L2	O	GV_{DD}	-
MEMC_MA3	L1	O	GV_{DD}	-
MEMC_MA4	M3	O	GV_{DD}	-
MEMC_MA5	M4	O	GV_{DD}	-
MEMC_MA6	M1	O	GV_{DD}	-
MEMC_MA7	N1	O	GV_{DD}	-
MEMC_MA8	N2	O	GV_{DD}	-
MEMC_MA9	N3	O	GV_{DD}	-
MEMC_MA10	L4	O	GV_{DD}	-
MEMC_MA11	P2	O	GV_{DD}	-
MEMC_MA12	N4	O	GV_{DD}	-

LA22	A11	O	OV_{DD}	-
LA23	A10	O	OV_{DD}	-
LA24	C12	O	OV_{DD}	-
LA25	A12	O	OV_{DD}	-
LCLK0	E13	O	OV_{DD}	-
LCS_B0	D13	O	OV_{DD}	2
LCS_B1	C13	O	OV_{DD}	2
LCS_B2	A13	O	OV_{DD}	2
LCS_B3	B13	O	OV_{DD}	2
LWE_B0/LFWE_B0/LBS_B0	A14	O	OV_{DD}	-
LWE_B1/LBS_B1	B14	O	OV_{DD}	-
LBCTL	A15	O	OV_{DD}	-
LGPL0/LFCLE	C14	O	OV_{DD}	-
LGPL1/LFALE	C15	O	OV_{DD}	-
LGPL2/LOE_B/LFRE_B	B16	O	OV_{DD}	2
LGPL3/LFWP_B	A16	O	OV_{DD}	-
LGPL4/LGTA_B/LUPWAIT/LFRB_B	E14	IO	OV_{DD}	2
LGPL5	B17	O	OV_{DD}	-
LALE	A17	O	OV_{DD}	-
DUART				
UART1_SOUT1	AB7	O	OV_{DD}	-
UART1_SIN1	AC6	I	OV_{DD}	-
UART1_SOUT2/UART1_RTS_B1	W10	O	OV_{DD}	-
UART1_SIN2/UART1_CTS_B1	Y9	I	OV_{DD}	-
I2C				
IIC_SDA1 A20		IO	OV_{DD}	1
IIC_SCL1	B20	IO	OV_{DD}	1
IIC_SDA2 /CKSTOP_OUT_B	D19	IO	OV_{DD}	1
IIC_SCL2/CKSTOP_IN_B	C20	IO	OV_{DD}	1
Interrupts				
IRQ_B0_MCP_IN_B	A21	IO	OV_{DD}	-
IRQ_B1/MCP_OUT_B	A22	IO	OV_{DD}	-
IRQ_B2/CKSTOP_IN_B	E18	I	OV_{DD}	-
IRQ_B3/CKSTOP_OUT_B/INTA_B	E19	IO	OV_{DD}	-
SPI				
SPIMOSI	B19	IO	OV_{DD}	-

SPIMISO	E16	IO	OV_{DD}	-
SPICLK E17		IO	OV_{DD}	-
SPISEL	A19	I	OV_{DD}	-
SPISEL_BOOT_B	D18		OV_{DD}	-
JTAG				
TCK	A2	I	OV_{DD}	-
TDI	C5	I	OV_{DD}	2
TDO	A3	O	OV_{DD}	-
TMS	D7	I	OV_{DD}	2
TRST_B	E9	I	OV_{DD}	2
Test Interface				
TEST_MODE	C6	I	OV_{DD}	-
System Control Signals				
HRESET_B	W23	IO	OV_{DD}	1
PORESET_B	W22	I	OV_{DD}	-
Clock Interface				
QE_CLK_IN	R22	I	OV_{DD}	-
SYS_CLK_IN	R23	I	OV_{DD}	-
SYS_XTAL_IN	P23	I	OV_{DD}	-
SYS_XTAL_OUT	P19	O	OV_{DD}	-
PCI_SYNC_IN	T23	I	OV_{DD}	-
PCI_SYNC_OUT	R20	O	OV_{DD}	-
CFG_CLKIN_DIV_B	U23	I	OV_{DD}	-
RTC_PIT_CLOCK	V23	I		
Miscellaneous Signals				
QUIESCE_B	D6	O	OV_{DD}	-
THERM0	E8		OV_{DD}	-
GPIO				
GPIO_0/SD_CLK/MSRCID0 (DDR ID)	E4	IO	OV_{DD}	-
GPIO_1/SD_CMD/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	-
GPIO_2/SD_CD/MSRCID2 (DDR ID)	D3	IO	OV_{DD}	-
GPIO_3/SD_WP/MSRCID3 (DDR ID)	E7	IO	OV_{DD}	-
GPIO_4/SD_DAT0/MSRCID4 (DDR ID)	D4	IO	OV_{DD}	-
GPIO_5/SD_DAT1/MDVAL (DDR ID)	C4	IO	OV_{DD}	-
GPIO_6/SD_DAT2/QE_EXT_REQ_3	B2	IO	OV_{DD}	-
GPIO_7/SD_DAT3/QE_EXT_REQ_1	B3	IO	OV_{DD}	-
GPIO_8/RXCAN1/LSRCID0/LCS_B4	C16	IO	OV_{DD}	-

FEC2_RX_CLK[CLK7]/GPIO_34	W14	IO	OV_{DD}	-
FEC2_RX_DV/GTM2_TIN2/GPIO_35	AB16	IO	OV_{DD}	-
FEC2_RX_ER/GTM2_TGATE2_B/GPIO_36	Y14	IO	OV_{DD}	-
FEC2_RXD0/GPIO_37	AA15	IO	OV_{DD}	-
FEC2_RXD1/GTM2_TIN3/GPIO_38	AC15	IO	OV_{DD}	-
FEC2_RXD2/GTM2_TGATE3_B/GPIO_39	AC16	IO	OV_{DD}	-
FEC2_RXD3/GPIO_40	AA14	IO	OV_{DD}	-
FEC2_TX_CLK[CLK8]/GTM2_TIN4/GPIO_41	W13	IO	OV_{DD}	-
FEC2_TX_EN/GTM2_TGATE4_B/GPIO_42	AB14	IO	OV_{DD}	-
FEC2_TX_ER/GTM2_TOUT4_B/GPIO_43	AC14	IO	OV_{DD}	-
FEC2_TXD0/GTM2_TOUT1_B/GPIO_44	Y12	IO	OV_{DD}	-
FEC2_TXD1/GTM2_TOUT2_B/GPIO_45	AA13	IO	OV_{DD}	-
FEC2_TXD2/GTM2_TOUT3_B/GPIO_46	AB13	IO	OV_{DD}	-
FEC2_TXD3/GPIO_47	AC13	IO	OV_{DD}	-
FEC3_COL/GPIO_48	AC12	IO	OV_{DD}	-
FEC3_CRS/GPIO_49	W11	IO	OV_{DD}	-
FEC3_RX_CLK[CLK11]/GPIO_50	W12	IO	OV_{DD}	-
FEC3_RX_DV/FEC1_TMR_TX_ESFD/GPIO_51	AA12	IO	OV_{DD}	-
FEC3_RX_ER/FEC1_TMR_RX_ESFD/GPIO_52	AB11	IO	OV_{DD}	-
FEC3_RXD0/FEC2_TMR_TX_ESFD/GPIO_53	AA11	IO	OV_{DD}	-
FEC3_RXD1/FEC2_TMR_RX_ESFD/GPIO_54	AC11	IO	OV_{DD}	-
FEC3_RXD2/FEC_TMR_TRIG1/GPIO_55	Y11	IO	OV_{DD}	-
FEC3_RXD3/FEC_TMR_TRIG2/GPIO_56	AB10	IO	OV_{DD}	-
FEC3_TX_CLK[CLK12]/FEC_TMR_CLK/GPIO_57	AC10	IO	OV_{DD}	-
FEC3_TX_EN/FEC_TMR_GCLK/GPIO_58	AA10	IO	OV_{DD}	-
FEC3_TX_ER/FEC_TMR_PP1/GPIO_59	AC8	IO	OV_{DD}	-
FEC3_TXD0/FEC_TMR_PP2/GPIO_60	AB8	IO	OV_{DD}	-
FEC3_TXD1/FEC_TMR_PP3/GPIO_61	AA9	IO	OV_{DD}	-
FEC3_TXD2/FEC_TMR_ALARM1/GPIO_62	AA8	IO	OV_{DD}	-
FEC3_TXD3/FEC_TMR_ALARM2/GPIO_63	AC7	IO	OV_{DD}	-

Configuration chapter in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

The *qe_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) as the following equation:

$$qe\_clk = (QE\_CLK\_IN \times CEPMF) \div (1 + CEPDF) \quad \textbf{Eqn. 3}$$

For more information, see the QUICC Engine PLL Multiplication Factor section and the "QUICC Engine PLL Division Factor" section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LCLK). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. For more information, see the LBC Bus Clock and Clock Ratios section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset.

The following table specifies which units have a configurable clock frequency. For detailed description, refer to the "System Clock Control Register (SCCR)" section in the *MPC8309 PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.

Table 54. Configurable clock units

Unit	Default Frequency	Options
I2C,SDHC, USB, DMA Complex	*csb_clk*	Off, csb_clk, *csb_clk*/2, *csb_clk*/3

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

The following table provides the maximum operating frequencies for the MPC8309 MAPBGA under recommended operating conditions (see Table 2).

Table 55. Operating Frequencies for MAPBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	417	MHz
Coherent system bus frequency (*csb_clk*)	167	MHz
QUICC Engine frequency (*qe_clk*)	233	MHz

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Output buffer DC impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

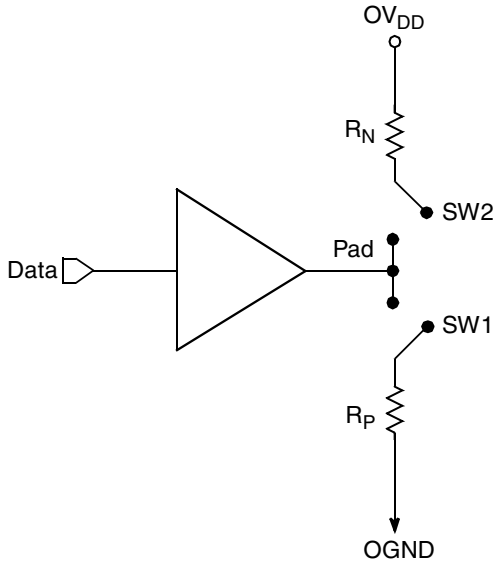


Figure 45. Driver impedance measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

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