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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45k42t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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0/1	28-Pin SPDIP/SOIC/SSOP	28-Pin (U)QFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	l²C	SPI	UART	WSD	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC0	11	8	ANC0	_	_	_		—	_		I	T1CKI ⁽¹⁾ T3CKI ⁽¹⁾ T3G ⁽¹⁾ SMTWIN1 ⁽¹⁾	_	I	_	_		IOCC0	SOSCO
RC1	12	9	ANC1	-	-	-	_	_	_	_	_	SMTSIG1 ⁽¹⁾	CCP2 ⁽¹⁾	_	-	_	_	IOCC1	SOSCI
RC2	13	10	ANC2	-	_	-	—	_	_	_	_	T5CKI ⁽¹⁾	CCP1 ⁽¹⁾	_	_	_	_	IOCC2	_
RC3	14	11	ANC3	-	_	-	_	SCL1 ^(3,4)	SCK1 ⁽¹⁾	_	_	T2IN ⁽¹⁾	-	_	_	_	-	IOCC3	-
RC4	15	12	ANC4	—	_	—	_	SDA1 ^(3,4)	SDI1 ⁽¹⁾	—	_	—	-	_	_	_	—	IOCC4	_
RC5	16	13	ANC5	—	—	—	_	—	—	—	_	T4IN ⁽¹⁾	—	_	_	—	_	IOCC5	_
RC6	17	14	ANC6	—	—	—	—	—	—	CTS1 ⁽¹⁾	_	—	—	_	_	—	—	IOCC6	_
RC7	18	15	ANC7	_	—	_	_	—	—	RX1 ⁽¹⁾	-		-	_	_	—	_	IOCC7	
RE3	1	26	-	-	-	-	—	—	—	—	—	—	—	-	—	-	—	IOCE3	MCLR VPP
Vdd	20	17	_	-	_	-	_	_	_	_	_	_	-	_	_	_	-	—	_
Vss	8, 19	5, 16	—	—	—	—		—	—	-	—	—	—	_	—	—	-	-	—
OUT ⁽²⁾	_		ADGRDA ADGRDB		_	C1OUT C2OUT	_	SDA1 SCL1 SDA2 SCL2	SS1 SCK1 SDO1	DTR1 RTS1 TX1 DTR2 RTS2 TX2	DSM	TMR0	CCP1 CCP2 CCP3 CCP4 PWM5OUT PWM6OUT PWM7OUT PWM8OUT	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B	CLC10UT CLC20UT CLC30UT CLC40UT	NCO	CLKR	_	_
Note	1:	This	s is a PPS rem	nappable inr	out signal. The i	input functio	on may	be moved fro	m the default	location show	vn to one of seve	eral other PORT	nins			1			

TABLE 1: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK42) (CONTINUED)

1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.

2: All output signals shown in this row are PPS remappable.

This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers. These pins can be configured for I²C and SMB™ 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I²C specific or SMBUs input buffer thresholds. 4:

3:

5.7.4 FIXED VOLTAGE REFERENCE DATA

The DIA stores measured FVR voltages for this device in mV for the different buffer settings of 1x, 2x or 4x at Program Memory locations 3F0030h to 3F003Bh. For more information on the FVR, refer to **Section 34.0 "Fixed Voltage Reference (FVR)"**.

- FVRA1X stores the value of ADC FVR1 Output voltage for 1x setting (in mV)
- FVRA2X stores the value of ADC FVR1 Output Voltage for 2x setting (in mV)
- FVRA4X stores the value of ADC FVR1 Output Voltage for 4x setting (in mV)
- FVRC1X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC2X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC4X stores the value of Comparator FVR2 output voltage for 4x setting (in mV)

5.8 Device Configuration Information

The Device Configuration Information (DCI) is a dedicated region in the Program memory space mapped from 3FFF00h to 3FFF09h. The data stored in these locations is read-only and cannot be erased.

Refer to Table 5-4: Device Configuration Information for PIC18(L)F26/27/45/55/46/47/56/57K42 for the complete DCI table address and description. The DCI holds information about the device which is useful for programming and Bootloader applications.

The erase size is the minimum erasable unit in the PFM, expressed as rows. The total device Flash memory capacity is (Row Size * Number of rows)

	Nome	DESCRIPTION					
ADDRESS	Name	DESCRIPTION	PIC18(L)F45/55K42	55K42 PIC18(L)F26/46/56K42 PIC18(L)F27/47/57K4		UNITS	
3F FF00h-3F FF01h	ERSIZ	Erase Row Size	64	64	64	Words	
3F FF02h-3F FF03h	WLSIZ	Number of write latches per row	128	128	128	Bytes	
3F FF04h-3F FF05h	URSIZ	Number of User Rows	256	512	1024	Rows	
3F FF06h-3F FF07h	EESIZ	Data EEPROM memory size	256	1024	1024	Bytes	
3F FF08h-3F FF09h	PCNT	Pin Count	40 ⁽¹⁾ /48	28/40 ⁽¹⁾ /48	28/40 ⁽¹⁾ /48	Pins	

TABLE 5-4:DEVICE CONFIGURATION INFORMATION FOR PIC18(L)F26/27/45/55/46/47/56/57K42

Note 1: Pin count of 40 is also used for 44-pin part.

REGISTER 7 -	5: OSCF	RQ: HFINTO	SC FREQUE	NCY SELEC	TION REGIS	TER			
U-0	U-0	U-0	U-0	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q		
—	_	_	—	FRQ<3:0>					
bit 7							bit 0		

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R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Reset value is determined by hardware

bit 7-4 Unimplemented: Read as '0'

bit 3-0 FRQ<3:0>: HFINTOSC Frequency Selection bits⁽¹⁾

FRQ<3:0>	Nominal Freq (MHz)					
1001						
1010						
1111						
1110	Reserved					
1101	1					
1100	1					
1011	1					
1000	64					
0111	48					
0110	32					
0101	16					
0100	12					
0011	8					
0010	4					
0001	2					
0000	1					

Note 1: Refer to Table 7-2 for more information.

9.3 Interrupt Priority

The final priority level for any pending source of interrupt is determined first by the user-assigned priority of that source in the IPRx register, then by the natural order priority within the IVT. The sections below detail the operation of Interrupt priorities.

9.3.1 USER (SOFTWARE) PRIORITY

User-assigned interrupt priority is enabled by setting the IPEN bit in the INTCON0 register (Register 9-1). Each peripheral interrupt source can be assigned a high or low priority level by the user. The userassignable interrupt priority control bits for each interrupt are located in the IPRx registers (Registers 9-25 through 9-35).

The interrupts are serviced based on predefined interrupt priority scheme defined below.

- Interrupts set by the user as high-priority interrupt have higher precedence of execution. High-priority interrupts will override a low-priority request when:
 - a) A low priority interrupt has been requested or its request is already pending.
 - b) A low- and high-priority interrupt are triggered concurrently, i.e., on the same instruction cycle⁽¹⁾.
 - c) A low-priority interrupt was requested and the corresponding Interrupt Service Routine is currently executing. In this case, the lower priority interrupt routine will complete executing after the high-priority interrupt has been serviced⁽²⁾.
- 2. Interrupts set by the user as a low priority have the lower priority of execution and are preempted by any high-priority interrupt.
- Interrupts defined with the same software priority cannot preempt or interrupt each other. Concurrent pending interrupts with the same user priority are resolved using the natural order priority. (when MVECEN = ON) or in the order the interrupt flag bits are polled in the ISR (when MVECEN = OFF).

- Note 1: When a high priority interrupt preempts a concurrent low priority interrupt, the GIEL bit may be cleared in the high priority Interrupt Service Routine. If the GIEL bit is cleared, the low priority interrupt will NOT be serviced even if it was originally requested. The corresponding interrupt flag needs to be cleared in user code.
 - 2: When a high priority interrupt is requested while a low priority Interrupt Service Routine is executing, the GIEL bit may be cleared in the high priority Interrupt Service Routine. The pending low priority interrupt will resume even if the GIEL bit is cleared.

9.4.3 PREEMPTING LOW PRIORITY INTERRUPTS

Low-priority interrupts can be preempted by high priority interrupts. While in the low priority ISR, if a high-priority interrupt arrives, the high priority interrupt request is generated and the low priority ISR is suspended, while the high priority ISR is executed, see Figure 9-4.

After the high priority ISR is complete and if any other high priority interrupt requests are not active, the execution returns to the preempted low priority ISR.

Note 1: The high priority interrupt flag must be cleared to avoid recursive interrupts.

2: If a low-priority ISR was already serviced halfway before moving on to a high priority ISR, then the low priority ISR is completely serviced even if user code clears GIEL.

FIGURE 9-4: INTERRUPT EXECUTION: HIGH PRIORITY INTERRUPT PREEMPTING LOW PRIORITY INTERRUPTS



R/W/HS-0/	0 R/W/HS-0/0	R/W/HS-0/0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
CLC1IF	CWG1IF	NCO1IF	-	CCP1IF	TMR2IF	TMR1GIF	TMR1IF
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable I	oit	U = Unimplen	nented bit, read	as '0'	
u = Bit is un	changed	x = Bit is unkn	own	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is s	et	'0' = Bit is clea	ared	HS = Bit is se	t in hardware		
bit 7	CLC1IF: CLC	1 Interrupt Flag	g bit				
	1 = Interrupt	has occurred (r	must be clear	ed by software)		
	0 = Interrupt	event has not o	occurred				
bit 6	CWG1IF: CW	G1 Interrupt FI	ag bit				
	1 = Interrupt	has occurred (r	nust be clear	ed by software)		
L:1 F							
DILD		Di interrupt Fla	ig bit must be clear	ad by coffware	N N		
	0 = Interrupt	event has not o	nust be clear	ed by soltware)		
bit 4	Unimplemen	ted: Read as ')'				
bit 3	CCP1IF: CCF	P1 Interrupt Flag	a bit				
	1 = Interrupt	t has occurred (must be cleared by software)					
	0 = Interrupt	event has not o	occurred	5	,		
bit 2	TMR2IF: TMF	R2 Interrupt Fla	g bit				
	1 = Interrupt	has occurred (r	nust be clear	ed by software)		
	0 = Interrupt	event has not c	occurred				
bit 1	TMR1GIF: TN	/IR1 Gate Inter	rupt Flag bit				
	1 = Interrupt	has occurred (r	nust be clear	ed by software)		
hit O							
DILU	1 = Interrupt	has occurred (r	y DIL Must be clear	ed by software)		
	0 = Interrupt	event has not o	ccurred	cu by soltware)		
Note 1: In	nterrupt flag bits g enable bit, or the g	et set when an lobal enable bi	interrupt con t. User softwa	dition occurs, r are should ensu	egardless of the ire the appropri	e state of its con ate interrupt fla	rresponding Ig bits are
C	ciear prior to enabl	ing an interrupt					

REGISTER 9-7: PIR4: PERIPHERAL INTERRUPT REGISTER 4⁽¹⁾

R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0	U-0	U-0	
TMR5GIF	TMR5IF	_	-	—	—	—	-	
bit 7							bit 0	
Legend:								
R = Readable I	bit	W = Writable I	bit	U = Unimpler	mented bit, read	as '0'		
u = Bit is unchanged x = Bit is unknown				-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set '0' = Bit is cleared HS = Bit is set in hardware								

PIR8: PERIPHERAL INTERRUPT REGISTER 8⁽¹⁾ **REGISTER 9-11:**

bit 7	TMR5GIF: TMR5 Gate Interrupt Flag bit
	1 = Interrupt has occurred (must be cleared by software)
	0 = Interrupt event has not occurred
bit 6	TMR5IF: TMR5 Interrupt Flag bit
	 1 = Interrupt has occurred (must be cleared by software)
	0 = Interrupt event has not occurred
bit 5-0	Unimplemented: Read as '0'

Note 1: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 9-12: PIR9: PERIPHERAL INTERRUPT REGISTER 9⁽¹⁾

U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	-	CLC3IF	CWG3IF	CCP3IF	TMR6IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4	Unimplemented: Read as '0'
bit 3	CLC3IF: CLC3 Interrupt Flag bit
	 1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred
bit 2	CWG3IF: CWG3 Interrupt Flag bit
	1 = Interrupt has occurred (must be cleared by software)0 = Interrupt event has not occurred
bit 1	CCP3IF: CCP3 Interrupt Flag bit
	1 = Interrupt has occurred (must be cleared by software)0 = Interrupt event has not occurred
bit 0	TMR6IF: TMR6 Interrupt Flag bit
	 1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred
Note 1:	Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its correspondition enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are

ing Э clear prior to enabling an interrupt.

R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
CLC1IP	CWG1IP	NCO1IP	_	CCP1IP	TMR2IP	TMR1GIP	TMR1IP
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	oit	U = Unimpler	mented bit, read	l as '0'	
u = Bit is unch	anged	x = Bit is unkn	own	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	CLC1IP: CLC	C1 Interrupt Pric	ority bit				
	1 = High pric 0 = 1 ow pric	prity rity					
hit 6		VG1 Interrunt P	riority hit				
bit o	1 = High price	verintenaperi	lonty bit				
	0 = Low prio	rity					
bit 5	NCO1IP: NC	O1 Interrupt Pri	ority bit				
	1 = High pric	ority					
	0 = Low prio	rity					
bit 4	Unimplemen	nted: Read as ')'				
bit 3	CCP1IP: CC	P1 Interrupt Price	ority bit				
	1 = High price	prity					
	0 = Low prio	rity					
bit 2		R2 Interrupt Pri	ority bit				
	\perp = Hign pric	rity					
hit 1		MR1 Gate Inter	runt Priority hi	ł			
bit i	1 = High price	ority	apti nonty bi				
	0 = Low prio	rity					
bit 0	TMR1IP: TM	R1 Interrupt Pri	ority bit				
	1 = High pric	ority					
	0 = Low prio	rity					

REGISTER 9-29: IPR4: PERIPHERAL INTERRUPT PRIORITY REGISTER 4

				••••			
U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—			BASE<20:16>		
bit 7							bit 0

REGISTER 9-36: IVTBASEU: INTERRUPT VECTOR TABLE BASE ADDRESS UPPER REGISTER

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 Unimplemented: Read as '0'

bit 4-0 BASE<20:16>: Interrupt Vector Table Base Address bits

REGISTER 9-37: IVTBASEH: INTERRUPT VECTOR TABLE BASE ADDRESS HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
BASE<15:8>								
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 BASE<15:8>: Interrupt Vector Table Base Address bits

REGISTER 9-38: IVTBASEL: INTERRUPT VECTOR TABLE BASE ADDRESS LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0
			BASE	<7:0>			
bit 7							bit 0
Legend:							

9		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 BASE<7:0>: Interrupt Vector Table Base Address bits

INTCOM GIE/GIEH GIEL IPPEN T INT INT_EOG INTGEOR INTREE UIRX UIRX UIRX IDAAL DMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UIRX IDAAL IDAAL <thidaal< th=""> <thida< th=""><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Register on Page</th></thida<></thidaal<>	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCOMSTAT+™¬¬ <t< td=""><td>INTCON0</td><td>GIE/GIEH</td><td>GIEL</td><td>IPEN</td><td>-</td><td>-</td><td>INT2EDG</td><td>INT1EDG</td><td>INT0EDG</td><td>135</td></t<>	INTCON0	GIE/GIEH	GIEL	IPEN	-	-	INT2EDG	INT1EDG	INT0EDG	135
Piefor Piefor Piefor CirtikeCKCIE 	INTCON1	STAT	<1:0>	-	-	-	-	-	-	136
PietSMT1PPAMESMT1RECTIEADTEDAIDEZOENINTOREINTOR1448PiezTRRNOEUIESPIITXIESPIITXIEDMAIAREDMAIAREDMAIORIEDMAISORTEIACSITXIE150PiezTRRNOEUIEUIEUITXIEUTRNEUZCIEIZCIENEIZCIENEIZCIENEIZCIENEIZCITXIE150PiesTRRNOEUIZCIEDMAZORDMAZORNEDMAZORNEDMAZORNEDMAZORNEIZCIENEIZCIENEIZCIENEIZCIENE155PiesTMRSOETMRSIEUZIEUZIEUZIEUZIECOP3ECOP3ETMRNE155PiesTTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ECOP3ETMRNE155PiesTOCIFCRCIFSCANFSMTIFCSWFOSFFHUDFSWF133PiesTOCIFCRCIFSCANFSMTIFOTTADDFZCIFNTTOF138PiesTMRSIFSMTIFSMTIFOTTDMAZORFDMAZORFMMADCHMATOF138PiesTOCIFCRCIFSCANFSMTIFSMTIFOTTDMAZORFDMAZORFIMARE141PiesTMRSIF <t< td=""><td>PIE0</td><td>IOCIE</td><td>CRCIE</td><td>SCANIE</td><td>NVMIE</td><td>CSWIE</td><td>OSFIE</td><td>HLVDIE</td><td>SWIE</td><td>147</td></t<>	PIE0	IOCIE	CRCIE	SCANIE	NVMIE	CSWIE	OSFIE	HLVDIE	SWIE	147
PE2I2C1RXIESPI17IESPI17IESPI17XIEDMA1ACDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEMATSONTEM41SONTE149PIE3TURRIEUTIEUTIEUTIRUEUTRUEUTRUEIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIST1PIE4CLC1IECORVIEMA2CREDMA2ORTEDMA2CNTEDMA2CREDMA2CREIMA2EIZC1EIZC1EIZC1EIZC1EIST2PIE5TMR3GETMR3EUZIEUZIECUC2IECWG2IETCCITRAE155PIE6TMR3GETMR3EINT2IECIC2IECWG2IETCCC2IEITMR8E155PIE10TTTTTTCCC2IEKM33EKTRAE155PIE10TCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIFE137PIR1SMTIPMAFSWT1FFSMT1FFSMT1FFDMA1AFDMA1ORIFDMA1ORIFMASCNTF138PIR2IZC1RXIFSMT1FFSW1TIFSWIFTFUZXIFUZXIFIZC1FFIZC1FF141PIR4CLC1FFFMR0FUTIFFSWIFTFUXXIFFUXXIFFUXXIFF12C1FF141PIR4IZC1FFITM81FNT1FFSWIFTFUXXIFFUXXIFFUXXIFF12C1FF12C1FF141PIR4CLC1FFOWG1FNCAC	PIE1	SMT1PWAIE	SMT1PRAIE	SMT1IE	C1IE	ADTIE	ADIE	ZCDIE	INT0IE	148
PE3TMR0IEU11EU1EIEU1TXIEU17XIEU12CIEE12C1EIE12C1EIE12C1EIE12C1TXIE150PIE4ICC2TXIEICC2TIF	PIE2	I2C1RXIE	SPI1IE	SPI1TXIE	SPI1RXIE	DMA1AIE	DMA10RIE	DMA1DCNTIE	DMA1SCNTIE	149
PE4CLC1IECWG1IENC01IETCCP1IETMR2IETMR2IETMR1GIETMR1IE151PIE6IZCZTXIEIZCZTXIEIZCZRXIEDMAZANEDMAZORIEDMAZORIEDMAZORIEDMAZORIEDMAZORIEIZCZIEINT1IE152PIE6TMR3GIETMR3IEUZIEUZIEUZIEUZIEUZIEIZCZIETMR4IE155PIE7TTIITIZIECLC2IECWG2IECP3IETMR4IE155PIE8TTTITTCLC3IECWG3IECP3IETMR6IE156PIE70TTTTCLC3IECWG3IECD3IETMR6IE156PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF133PIR11SMT1PRAIFSMT1FAIFSPITIAIFSPITIAIFSPITIAIFDMA1AIFDMA1ORIFDMATOCTIFDMATOCTIF141PIR3IICIFCLC1IFCWG1IFNC01IFITTCCP1IFTMR2IFTMR1GIF141PIR4CLC1IFCWG3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIF142PIR4TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFTMR1GIF141PIR5IZC2TXFIZC2RXFDMA2AFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFCI2IFITMR3IF141PIR6TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIFI	PIE3	TMR0IE	U1IE	U1EIE	U1TXIE	U1RXIE	I2C1EIE	I2C1IE	I2C1TXIE	150
PIESI2C2TXIEI2C2RXIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDVA20EC2IEINTIE152PIEGTMTMITMR3IEUZIEUZIEUZIKIEUZRIEIZC2ELEIZC2ELEIZC2ELEIS3PIE7TTITMR3IEINTIECLC2IECWG2IETCC2PIETMR4IE155PIE3TTTTCLC3IECWG3IECC2IETMR4IE155PIE10TTTTTCLC3IECWG3IECC2IETMR4IE155PIR10NOCIFCRCIFSCANIFNVMIFCSUFOSFFHLVDIFSWITIF137PIR1SMT1PMAIFSMT1FSPITAIFSPITAFADIFADIFZCDIFINTOIF138PIR2I2C1RXIFSPITAFSPITAFSPITAFDMA10FFDMA10CNFDMA10CNTFDMA10CNTF140PIR3TMR0FU1FU1FFUTTIFUTR1FUTR1FTMR1GFIMT1F141PIR5I2C2TXF10/2CXFDMA2AFDMA2AFFDMA2CNTFDMA2SCNTFCC2FFINT1F142PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2TKFI2C1TXF144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT4F144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT6F145PIR7	PIE4	CLC1IE	CWG1IE	NCO1IE	—	CCP1IE	TMR2IE	TMR1GIE	TMR1IE	151
PIEGTMR3GIETMR3IEU2IEU2IEIU2IEIEU2IXIEU2RXIEI2C2IEII12C2IE1533PIE7CC22IETMR4IE1544PIE8TMR5IETMR5IECC22IETMR6IE1555PIE9CLC3IECWG3IECCP3IETMR6IE1556PIE10CLC3IECWG3IECCP3IETMR6IE1556PIR0IOCIFCRCIFSCANIFN/MIFCSWIFOSFIFHIVDIFSWIF1377PIR1SMT1PWAIFSMT1PRAIFSMT1IFC11FAD1FAD1FZCDIFINTOF138PIR2I2C17XIFSP11FXSP11FXIFSP11FXIFDMA1AIFDMA1CRIFDMA1CRIFDMA1CRIFIMACRIFIMACRIF1411PIR3TMR0IFU11FU11EIFU11XIFU1RXIFIZC1FIFIZC1FIFIZC1TXIF1420PIR4CLC1IFCWG1IFNC01IFCCP1IFTMR2IFTMR1GFTMR1IF1442PIR3ITM2FIDM2FDMA2CRIFDMA2CNTIFDMA2SCNTIFIZC2IFIZC1TXIF1420PIR4CLC1IFCWG1IFU2IFU2IFU2IFU2IFU2IFIZC1TXIF1441PIR5ITM2FIDM2FCLC2IFCWG2IFCCP2IFTMR1IF1442PIR6ITM2FITM2FU2IFU2IFU2IFU2IFIZC1FIFIZC1FFIZC	PIE5	I2C2TXIE	I2C2RXIE	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	C2IE	INT1IE	152
PIE7INT2IECLC2IECWG2IECCP2IETMR4IE154PIE8TMR5IETMR5IE155PIE9155PIE9CLC3IECWG3IECCP3IETMR6IE155PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF137PIR1SMT1PWAFSMT1PAFAFSMT1FCHFADTFADFZCDIFINTOIF138PIR2ICC1FCRCIFSCANIFOTHADM1AIFDMA1ORIFDMAIONIFDMAISCNTF139PIR3TMR0IFU11FU11FU11FU11FU11FU11F141141PIR4CLC1FCWG1FNC01F-CCP1IFTMR2IFTMR6IFTMR1F141PIR512C2TXF12C3TXFDMA2AFDMA2ORIFDMA2CNTFDMA2SCNTFC2FINT1F142PIR6TMR3GFTMR3FU2FU2FU2TKFU2RXF12C2EF12C2IF143PIR7T145PIR8TMR3GFTMR3FV2FU2FU2TKFU2RXF12C2FF12C2IF144PIR9TMR3GFTMR3FSMT1PO145PIR10<	PIE6	TMR3GIE	TMR3IE	U2IE	U2EIE	U2TXIE	U2RXIE	I2C2EIE	I2C2IE	153
PIE8TIMRSGIETIMRSIE111 <td>PIE7</td> <td>_</td> <td>-</td> <td>INT2IE</td> <td>CLC2IE</td> <td>CWG2IE</td> <td>-</td> <td>CCP2IE</td> <td>TMR4IE</td> <td>154</td>	PIE7	_	-	INT2IE	CLC2IE	CWG2IE	-	CCP2IE	TMR4IE	154
PIE9 CLC3IE CWG3IE CCP3IE TMR6IE 155 PIE10 CLC3IE CCP3IE TMR6IE 155 PIR0 IOCIF CRCIF SCANIF IC CLC4IE CCP4IE 156 PIR0 SMT1PAUR SMT1PAUR SCANIF CIF ADTIF ADDIF ADDIF ADDIF MA10CNIF DMA1SCNTF 138 PIR2 12C1RXIF SP1IIF SP1ITXIF SP1IXIF DMA1AIF DMA1ORIF DMA1SCNTF 139 PIR3 TMR0IF U11F U1EIF U1XIF U1XIF U2RUF 12C21F 12C21F 12C21F 12C21F 141 PIR3 TMR3GIF TMR3IF CLC3IF CW31F CMA2CNTF DMA2CNTF DMA2CNTF CL2IF 141 PIR4 CLC1F TMR3IF TMR3IF TMR3IF TMR3IF TMR3IF 145 PIR7	PIE8	TMR5GIE	TMR5IE	-	—	-	—	—	—	155
PHE10 — — — — — CLC4HE CCP4HE 156 PIR0 IOCIF CRCH SCAMIF NVMIF CSWIF OSFIF HLVDIF SWITF 137 PIR1 SMT1PWAHF SMT1PRAF SMT1H C1IF ADTIF ADIF ZCDIF INTOIF 138 PIR2 IZC1RXIF SP114F SMT1VF DMA1ALF DMA1ALF DMA1ALF DMA1ALF DMA1ALF DMA1ALF IMATISCHTF 139 PIR3 TMR0IF U1IF U1EF UTXIF DMA2ACTF DMA2ACTF IMATISCHTF 12C1TKIF 12C1TKIF 141 PIR3 TMR3GIF TMR3F DM2ACFF DMA2ACTFF DMA2SCNTF C2EIF INTHF 141 PIR4 CLC1IF CWG1FF TMR3F TMR3FF C1C2IF CWG2FF CCP2IF TMRAFF 144 PIR4 TMR5GIF TMR3FF TMR3FF C1C2IF CWG3FF CCP3IF TMRAFF 145 <td< td=""><td>PIE9</td><td>_</td><td>-</td><td>-</td><td>—</td><td>CLC3IE</td><td>CWG3IE</td><td>CCP3IE</td><td>TMR6IE</td><td>155</td></td<>	PIE9	_	-	-	—	CLC3IE	CWG3IE	CCP3IE	TMR6IE	155
PIRO IOCIF CRCIF SCANIF NVMIF CSWIF OSFIF HLVDIF SWIF 137 PIR1 SMT1PWAIF SMT1PRAIF SMT1IF C1IF ADTF ADIF ZCIR INTOIF 138 PIR2 IZCIRXIF SPI1IF SPI1IF SPI1IF SPI1IF SPI1IF DMAISCITF DMAISCITF DMAISCITF 139 PIR3 TMR0IF UUIF UITXIF DMAISCITF DMAISCITF DMAISCITF 140 PIR4 CLCIFF CWGIFF NCOIFF CCP1F TMR3IFF TMR1F 141 PIR5 12C2TXF 12C2RXF DMA2AIF DMA2ORIF DMA2SCITF DMA2SCITF C2IF INT1F 142 PIR6 TMR3GIF TMR3F U2IF U2EIF U2TXIF U2RXIF 12C2IFF TMR1F 144 PIR6 TMR3GIF TMR3F U2IF C2IF CCP3IF TMR6IF 145 PIR9 - - - - - <td>PIE10</td> <td>_</td> <td>_</td> <td>-</td> <td>—</td> <td>-</td> <td>-</td> <td>CLC4IE</td> <td>CCP4IE</td> <td>156</td>	PIE10	_	_	-	—	-	-	CLC4IE	CCP4IE	156
PIR1 SMT1PWAIF SMT1IPRAIF SMT1IF C1IF ADIF ADIF ZCDIF INTOIF 138 PIR2 I2C1RXIF SP11IF SP11TXIF SP11XIF DMA1AIF DMA1ORIF DMA1DCNTIF DMA1SCNTF 139 PIR3 TMR0IF U1F U1EF U1TXIF URXIF I2C1EF I2C1F I2C1F I2C1F I2C1F IANT1F 141 PIR4 CLC1IF CWG1IF NC0IF — CCP1IF TMR1F IATT1F 142 PIR5 I2C2TXF I2C2RXF DMA2AIF DMA2ORIF DMA2SCNTF U2Z1F IXT1F 142 PIR6 TMR3GIF TMR3IF U2IF U2Z1F U2RXIF U2C2EIF TMR4IF 144 PIR6 TMR5GIF TMR3IF TMR1F U2IF CLC3IF CWG3IF CCP3IF TMR4IF 144 PIR7 — — — — — — 145 PIR8 TMR5GIF TMR5IF <	PIR0	IOCIF	CRCIF	SCANIF	NVMIF	CSWIF	OSFIF	HLVDIF	SWIF	137
PIR2 IZC1RXIF SPI1T SPI1TXIF SPI1TXIF DMA1AIF DMA1ORIF DMA1DCNTIF DMA1SCNTIF 139 PIR3 TMR0IF U1IF U1EIF U1TXIF U1RXIF I2C1EIF I2C1IF I2C1TXIF 140 PIR4 CLC1IF CWG1IF NC01F — CCP1F TMR2IF TMR3IF TMR1F 141 PIR6 TMR3GIF TMR3IF U2EF DMA2CIFF DMA2SCNTF C2IF INT1F 142 PIR6 TMR3GIF TMR3IF U2E U2EIF U2RXIF U2RXIF IZC2IF TMR4F 144 PIR7 — — INT2F CLC2IF CWG3IF CCP3IF TMR4F 144 PIR8 TMR5GIF TMR5IF — — — CCP3IF TMR6F 145 PIR9 — — — — CLC3IF CWG3IF CCP3IF TMR6F 145 PIR10 — CCIP SCANP NVMIP	PIR1	SMT1PWAIF	SMT1PRAIF	SMT1IF	C1IF	ADTIF	ADIF	ZCDIF	INT0IF	138
PIR3 TMR0IF U1IF U1EIF U1TXIF U1RXIF I2C1EIF I2C1IF I2C1TXIF 140 PIR4 CLC1IF CWG1IF NCO1IF — CCP1IF TMR2IF TMR1GIF TMR1IF 141 PIR5 I2C2TXF I2C2RXF DMA2AF DMA2ORIF DMA2SCNTIF C2F INT1GF 142 PIR6 TMR3GIF TMR3IF U2IF U2EIF U2TXIF U2RXIF I2C2EF I2C2IF 143 PIR7 — — ITMR3GIF TMR3IF — — — — — 145 PIR8 TMRSGIF TMRSIF — — — — — 145 PIR9 — — — — — — — 145 PIR10 — — — — CLC3IF CWG3IF CCP3IF TMR6IF 145 PIR10 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMT1PRAIP SMT1PRAIP S	PIR2	I2C1RXIF	SPI1IF	SPI1TXIF	SPI1RXIF	DMA1AIF	DMA10RIF	DMA1DCNTIF	DMA1SCNTIF	139
PIR4 CLC1IF CWG1IF NC01IF T CCP1IF TMR2IF TMR1GIF TMR1IF 141 PIR5 I2C2TXF I2C2RXF DMA2AIF DMA2ORIF DMA2CNTIF DMA2SCNTIF C2IF INT1IF 142 PIR6 TMR3GIF TMR3IF U2IF U2TXIF U2RXIF I2C2EIF I2C2IF 143 PIR7 - - - CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF - - - - - - 145 PIR9 - - - - - - - 145 PIR9 - - - - - - - - 145 PIR10 - - - - - CLC3IF CWG3IF CLC3IF KWR3IF K146 IPR0 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 156 <td>PIR3</td> <td>TMR0IF</td> <td>U1IF</td> <td>U1EIF</td> <td>U1TXIF</td> <td>U1RXIF</td> <td>I2C1EIF</td> <td>I2C1IF</td> <td>I2C1TXIF</td> <td>140</td>	PIR3	TMR0IF	U1IF	U1EIF	U1TXIF	U1RXIF	I2C1EIF	I2C1IF	I2C1TXIF	140
PIRSI2C2TXFI2C2RXFDMA2AIFDMA2ORIFDMA2DCNTIFDMA2DCNTIFDMA2SCNTIFC2IFINT1IF142PIR6TMR3GIFTMR3IFU2IFU2EIFU2TXIFU2RXIFI2C2EIFI2C2IF143PIR7———INT2IFCLC2IFCWG2IF—CCP2IFTMR4IF144PIR8TMR5GIFTMR5IF——————145PIR9————————145PIR10————————145PIR10IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PMAPSMT1PANIPSMT1IPC1IPADIPADIPZCDIPINA1SCNTIP158IPR2I2C1RPSPI1IPSPI1IPSPI1RIPDMA1AIPDMA1ORIPDMA1DCNTPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG3IPNCO1IPMA2ORIPDMA2SCNTIPDMA1SCNTIP162IPR5I2C2TXPI2C2TXPDMA2AIPDMA2ORIPDMA2SCNTIPDMA1SCNTIP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP166 <td>PIR4</td> <td>CLC1IF</td> <td>CWG1IF</td> <td>NCO1IF</td> <td>—</td> <td>CCP1IF</td> <td>TMR2IF</td> <td>TMR1GIF</td> <td>TMR1IF</td> <td>141</td>	PIR4	CLC1IF	CWG1IF	NCO1IF	—	CCP1IF	TMR2IF	TMR1GIF	TMR1IF	141
PIR6 TMR3GIF TMR3IF U2IF U2EIF U2TXIF U2CXIF I2C2EIF I2C2IF 143 PIR7 — — INT2IF CLC2IF CWG2IF — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — — — 145 PIR9 — — — — — — — — 145 PIR0 — — — — — — — 145 PIR0 — — — — — — CLC3IF CM31F CCP3IF TMR6IF 145 PIR10 — CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMT1PWAIP SMT1P SMT1P MIP IMA10P IMA10CN	PIR5	I2C2TXF	I2C2RXF	DMA2AIF	DMA2ORIF	DMA2DCNTIF	DMA2SCNTIF	C2IF	INT1IF	142
PIR7 — INT2IF CLC2IF CWG2IF — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — — — 145 PIR9 — — — — — — — 145 PIR9 — — — — — — — 145 PIR0 — — — — — — — — 145 PIR0 — — — — — — — — 145 PIR10 — — — — — CLC3IF CWG3IF CCP3IF TMR6IF 145 IPR0 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMTPWAIP SMT1PAIP SMT1PAIP SMT1PAIP DMA1AIP DMA1DCNIP DMA1SCNTP DMA1SCNTP IDA1SCNTP	PIR6	TMR3GIF	TMR3IF	U2IF	U2EIF	U2TXIF	U2RXIF	I2C2EIF	I2C2IF	143
PIR8TMR5GIFTMR5IF——————145PIR9————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10—————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10———————CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1IPC1IPADTPADIPZCDIPINT0IP158IPR2I2C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA10CNTIPDMA1SCNTIP159IPR3TMR0IPU11PU1EIPU1TXIPU1RXIPI2C1EIP12C1IP12C1TXIP160IPR4CLC1IPCWG1IPNCO1IP—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7——————————164IPR8TMR5GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIP12C1P164IPR8TMR5GIPTMS1P———————16	PIR7	-	-	INT2IF	CLC2IF	CWG2IF	—	CCP2IF	TMR4IF	144
PIR9CLC3IFCWG3IFCCP3IFTMR6IF145PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSM11PC1IPADTIPADIPZCDIPINT0IP158IPR212C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIP12C1EIP12C1IP12C1TXIP160IPR4CLC1PCWG1IPNC01IP-CCP1IPTMR2IPTMR1GIPTMR1IP161IPR512C2TXP12C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIP12C2EIP12C2IP163IPR7164IPR8TMR5GIPTMR5IP164IPR9165IPR10166NTBASEU166NTBASEU166NTBASEL167NTBASEL-<	PIR8	TMR5GIF	TMR5IF	-	—	-	—	—	—	145
PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSP11IPSP11IPSP1RIPDMA1AIPDMA1ORIPDMA1DCNTPDMA1SCNTP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1IPCCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7164IPR8TMR5GIPTMR3IP164IPR8TMR5GIPTMR5IP165IPR10166IVTBASEU166IVTBASEL167IVTADU167IVTADL167IVTADL167IVTADL<	PIR9	-	-	-	—	CLC3IF	CWG3IF	CCP3IF	TMR6IF	145
IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSPI1IPSPI1TIPSPI1RIPDMA1AIPDMA1ORPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1P—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7IMTSIPCLC2IPCWG2IP-CCP3IPTMR4IP164IPR8TMRSGIPTMRSIP164IPR8TMRSGIPTMRSIP166IPR10166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IFR8TMRSGIP	PIR10	_	-	-	—	-	—	CLC4IF	CCP4IF	146
IPR1 SMT1PWAIP SMT1PRAIP SMT1IP C1IP ADTIP ADIP ZCDIP INTOIP 158 IPR2 I2C1RIP SPI1IP SPI1TIP SPI1RIP DMA1AIP DMA1ORIP DMA1DCNTIP DMA1SCNTIP 159 IPR3 TMR0IP U1IP U1EIP U1TXIP U1RXIP I2C1EIP I2C1IP I2C1TXIP 160 IPR4 CLC1IP CWG1IP NC01IP — CCCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR4 CLC1IP CWG1IP NC01IP — CCCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR5 I2C2TXP I2C2RXP DMA2AIP DMA2ORIP DMA2CNTIP DMA2SCNTIP C2IP INT1IP 162 IPR6 TMR3GIP TMR3IP U2IP U2EIP U2TXIP U2RXIP I2C2EIP I2C2IP 163 IPR6 TMR5GIP TMR3IP — — — CC2G3IP TMR4IP 164 IPR9	IPR0	IOCIP	CRCIP	SCANIP	NVMIP	CSWIP	OSFIP	HLVDIP	SWIP	157
IPR2 I2C1RIP SPI1IP SPI1RIP DMA1AIP DMA1ORIP DMA1DCNTP DMA1SCNTIP 159 IPR3 TMR0IP U1IP U1EIP U1TXIP U1RXIP I2C1EIP I2C1IP I2C1TXIP 160 IPR4 CLC1IP CWG1IP NCO1IP — CCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR4 I2C2TXP I2C2RXP DMA2AIP DMA2ORIP DMA2DCNTIP DM2SCNTIP C2IP INT1IP 162 IPR6 TMR3GIP TMR3IP U2IP U2EIP U2TXIP U2RXIP I2C2EIP I2C2IP 163 IPR7 — — INT2IP CLC2IP CWG2IP — CCP2IP TMR4IP 164 IPR8 TMR5GIP TMR5IP — — — — — 164 IPR9 — — — — CC3IP CWG3IP CCP3IP TMR6IP 165 IPR10 — — — —<	IPR1	SMT1PWAIP	SMT1PRAIP	SMT1IP	C1IP	ADTIP	ADIP	ZCDIP	INT0IP	158
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR2	I2C1RIP	SPI1IP	SPI1TIP	SPI1RIP	DMA1AIP	DMA10RIP	DMA1DCNTIP	DMA1SCNTIP	159
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	IPR3	TMR0IP	U1IP	U1EIP	U1TXIP	U1RXIP	I2C1EIP	I2C1IP	I2C1TXIP	160
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR4	CLC1IP	CWG1IP	NCO1IP	—	CCP1IP	TMR2IP	TMR1GIP	TMR1IP	161
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR5	I2C2TXP	I2C2RXP	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	C2IP	INT1IP	162
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR6	TMR3GIP	TMR3IP	U2IP	U2EIP	U2TXIP	U2RXIP	I2C2EIP	I2C2IP	163
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR7	-	-	INT2IP	CLC2IP	CWG2IP	—	CCP2IP	TMR4IP	164
IPR9 - - - CLC3IP CWG3IP CCP3IP TMR6IP 165 IPR10 - - - - - CLC3IP CCP3IP TMR6IP 165 IPR10 - - - - - CLC4IP CCP4IP 165 IVTBASEU - - - - BASE<20:16> 166 IVTBASEL - - BASE<15:8> 166 165 IVTBASEL - - BASE<7:0> 166 167 IVTADU Image: Comparison of the c	IPR8	TMR5GIP	TMR5IP	-	—	-	—	—	—	164
IPR10 - - - - CCP4IP 165 IVTBASEU - - - - - 166 IVTBASEH - - - BASE<15:8> 166 IVTBASEL BASE<15:8> 166 IVTBASEL BASE<7:0> 166 IVTADU Image: Comparison of the temperature of temper	IPR9	-	-	-	—	CLC3IP	CWG3IP	CCP3IP	TMR6IP	165
IVTBASEU — — — BASE BASE 166 IVTBASEH BASE<15:8> 166 166 IVTBASEL BASE<7:0> 166 IVTADU Image: Comparison of the system of the sys	IPR10	_	_	_	-	_	-	CLC4IP	CCP4IP	165
IVTBASEH BASE<15:8> 166 IVTBASEL BASE<7:0> 166 IVTADU AD 167 IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTBASEU	_	_	-			BASE<20:16>			166
IVTBASEL BASE<7:0> 166 IVTADU AD AD 167 IVTADH AD AD 167 IVTADL AD AD<7:0> 167	IVTBASEH	BASE<15:8>							166	
IVTADU AD AD 167 IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTBASEL				BAS	SE<7:0>				166
IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTADU						AD<20:16>			167
IVTADL AD<7:0> 167	IVTADH				AD	<15:8>				167
	IVTADL				AE)<7:0>				167
IVTLOCK — — — — — — — IVTLOCKED 168	IVTLOCK	—	—	—	—	_	—	—	IVTLOCKED	168

TABLE 9-3:	SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for interrupts.

13.3 Data EEPROM Memory

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, which is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Five SFRs are used to read and write to the data EEPROM as well as the program memory. They are:

- NVMCON1
- NVMCON2
- NVMDAT
- NVMADRL
- NVMADRH⁽¹⁾

Note 1: NVMADRH register is not implemented on PIC18(L)F45/55K42.

The data EEPROM allows byte read and write. When interfacing to the data memory block, NVMDAT holds the 8-bit data for read/write and the NVMADRH:NVMADRL register pair holds the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an internal programming timer; it will vary with voltage and temperature as well as from chip-to-chip. Refer to the Data EEPROM Memory parameters in Section 44.0 "Electrical Specifications" for limits.

13.3.1 NVMADRL AND NVMADRH REGISTERS

The NVMADRH:NVMADRL registers are used to address the data EEPROM for read and write operations.

13.3.2 NVMCON1 AND NVMCON2 REGISTERS

Access to the data EEPROM is controlled by two registers: NVMCON1 and NVMCON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The NVMCON1 register (Register 13-1) is the control register for data and program memory access. Control bits REG<1:0> determine if the access will be to program, Data EEPROM Memory or the User IDs, Configuration bits, Revision ID and Device ID.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

The WRERR bit is set by hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

The WR control bit initiates write operations. The bit can be set but not cleared by software. It is cleared only by hardware at the completion of the write operation.

The NVMIF Interrupt Flag bit of the PIR0 register is set when the write is complete. It must be cleared by software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (REG<1:0> = 0x10). Program memory is read using table read instructions. See Section 13.1.1 "Table Reads and Table Writes" regarding table reads.





REGISTER 25-13: SMT1CPWL: SMT CAPTURED PULSE WIDTH REGISTER – LOW BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x
			SMT1C	PW<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	1 as '0'	
u = Bit is unch	- Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all oth					other Resets	

bit 7-0 SMT1CPW<7:0>: Significant bits of the SMT PW Latch – Low Byte

'0' = Bit is cleared

'1' = Bit is set

'1' = Bit is set

REGISTER 25-14: SMT1CPWH: SMT CAPTURED PULSE WIDTH REGISTER - HIGH BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	
			SMT1CF	PW<15:8>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, read	1 as '0'		
u = Bit is unchanged x = Bit is unknown			nown	-n/n = Value at POR and BOR/Value at all other Resets				

bit 7-0 SMT1CPW<15:8>: Significant bits of the SMT PW Latch – High Byte

'0' = Bit is cleared

REGISTER 25-15: SMT1CPWU: SMT CAPTURED PULSE WIDTH REGISTER – UPPER BYTE

R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	R-x/x	
SMT1CPW<23:16>								
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 SMT1CPW<23:16>: Significant bits of the SMT PW Latch – Upper Byte

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REGISTER 25-16: SMT1PRL: SMT PERIOD REGISTER – LOW BYTE

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	
			SMT1F	PR<7:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	d as '0'		
u = Bit is unchanged x = Bit is unknown				-n/n = Value at POR and BOR/Value at all other Resets				

bit 7-0 SMT1PR<7:0>: Significant bits of the SMT Timer Value for Period Match – Low Byte

REGISTER 25-17: SMT1PRH: SMT PERIOD REGISTER – HIGH BYTE

'0' = Bit is cleared

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	
SMT1PR<15:8>								
bit 7							bit 0	
Legend:								

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 SMT1PR<15:8>: Significant bits of the SMT Timer Value for Period Match – High Byte

REGISTER 25-18: SMT1PRU: SMT PERIOD REGISTER – UPPER BYTE

R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	R/W-x/1	
SMT1PR<23:16>								
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 SMT1PR<23:16>: Significant bits of the SMT Timer Value for Period Match – Upper Byte

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'1' = Bit is set

IORWF Inclusive OR W with f							
Synta	ax:	IORWF	f {,d {,a}}				
Oper	ands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$					
Oper	ation:	(W) .OR. (f	$\rightarrow dest$				
Statu	is Affected:	N, Z					
Enco	oding:	0001	00da	ffff	ffff		
Desc	rription:	Inclusive C '0', the result is (default). If 'a' is '0', ' If 'a' is '1', ' GPR bank. If 'a' is '0' a set is enab in Indexed mode when tion 41.2.3 Oriented I eral Offset	Inclusive OR W with register 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '0', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Sec- tion 41.2.3 "Byte-Oriented and Bit- Oriented Instructions in Indexed Lit- oren Offset Mode" for details				
Word	ls:	1					
Cycle	es:	1					
QC	ycle Activity:						
	Q1	Q2	Q3		Q4		
	Decode	Read register 'f'	Proce Dat	ess V a de	Write to estination		
Exan	nple:	IORWF R	ESULT,	0, 1			

Syntax:LFSR f, kOperands: $0 \le f \le 2$ $0 \le k \le 16383$ Operation: $k \rightarrow FSRf$ Status Affected:NoneEncoding: 1110 1111 $00k_{13}k$ k_7kkk $kkkk$ $kkkk$ Description:The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.Words:2 Q Cycle Activity:Q1Q2 MSB Q3 MSB Q4Process $FSRfH$ DecodeRead literal $K' MSB$ ProcessWrite $K'RSH$ DecodeRead literal $K' MSB$ ProcessWrite $K'RSH$ DecodeRead literal $K' MSB$ ProcessWrite $K'RSH$ Q2Q3 $K' MSB$	LFS	R	Load FS	R					
$\begin{array}{cccccccc} \mbox{Operands:} & 0 \leq f \leq 2 \\ & 0 \leq k \leq 16383 \end{array} \\ \mbox{Operation:} & k \rightarrow FSRf \\ \mbox{Status Affected:} & None \\ \mbox{Encoding:} & \hline 1110 & 1110 & 00k_{13}k & kkkk \\ & 1111 & 0000 & k_7kkk & kkkk \\ \mbox{Description:} & The 14-bit literal 'k' is loaded into the \\ & File Select Register pointed to by 'f'. \\ \mbox{Words:} & 2 \\ \mbox{Cycles:} & 2 \\ \mbox{Q Cycle Activity:} & \hline \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Synta	ax:	LFSR f, k						
Operation: $k \rightarrow FSRf$ Status Affected:NoneEncoding: 1110 1110 $00k_{13}k$ $kkkk$ Description:The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.Words:2Cycles:2Q Cycle Activity:Q1Q2Q3Q4DecodeRead literal 'k' MSBProcessWrite literal 'k' MSB to FSRfHDecodeRead literalProcessWrite literal 'k' MSB to FSRfH	Oper	ands:	$\begin{array}{l} 0 \leq f \leq 2 \\ 0 \leq k \leq 163 \end{array}$	383					
Status Affected: None Encoding: 1110 1110 00k13k kkkk Description: The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'. Words: 2 Cycles: 2 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write literal 'k' MSB to FSRfH Decode Read literal Process Write literal	Oper	ation:	$k \to FSRf$						
Encoding: 1110 1110 00k13k kkkk 1111 0000 k7kkk kkkk Description: The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'. Words: 2 Cycles: 2 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write literal 'k' MSB Data SB to FSRfH Decode Read literal Process Write literal 'k'	Statu	s Affected:	None						
Description: The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'. Words: 2 Cycles: 2 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write iteral 'k' MSB Data literal 'k' MSB to FSRfH Decode Read literal Process Write literal	Encoding:		1110 1111	1110 0000	00k ₁₃ k k ₇ kkk	kkkk kkkk			
Words: 2 Cycles: 2 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write 'k' MSB Data literal 'k' MSB to FSRfH Decode Read literal Process Write literal	Description:		The 14-bit File Select	The 14-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.					
Cycles: 2 Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write 'k' MSB Data literal 'k' MSB to FSRfH Decode Read literal Process Write literal	Word	ls:	2	2					
Q Cycle Activity: Q1 Q2 Q3 Q4 Decode Read literal Process Write 'k' MSB Data literal 'k' MSB to FSRfH Decode Read literal Process Write literal	Cycles:		2	2					
Q1 Q2 Q3 Q4 Decode Read literal 'k' MSB Process Data Write literal 'k' MSB to FSRfH Decode Read literal Process Write literal	QC	ycle Activity:							
Decode Read literal 'k' MSB Process Data Write literal 'k' MSB to FSRfH Decode Read literal Process Write literal		Q1	Q2	Q3		Q4			
Decode Read literal Process Write literal		Decode	Read literal 'k' MSB	Proce Data	ess a lin N	Write teral 'k' ⁄ISB to FSRfH			
'k' LSB Data 'k' to FSRfL		Decode	Read literal 'k' LSB	Proce Data	ess Wr a 'k'	ite literal to FSRfL			

Example: LFSR 2, 3ABh

•		
After Instruction		
FSR2H	=	03h
FSR2L	=	ABh

Examp	le

Before Instruction								
RESULT	=	13h						
W	=	91h						
After Instructio	n							
RESULT	=	13h						
W	=	93h						

POP	Рор Тор о	f Return Sta	ack	PUS	н	Push Top	of Retur	n Stac	k
Syntax:	POP			Synta	ax:	PUSH			
Operands:	None			Oper	ands:	None			
Operation:	$(TOS) \rightarrow bit$	bucket		Oper	ation:	$(\text{PC + 2}) \rightarrow$	TOS		
Status Affected:	None			Statu	s Affected:	None			
Encoding:	0000	0000 000	00 0110	Enco	ding:	0000	0000	0000	0101
Description:	The TOS va stack and is then become was pushed This instruct the user to p stack to incc	lue is pulled c discarded. Th es the previou onto the retui ion is provide properly mana prporate a soft	off the return ne TOS value is value that rn stack. d to enable ige the return tware stack.	Desc Word	ription: Is:	The PC + 2 the return st value is pus This instruc software sta then pushin 1	is pushed tack. The p shed down tion allows ack by mod g it onto th	onto the previous on the s implem lifying T e return	e top of TOS stack. enting a OS and stack.
Words:	1			Cycle	es:	1			
Cycles:	1			QC	vcle Activity:				
Q Cycle Activity	:				Q1	Q2	Q3		Q4
Q1 Decode	Q2 No operation	Q3 POP TOS value	Q4 No operation		Decode	PUSH PC + 2 onto return stack	No operatio	n oj	No peration
Example:	POP GOTO	NEW		Exan	<u>iple</u> : Before Instru	PUSH			
Before Instr TOS Stack (uction (1 level down)	= 0031A = 014332	2h 2h		TOS PC		= 345 = 012	5Ah 24h	
After Instruc TOS PC	ction	= 014332 = NEW	2h		After Instructi PC TOS Stack (1	on level down)	= 012 = 012 = 345	26h 26h 5Ah	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page	
3CE6h	CLKRCON	EN	_	—	C	C		113			
3CE5h	CLKRCLK	—	_	_	_		(114			
3CE4h - 3C7Fh	—	Unimplemented									
3C7Eh	CLCDATA0	—	—	—	—	CLC4OUT	CLC3OUT	CLC2OUT	CLC1OUT	447	
3C7Dh	CLC1GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	446	
3C7Ch	CLC1GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	445	
3C7Bh	CLC1GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	444	
3C7Ah	CLC1GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	443	
3C79h	CLC1SEL3				D	4S				442	
3C78h	CLC1SEL2				D	3S				442	
3C77h	CLC1SEL1				D	2S				442	
3C76h	CLC1SEL0				D	1S				442	
3C75h	CLC1POL	POL	_	_	_	G4POL	G3POL	G2POL	G1POL	441	
3C74h	CLC1CON	EN	OE	OUT	INTP	INTN		MODE		440	
3C73h	CLC2GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	446	
3C72h	CLC2GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	445	
3C71h	CLC2GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	444	
3C70h	CLC2GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	443	
3C6Fh	CLC2SEL3		D4S								
3C6Eh	CLC2SEL2				D	35				442	
3C6Dh	CLC2SEL1				D	28				442	
3C6Ch	CLC2SEL0	201			D	15	00001	00000	0.45.01	442	
3C6Bh		POL	-	-	-	G4POL	G3POL	G2POL	GIPOL	441	
3C6An	CLC2CON	EN	UE CADAN	001			04000	MODE	O 4 D 4 N	440	
3C69h	CLC3GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D21	G4D2N	G4D11	G4D1N G2D1N	440	
300011		G3D4T	G3D4N	GSDST	GODON	GSD2T	GODON	G3D11	G3D1N	440	
300711 2066b		G2D4T	G2D4N	G2D3T	G2D3N C1D2N	G2D2T	GZDZN C1D2N	G2D11	G2D1N	444	
3C65h		GID41	GID4N	GID31	GIDSN		GIDZN	GIDTI	GIDIN	442	
3C64h					D'	+0 39				442	
3C63h	CLC3SEL1				D:	25				442	
3C62h	CLC3SEL0					15				443	
3C61h		POI	_	_	_	G4POI	G3POI	G2POI	G1POI	441	
3C60h	CLC3CON	EN	OE	OUT	INTP		00.02	MODE	0.1.02	440	
3C5Fh	CLC4GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	446	
3C5Eh	CLC4GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	445	
3C5Dh	CLC4GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	444	
3C5Ch	CLC4GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	443	
3C5Bh	CLC4SEL3				D4	4S				442	
3C5Ah	CLC4SEL2				D	3S				442	
3C59h	CLC4SEL1				D	2S				442	
3C58h	CLC4SEL0				D	1S				443	
3C57h	CLC4POL	POL		_	_	G4POL	G3POL	G2POL	G1POL	441	
3C56h	CLC4CON	EN	OE	OUT	INTP	INTN		MODE		440	
3C55h - 3C00h	—			·	Unimple	emented					
3BFFh	DMA1SIRQ	_				SIRQ				256	
Legend:	x = unknown. u	u = unchanged.	— = unimpleme	nted, a = value	e depends on o	condition					

TABLE 42-1: REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Note

1: Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

Unimplemented on PIC18(L)F26/27/45/46/47K42 devices. 3:

Unimplemented in PIC18(L)F45/55K42. 4:

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
39DAh	OSCCON2	—		COSC			105			
39D9h	OSCCON1	—		NOSC		NDIV				104
39D8h	CPUDOZE	IDLEN	DOZEN	ROI	DOE	—		177		
39D7h - 39D2h	—	Unimplemented								
39D1h	VREGCON ⁽¹⁾	—	—	—	—	—	—	VREGPM	—	176
39D0h	BORCON	SBOREN	—	—	—	_	—	—	BORRDY	85
39CFh - 39C8h	—	Unimplemented								
39C7h	PMD7	_	—	—	—	_	—	DMA2MD	DMA1MD	297
39C6h	PMD6	—	—	SMT1MD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	DSMMD	296
39C5h	PMD5	—	—	U2MD	U1MD	—	SPI1MD	I2C2MD	I2C1MD	295
39C4h	PMD4	CWG3MD	CWG2MD	CWG1MD	—	_	—	—	—	294
39C3h	PMD3	PWM8MD	PWM7MD	PWM6MD	PWM5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	293
39C2h	PMD2	_	DACMD	ADCMD	_		CMP2MD	CMP1MD	ZCDMD	292
39C1h	PMD1	NCO1MD	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	291
39C0h	PMD0	SYSCMD	FVRMD	HLVDMD	CRCMD	SCANMD	NVMMD	CLKRMD	IOCMD	290
39BFh - 39ABh	—				Unimple	emented				
39AAh	PIR10		—	—	—	—	_	CLC4IF	CCP4IF	146
39A9h	PIR9		—	—	—	CLC3IF	CWG3IF	CCP3IF	TMR6IF	145
39A8h	PIR8	TMR5GIF	TMR5IF	—	—	—	—	—	—	145
39A7h	PIR7	—	—	INT2IF	CLC2IF	CWG2IF	—	CCP2IF	TMR4IF	144
39A6h	PIR6	TMR3GIF	TMR3IF	U2IF	U2EIF	U2TXIF	U2RXIF	I2C2EIF	I2C2IF	143
39A5h	PIR5	I2C2TXIF	I2C2RXIF	DMA2AIF	DMA2ORIF	DMA2DCN- TIF	DMA2SCN- TIF	C2IF	INT1IF	142
39A4h	PIR4	CLC1IF	CWG1IF	NCO1IF	_	CCP1IF	TMR2IF	TMR1GIF	TMR1IF	141
39A3h	PIR3	TMR0IF	U1IF	U1EIF	U1TXIF	U1RXIF	I2C1EIF	I2C1IF	I2C1TXIF	140
39A2h	PIR2	I2C1RXIF	SPI1IF	SPI1TXIF	SPI1RXIF	DMA1AIF	DMA10RIF	DMA1DCN- TIF	DMA1SCNTIF	138
39A1h	PIR1	SMT1PWAIF	SMT1PRAIF	SMT1IF	C1IF	ADTIF	ADIF	ZCDIF	INT0IF	138
39A0h	PIR0	IOCIF	CRCIF	SCANIF	NVMIF	CSWIF	OSFIF	HLVDIF	SWIF	137
399Fh - 399Bh	_				Unimple	emented				
399Ah	PIE10	—	—	—	_	_	_	CLC4IE	CCP4IE	156
3999h	PIE9	—	_	—	_	CLC3IE	CWG3IE	CCP3IE	TMR6IE	155
3998h	PIE8	TMR5GIE	TMR5IE	_	_	_		_	—	155
3997h	PIE7	_	—	INT2IE	CLC2IE	CWG2IE		CCP2IE	TMR4IE	154
3996h	PIE6	TMR3GIE	TMR3IE	U2IE	U2EIE	U2TXIE	U2RXIE	I2C2EIE	I2C2IE	153
3995h	PIE5	I2C2TXIE	I2C2RXIE	DMA2AIE	DMA2ORIE	DMA2DCN- TIE	DMA2SCN- TIE	C2IE	INT1IE	152
3994h	PIE4	CLC1IE	CWG1IE	NCO1IE	_	CCP1IE	TMR2IE	TMR1GIE	TMR1IE	151
3993h	PIE3	TMR0IE	U1IE	U1EIE	U1TXIE	U1RXIE	I2C1EIE	I2C1IE	I2C1TXIE	150
3992h	PIE2	I2C1RXIE	SPI1IE	SPI1TXIE	SPI1RXIE	DMA1AIE	DMA10RIE	DMA1DCN- TIE	DMA1SCNTIE	149
3991h	PIE1	SMT1PWAIE	SMT1PRAIE	SMT1IE	C1IE	ADTIE	ADIE	ZCDIE	INT0IE	148
3990h	PIE0	IOCIE	CRCIE	SCANIE	NVMIE	CSWIE	OSFIE	HLVDIE	SWIE	147
398Fh - 398Bh	—				Unimple	emented				
398Ah	IPR10	_	_	_	_	_	_	CLC4IP	CCP4IP	165
Lonondi				منامير م المعاد						

TABLE 42-1:REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

Note 1: Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

3: Unimplemented on PIC18(L)F26/27/45/46/47K42 devices.

4: Unimplemented in PIC18(L)F45/55K42.

TABLE 44-7:	MEMORY PROGRAMMING SPECIFICATIONS
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Standard Operating Conditions (unless otherwise stated)									
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions		
Data EEPROM Memory Specifications									
MEM20	ED	DataEE Byte Endurance	100k	_	_	E/W	-40°C ≤ TA ≤ +85°C		
MEM21	T _{D_RET}	Characteristic Retention		40		Year	Provided no other specifications are violated		
MEM22	$N_{D_{REF}}$	Total Erase/Write Cycles before Refresh	1M 500k	10M —		E/W	-40°C ≤ TA ≤ +60°C -40°C ≤)TA ≤ +85°C		
MEM23	$V_{D_{RW}}$	VDD for Read or Erase/Write operation	VDDMIN	Ι	VDDMAX	٧<			
MEM24	$T_{D_{BEW}}$	Byte Erase and Write Cycle Time		4.0	5.0 <	ms			
Program	n Flash Me	emory Specifications			\langle				
MEM30	E _P	Memory Cell Endurance	10k	Ι	- /	EN	-40°C		
MEM32	T _{P_RET}	Characteristic Retention	_	40 <	1	Year	Provided no other specifications are violated		
MEM33	$V_{P_{RD}}$	VDD for Read operation	VDDMIN		VDBMAX	\checkmark			
MEM34	V _{P_REW}	VDD for Row Erase or Write operation		Á		/ v			
MEM35	T _{P_REW}	Self-Timed Row Erase or Self-Timed Write		80	2.5	ms			

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Memory Cell Endurance for the Program memory is defined as: One Row Erase operation and one Self-Timed Write.

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Leads	N		44		
Lead Pitch	е		0.80 BSC		
Overall Height	Α	-	-	1.20	
Standoff	A1	0.05 - 0.15			
Molded Package Thickness	A2	0.95 1.00 1.			
Overall Width	E	12.00 BSC			
Molded Package Width	E1	10.00 BSC			
Overall Length	D	12.00 BSC			
Molded Package Length	D1	10.00 BSC			
Lead Width	b	0.30 0.37 0.45			
Lead Thickness	С	0.09 - 0.20			
Lead Length	L	0.45 0.60 0.75			
Footprint	L1	1.00 REF			
Foot Angle	θ	0°	3.5°	7°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exact shape of each corner is optional.

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2