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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 43x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f57k42-i-mv

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0/I	48-Pin TQFP	48-Pin UQFN	ADC	Voltage Reference	DAC	Comparators	Zero Cross Detect	l²C	SPI	UART	WSQ	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC2	40	40	ANC2	—	-	—	—	—	-	—	—	T5CKI ⁽¹⁾	CCP1 ⁽¹⁾	—	-	-	—	IOCC2	-
RC3	41	41	ANC3	-	-	—	—	SCL1 ^(3,4)	SCK1 ⁽¹⁾	-	—	T2IN ⁽¹⁾	-	—	_	—	—	IOCC3	-
RC4	46	46	ANC4	—	-	—	—	SDA1 ^(3,4)	SDI1 ⁽¹⁾	—	—	_	—	—	_	—	—	IOCC4	
RC5	47	47	ANC5	—	-	—	—	—	—	—	—	T4IN ⁽¹⁾	—	—	—	—	—	IOCC5	-
RC6	48	48	ANC6	_	-	_	—	_	—	CTS1 ⁽¹⁾	_	_	—	_		—	-	IOCC6	-
RC7	1	1	ANC7	_	-	—	—	_	—	RX1 ⁽¹⁾	_	_	_	_	_	—	—	IOCC7	-
RD0	42	42	AND0	_	-	_	—	(4)	—	_	_	_	_	_		—	-	_	-
RD1	43	43	AND1	_	-	—	—	(4)	—	_	_	-	-	—		—	—	-	-
RD2	44	44	AND2	_	-	-	—	_	—	_	_	-	-	_	_	-	-	-	-
RD3	45	45	AND3	_	-	—	—	_	—	_	_	-	-	—		—	—	-	-
RD4	2	2	AND4	_	-	_	-	_	—	_	_	-	_	-	_	_	_	-	—
RD5	3	3	AND5	_	-	—	—	_	—	_	_	-	-	—		—	—	-	-
RD6	4	4	AND6	_	-	-	—	_	—	_	_	_	—	_		—	-	_	-
RD7	5	5	AND7	_	-	—	—	_	—	_	_	-	-	—		—	—	-	-
RE0	27	27	ANE0	_	-	-	—	_	—	_	_	_	—	_		—	-	_	-
RE1	28	28	ANE1	_	-	—	—	_	—	_	_	_	_	_	_	—	—	-	-
RE2	29	29	ANE2	_	-	_	-	_	—	_	-	-	_	-	_	_	_	-	—
RE3	20	20	—	—	—	—	-	—	—	—	—	-	—	—	-	—	—	IOCE3	MCLR VPP
RF0	36	36	ANF0	_	-	_	—	_	—	_	_	-	_	_	_	_	_	-	—
RF1	37	37	ANF1	—	-	—	—	—	—	—	_	-	—	_	—	—	—	_	—
RF2	38	38	ANF2	—	_	_	—	—	—	—	—	_	—	—	—	—	—	—	—
RF3	39	39	ANF3	—	_	_	—	—	—	—	_	_	—	_	_	—	_	_	_
RF4	12	12	ANF4	_	_	_	-	_	—	_	_	-	_	_	_	_	-	_	-
RF5	13	13	ANF5	-	—	—	—	—	—	-	—	-	—	_	—	—	-	_	-
RF6	14	14	ANF6	_	—	—	_	_	—	_	—	-	—	_	_	—	-	—	-
RF7	15	15	ANF7	-	-	—	_	_	—	-	_	-	—	_	-	—	-	_	-
Note	1:	This is	a PPS remap	pable input si	ignal. The input	t function ma	y be mov	ed from the d	lefault locatio	on shown to a	one of several of	other PORTx pin	S.						

48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42 (CONTINUED)

2: All output signals shown in this row are PPS remappable.

This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers. 3:

These pins can be configured for I²C and SMBTM 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4/RD0/RD1 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds. 4:

TABLE 3:

7.2.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during runtime using clock switching. Refer to Section 7.3 "Clock Switching" for more information.

Two power modes are available for the secondary oscillator. These modes are selected with the SOSCPWR (OSCCON3<6>). Clearing this bit selects the lower Crystal Gain mode which provides lowest microcontroller power consumption. Setting this bit enables a higher Gain mode to support faster crystal start-up or crystals with higher ESR.

FIGURE 7-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Application Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for PIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)
 - TB097, "Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS" (DS91097)
 - AN1288, "Design Practices for Low-Power External Oscillators" (DS01288)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
I2C2TXIE	I2C2RXIE	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	C2IE	INT1IE
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable b	it	U = Unimpleme	ented bit, read as	s 'O'	
u = Bit is und	changed	x = Bit is unkno	own	-n/n = Value at	POR and BOR/	Value at all ot	her Resets
'1' = Bit is se	t	'0' = Bit is clea	red				
bit 7	I2C2TXIE: I ²	² C2 Transmit Int	errupt Enable b	it			
	1 = Enabled	1					
h # 0							
DILO	1 = Enabled	-C2 Receive Inte	errupt Enable b	IL			
	0 = Disable	d					
bit 5	DMA2AIE:	DMA2 Abort Inte	rrupt Enable bit				
	1 = Enabled	1					
	0 = Disable	d					
bit 4	DMA2ORIE:	: DMA2 Overrun	Interrupt Enab	le bit			
	1 = Enablec	1					
h # 0			notion Count In	termunt Enchle hi			
DIL S	1 = Enabled	IE: DIVIAZ DESU	nation Count in	terrupt Enable bi	L		
	0 = Disable	d					
bit 2	DMA2SCNT	IE: DMA2 Sour	ce Count Interru	ıpt Enable bit			
	1 = Enabled	1					
	0 = Disable	d					
bit 1	C2IE: C2 Int	errupt Enable bi	t				
	1 = Enablec	1					
hit 0		u Arnal Intorrupt 1	Enable bit				
	1 = Enablec	ananntenupt i 1					
	0 = Disable	d					

REGISTER 9-19: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
I2C2TXIP	I2C2RXIP	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	C2IP	INT1IP
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable b	it	U = Unimpleme	ented bit, read as	s 'O'	
u = Bit is und	changed	x = Bit is unkno	own	-n/n = Value at	POR and BOR/	/alue at all ot	her Resets
'1' = Bit is se	et	'0' = Bit is clea	red				
bit 7		C2 Transmit Int	errupt Priority b	it			
	1 = High pri	ority					
hit 6		$^{2}C^{2}$ Receive Int	orrupt Priority b	i+			
DILO	1 = High pri	ority		it.			
	0 = Low price	prity					
bit 5	DMA2AIP:	DMA2 Abort Inte	rrupt Priority bit				
	1 = High pri	ority					
	0 = Low price	ority					
bit 4	DMA2ORIP:	DMA2 Overrun	Interrupt Priori	ty bit			
	1 = High pri	ority					
hit 3		I P: DMA2 Desti	nation Count Int	errunt Priority hit			
bit o	1 = High pri	oritv		ionupri nonty bit			
	0 = Low price	ority					
bit 2	DMA2SCNT	IP: DMA2 Source	ce Count Interru	pt Priority bit			
	1 = High pri	ority					
	0 = Low price	ority					
bit 1	C2IP: C2 Int	errupt Priority bi	t				
	\perp = Hign pri 0 = Low pric	ority pritv					
bit 0	INT1IP: Exte	ernal Interrupt 1	Interrupt Priority	v bit			
	1 = High pri	ority		,			
	0 = Low price	prity					

REGISTER 9-30: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

INTCOM GIE/GIEH GIEL IPPEN T INT INT_EOG INTGEOR INTREE UIRX UIRX UIRX IDAAL DMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UMAADORE UIRX IDAAL IDAAL <thidaal< th=""> <thida< th=""><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Register on Page</th></thida<></thidaal<>	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCOMSTAT+™¬¬ <t< td=""><td>INTCON0</td><td>GIE/GIEH</td><td>GIEL</td><td>IPEN</td><td>-</td><td>-</td><td>INT2EDG</td><td>INT1EDG</td><td>INT0EDG</td><td>135</td></t<>	INTCON0	GIE/GIEH	GIEL	IPEN	-	-	INT2EDG	INT1EDG	INT0EDG	135
Piefor Piefor Piefor CirtikeCKCIE 	INTCON1	STAT	<1:0>	-	-	-	-	-	-	136
PietSMT1PPAMESMT1RECTIEADTEDAIDEZOENINTOREINTOR1448PiezTRRNOEUIESPIITXIESPIITXIEDMAIAREDMAIAREDMAIORIEDMAISORTEIACSITXIE150PiezTRRNOEUIEUIEUITXIEUTRNEUZCIEIZCIENEIZCIENEIZCIENEIZCIENEIZCITXIE150PiesTRRNOEUIZCIEDMAZORDMAZORNEDMAZORNEDMAZORNEDMAZORNEIZCIENEIZCIENEIZCIENEIZCIENE155PiesTMRSOETMRSIEUZIEUZIEUZIEUZIECOP3ECOP3ETMRNE155PiesTTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ETMRNE155PiesTTTTTCCOP3ECOP3ETMRNE155PiesTOCIFCRCIFSCANFSMTIFCSWFOSFFHUDFSWF133PiesTOCIFCRCIFSCANFSMTIFOTTADIFZCIFNOTOF138PiesTMRSIFSMTIFSMTIFOTTDMAZORFDMAZORFMMADCHMATOF138PiesTOCIFCRCIFSCANFSMTIFSMTIFOTTDMAZORFDMAZORFIMARE141PiesTMRSIF <t< td=""><td>PIE0</td><td>IOCIE</td><td>CRCIE</td><td>SCANIE</td><td>NVMIE</td><td>CSWIE</td><td>OSFIE</td><td>HLVDIE</td><td>SWIE</td><td>147</td></t<>	PIE0	IOCIE	CRCIE	SCANIE	NVMIE	CSWIE	OSFIE	HLVDIE	SWIE	147
PE2I2C1RXIESPI17IESPI17IESPI17XIEDMA1ACDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEDMA1ORIEMATSONTEM41SONTE149PIE3TURRIEUTIEUTIEUTIRUEUTRUEUTRUEIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIZC1EIST1PIE4CLC1IECORVIEMA2CREDMA2ORTEDMA2CNTEDMA2CREDMA2CREIMA2EIZC1EIZC1EIZC1EIZC1EIST2PIE5TMR3GETMR3EUZIEUZIECUC2IECWG2IETCCITRAE155PIE6TMR3GETMR3EINT2IECIC2IECWG2IETCCC2IEITMR8E155PIE10TTTTTTCCC2IEKM33EKTRAE155PIE10TCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIFE137PIR1SMTIPMAFSWT1FFSCANIFADTFADIFZCDIFITMR1E138PIR2IZC1RXIFSPI1FXSPI17XIFDMA1AFDMA1ORIFDMA1ORIFDMA1ORIFMASCNTF142PIR4CLC1IFOKG1IFNCOIFSCANIFDMA2ORIFDMA2ORIFDMA1ORIFDMA1ORIFITMR1F141PIR4CLC1IFCWG1IFNCOIFMAZORIFDMA2ORIFDMA2ORIFDMA2ORIFITMR1GIF1161PIR4CLC1IFOWG1IF <t< td=""><td>PIE1</td><td>SMT1PWAIE</td><td>SMT1PRAIE</td><td>SMT1IE</td><td>C1IE</td><td>ADTIE</td><td>ADIE</td><td>ZCDIE</td><td>INT0IE</td><td>148</td></t<>	PIE1	SMT1PWAIE	SMT1PRAIE	SMT1IE	C1IE	ADTIE	ADIE	ZCDIE	INT0IE	148
PE3TMR0IEU11EU1EIEU1TXIEU17XIEU12CIEE12C1EIE12C1EIE12C1EIE12C1TXIE150PIE4ICC2TXIEICC2TIF	PIE2	I2C1RXIE	SPI1IE	SPI1TXIE	SPI1RXIE	DMA1AIE	DMA10RIE	DMA1DCNTIE	DMA1SCNTIE	149
PE4CLC1IECWG1IENC01IETCCP1IETMR2IETMR2IETMR1GIETMR1IE151PIE6IZCZTXIEIZCZTXIEIZCZRXIEDMAZANEDMAZORIEDMAZORIEDMAZORIEDMAZORIEDMAZORIEIZCZIEINT1IE152PIE6TMR3GIETMR3IEUZIEUZIEUZIEUZIEUZIEIZCZIETMR4IE155PIE7TTIITIZIECLC2IECWG2IECP3IETMR4IE155PIE8TTTITTCLC3IECWG3IECP3IETMR6IE156PIE70TTTTCLC3IECWG3IECD3IETMR6IE156PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF133PIR11SMT1PRAIFSMT1FAIFSPITIAIFSPITIAIFSPITIAIFDMA1AIFDMA1ORIFDMATOCTIFDMATOCTIF141PIR3IICIFCLC1IFCWG1IFNC01IFITTCCP1IFTMR2IFTMR1GIF141PIR4CLC1IFCWG3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIF142PIR4TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFTMR1GIF141PIR5IZC2TXFIZC2RXFDMA2AFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFDMA2ORIFCI2IFITMR3IF141PIR6TMR3IFTMR3IFUZIFUZIFIFUZIFIFUZIFIFUZIFIFI	PIE3	TMR0IE	U1IE	U1EIE	U1TXIE	U1RXIE	I2C1EIE	I2C1IE	I2C1TXIE	150
PIESI2C2TXIEI2C2RXIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDMA20RIEDVA20EC2IEINTIE152PIEGTMTMITMR3IEUZIEUZIEUZIKIEUZRIEIZC2ELEIZC2ELEIZC2ELEIS3PIE7TTITMR3IEINTIECLC2IECWG2IETCC2PIETMR4IE155PIE3TTTTCLC3IECWG3IECC2IETMR4IE155PIE10TTTTTCLC3IECWG3IECC2IETMR4IE155PIR10NOCIFCRCIFSCANIFNVMIFCSUFOSFFHLVDIFSWITIF137PIR1SMT1PMAIFSMT1FSPITAIFSPITAFADIFADIFZCDIFINTOIF138PIR2I2C1RXIFSPITAFSPITAFSPITAFDMA10FFDMA10CNFDMA10CNTFDMA10CNTF140PIR3TMR0FU1FU1FFUTTIFUTR1FUTR1FTMR1GFIMT1F141PIR5I2C2TXF10/2CXFDMA2AFDMA2AFFDMA2CNTFDMA2SCNTFCC2FFINT1F142PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2TKFI2C1TXF144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT4F144PIR6TMR3GFTMR3FU2FU2FFUTX1FU2RXFI2C2FFIMT6F145PIR7	PIE4	CLC1IE	CWG1IE	NCO1IE	—	CCP1IE	TMR2IE	TMR1GIE	TMR1IE	151
PIEGTMR3GIETMR3IEU2IEU2IEIU2IEIEU2IXIEU2RXIEI2C2IEII12C2IE1533PIE7CC22IETMR4IE1544PIE8TMR5IETMR5IECC22IETMR6IE1555PIE9CLC3IECWG3IECCP3IETMR6IE1556PIE10CLC3IECWG3IECCP3IETMR6IE1556PIR0IOCIFCRCIFSCANIFN/MIFCSWIFOSFIFHIVDIFSWIF1377PIR1SMT1PWAIFSMT1PRAIFSMT1IFC11FAD1FAD1FZCDIFINTOF138PIR2I2C17XIFSP11FXSP11FXIFSP11FXIFDMA1AIFDMA1CRIFDMA1CRIFDMA1CRIFIMACRIFIMACRIF1411PIR3TMR0IFU11FU11EIFU11XIFU1RXIFIZC1FIFIZC1FIFIZC1TXIF1420PIR4CLC1IFCWG1IFNC01IFCCP1IFTMR2IFTMR1GFTMR1IF1442PIR3ITM2FIDM2FDMA2CRIFDMA2CNTIFDMA2SCNTIFIZC2IFIZC1TXIF1420PIR4CLC1IFCWG1IFU2IFU2IFU2IFU2IFU2IFIZC1TXIF1441PIR5ITM2FIDM2FCLC2IFCWG2IFCCP2IFTMR1IF1442PIR6ITM2FITM2FU2IFU2IFU2IFU2IFIZC1FIFIZC1FFIZC	PIE5	I2C2TXIE	I2C2RXIE	DMA2AIE	DMA2ORIE	DMA2DCNTIE	DMA2SCNTIE	C2IE	INT1IE	152
PIE7INT2IECLC2IECWG2IECCP2IETMR4IE154PIE8TMR5IETMR5IE155PIE9155PIE9CLC3IECWG3IECCP3IETMR6IE155PIR0IOCIFCRCIFSCANIFNVMIFCSWIFOSFIFHLVDIFSWIF137PIR1SMT1PWAFSMT1PAFAFSMT1FCHFADTFADFZCDIFINTOIF138PIR2ICC1FCRCIFSCANIFOTHADM1AIFDMA1ORIFDMAIONIFDMAISCNTF139PIR3TMR0IFU11FU11FU11FU11FU11FU11F141141PIR4CLC1FCWG1FNC01F-CCP1IFTMR2IFTMR6IFTMR1F141PIR512C2TXF12C3TXFDMA2AFDMA2ORIFDMA2CNTFDMA2SCNTFC2FINT1F142PIR6TMR3GFTMR3FU2FU2FU2TKFU2RXF12C2EF12C2IF143PIR7T145PIR8TMR3GFTMR3FV2FU2FU2TKFU2RXF12C2FF12C2IF144PIR9TMR3GFTMR3FSMT1PO145PIR10<	PIE6	TMR3GIE	TMR3IE	U2IE	U2EIE	U2TXIE	U2RXIE	I2C2EIE	I2C2IE	153
PIE8TIMRSGIETIMRSIE111 <td>PIE7</td> <td>_</td> <td>-</td> <td>INT2IE</td> <td>CLC2IE</td> <td>CWG2IE</td> <td>-</td> <td>CCP2IE</td> <td>TMR4IE</td> <td>154</td>	PIE7	_	-	INT2IE	CLC2IE	CWG2IE	-	CCP2IE	TMR4IE	154
PIE9 CLC3IE CWG3IE CCP3IE TMR6IE 155 PIE10 CLC3IE CCP3IE TMR6IE 155 PIR0 IOCIF CRCIF SCANIF IC CLC4IE CCP4IE 156 PIR0 SMT1PAUR SMT1PAUR SCANIF CIF ADTIF ADDIF ADDIF ADDIF MA10CNIF DMA1SCNTF 138 PIR2 12C1RXIF SP1IIF SP1ITXIF SP1IXIF DMA1AIF DMA1ORIF DMA1SCNTF 139 PIR3 TMR0IF U11F U1EIF U1XIF U1XIF U2RUF 12C21F 12C21F 12C21F 12C21F 141 PIR3 TMR3GIF TMR3IF CLC3IF CW31F CMA2CNTF DMA2CNTF DMA2CNTF CL2IF 141 PIR4 CLC1F TMR3IF TMR3IF TMR3IF TMR3IF TMR3IF 145 PIR7	PIE8	TMR5GIE	TMR5IE	-	—	-	—	—	_	155
PHE10 — — — — — CLC4HE CCP4HE 156 PIR0 IOCIF CRCH SCAMIF NVMIF CSWIF OSFIF HLVDIF SWITF 137 PIR1 SMT1PWAHF SMT1PRAF SMT1H C1IF ADTIF ADIF ZCDIF INTOIF 138 PIR2 IZC1RXIF SP114F SMT1VF DMA1ALF DMA1ALF DMA1ALF DMA1ALF DMA1ALF DMA1ALF IMATISCHTF 139 PIR3 TMR0IF U1IF U1EF UTXIF DMA2ACTF DMA2ACTF IMATISCHTF 12C1TKIF 12C1TKIF 141 PIR3 TMR3GIF TMR3F DM2ACFF DMA2ACTFF DMA2SCNTF C2EIF INTHF 141 PIR4 CLC1IF CWG1FF TMR3F TMR3FF C1C2IF CWG2FF CCP2IF TMRAFF 144 PIR4 TMR5GIF TMR3FF TMR3FF C1C2IF CWG3FF CCP3IF TMRAFF 145 <td< td=""><td>PIE9</td><td>_</td><td>-</td><td>-</td><td>—</td><td>CLC3IE</td><td>CWG3IE</td><td>CCP3IE</td><td>TMR6IE</td><td>155</td></td<>	PIE9	_	-	-	—	CLC3IE	CWG3IE	CCP3IE	TMR6IE	155
PIRO IOCIF CRCIF SCANIF NVMIF CSWIF OSFIF HLVDIF SWIF 137 PIR1 SMT1PWAIF SMT1PRAIF SMT1IF C1IF ADTF ADIF ZCIR INTOIF 138 PIR2 IZCIRXIF SPI1IF SPI1IF SPI1IF SPI1IF SPI1IF DMAISCITF DMAISCITF DMAISCITF 139 PIR3 TMR0IF UUIF UITXIF DMAISCITF DMAISCITF DMAISCITF 140 PIR4 CLCIFF CWGIFF NCOIFF CCP1F TMR3IFF TMR1F 141 PIR5 12C2TXF 12C2RXF DMA2AIF DMA2ORIF DMA2SCITF DMA2SCITF C2IF INT1F 142 PIR6 TMR3GIF TMR3F U2IF U2EIF U2TXIF U2RXIF 12C2IFF TMR1F 144 PIR6 TMR3GIF TMR3F U2IF C2IF CCP3IF TMR6IF 145 PIR9 - - - - - <td>PIE10</td> <td>_</td> <td>_</td> <td>-</td> <td>—</td> <td>-</td> <td>-</td> <td>CLC4IE</td> <td>CCP4IE</td> <td>156</td>	PIE10	_	_	-	—	-	-	CLC4IE	CCP4IE	156
PIR1 SMT1PWAIF SMT1IPRAIF SMT1IF C1IF ADIF ADIF ZCDIF INTOIF 138 PIR2 I2C1RXIF SP11IF SP11TXIF SP11XIF DMA1AIF DMA1ORIF DMA1DCNTIF DMA1SCNTF 139 PIR3 TMR0IF U1F U1EF U1TXIF URXIF I2C1EF I2C1F I2C1F I2C1F I2C1F IANT1F 141 PIR4 CLC1IF CWG1IF NC0IF — CCP1IF TMR1F IATT1F 142 PIR5 IZC2TXF IZC2RXF DMA2AIF DMA2ORIF DMA2SCNTF U2Z1F IXT1F 142 PIR6 TMR3GIF TMR3IF U2IF UZEIF UZEIF UZEXF UZEXF UZEXF UZEXF IXT1F 144 PIR6 TMR5GIF TMR5IF T — — — — — 145 PIR7 — — — — CLC1F CVEXF TMR4IF 144 <t< td=""><td>PIR0</td><td>IOCIF</td><td>CRCIF</td><td>SCANIF</td><td>NVMIF</td><td>CSWIF</td><td>OSFIF</td><td>HLVDIF</td><td>SWIF</td><td>137</td></t<>	PIR0	IOCIF	CRCIF	SCANIF	NVMIF	CSWIF	OSFIF	HLVDIF	SWIF	137
PIR2 IZC1RXIF SPI1T SPI1TXIF SPI1TXIF DMA1AIF DMA1ORIF DMA1DCNTIF DMA1SCNTIF 139 PIR3 TMR0IF U1IF U1EIF U1TXIF U1RXIF I2C1EIF I2C1IF I2C1TXIF 140 PIR4 CLC1IF CWG1IF NC01F — CCP1F TMR2IF TMR3IF TMR1F 141 PIR6 TMR3GIF TMR3IF U2EF DMA2CIFF DMA2SCNTF C2IF INT1F 142 PIR6 TMR3GIF TMR3IF U2E U2EIF U2RXIF U2RXIF IZC2IF TMR4F 144 PIR7 — — ITTTF CLC2IF CWG3IF CCP3IF TMR4F 144 PIR8 TMR5GIF TMR5IF — — — CCP3IF TMR6F 145 PIR9 — — — — CLC3IF CWG3IF CCP3IF TMR6F 145 PIR10 — CCIP SCANP NVMIP	PIR1	SMT1PWAIF	SMT1PRAIF	SMT1IF	C1IF	ADTIF	ADIF	ZCDIF	INT0IF	138
PIR3 TMR0IF U1IF U1EIF U1TXIF U1RXIF I2C1EIF I2C1IF I2C1TXIF 140 PIR4 CLC1IF CWG1IF NCO1IF — CCP1IF TMR2IF TMR1GIF TMR1IF 141 PIR5 I2C2TXF I2C2RXF DMA2AF DMA2ORIF DMA2SCNTIF C2F INT1GF 142 PIR6 TMR3GIF TMR3IF U2IF U2EIF U2TXIF U2RXIF I2C2EF I2C2IF 143 PIR7 — — ITMR3GIF TMR3IF — — — — — 145 PIR8 TMRSGIF TMRSIF — — — — — 145 PIR9 — — — — — — — 145 PIR10 — — — — CLC3IF CWG3IF CCP3IF TMR6IF 145 PIR10 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMT1PRAIP SMT1PRAIP S	PIR2	I2C1RXIF	SPI1IF	SPI1TXIF	SPI1RXIF	DMA1AIF	DMA10RIF	DMA1DCNTIF	DMA1SCNTIF	139
PIR4 CLC1IF CWG1IF NC01IF T CCP1IF TMR2IF TMR1GIF TMR1IF 141 PIR5 I2C2TXF I2C2RXF DMA2AIF DMA2ORIF DMA2CNTIF DMA2SCNTIF C2IF INT1IF 142 PIR6 TMR3GIF TMR3IF U2IF U2TXIF U2RXIF I2C2EIF I2C2IF 143 PIR7 - - - CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF - - - - - - 145 PIR9 - - - - - - - 145 PIR9 - - - - - - - 145 PIR10 - - - - - CLC3IF CWG3IF CC4IF 146 IPR0 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 <td< td=""><td>PIR3</td><td>TMR0IF</td><td>U1IF</td><td>U1EIF</td><td>U1TXIF</td><td>U1RXIF</td><td>I2C1EIF</td><td>I2C1IF</td><td>I2C1TXIF</td><td>140</td></td<>	PIR3	TMR0IF	U1IF	U1EIF	U1TXIF	U1RXIF	I2C1EIF	I2C1IF	I2C1TXIF	140
PIRSI2C2TXFI2C2RXFDMA2AIFDMA2ORIFDMA2DCNTIFDMA2DCNTIFDMA2SCNTIFC2IFINT1IF142PIR6TMR3GIFTMR3IFU2IFU2EIFU2TXIFU2RXIFI2C2EIFI2C2IF143PIR7———INT2IFCLC2IFCWG2IF—CCP2IFTMR4IF144PIR8TMR5GIFTMR5IF——————145PIR9————————145PIR10————————145PIR10IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PMAPSMT1PANIPSMT1IPC1IPADIPADIPZCDIPINA1SCNTIP158IPR2I2C1RPSPI1IPSPI1IPSPI1RIPDMA1AIPDMA1ORIPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG3IPNCO1IP—CCP1IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2XPDMA2AIPDMA2ORIPDMA2SCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR6TMR3GIPTMR3IPO——————— <td< td=""><td>PIR4</td><td>CLC1IF</td><td>CWG1IF</td><td>NCO1IF</td><td>—</td><td>CCP1IF</td><td>TMR2IF</td><td>TMR1GIF</td><td>TMR1IF</td><td>141</td></td<>	PIR4	CLC1IF	CWG1IF	NCO1IF	—	CCP1IF	TMR2IF	TMR1GIF	TMR1IF	141
PIR6 TMR3GIF TMR3IF U2IF U2EIF U2TXIF U2CXIF I2C2EIF I2C2IF 143 PIR7 — — INT2IF CLC2IF CWG2IF — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — — — 145 PIR9 — — — — — — — — 145 PIR0 — — — — — — — 145 PIR0 — — — — — — CLC3IF CM31F CCP3IF TMR6IF 145 PIR10 — CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMT1PWAIP SMT1P SMT1P MIP IMA10P IMA10CN	PIR5	I2C2TXF	I2C2RXF	DMA2AIF	DMA2ORIF	DMA2DCNTIF	DMA2SCNTIF	C2IF	INT1IF	142
PIR7 — INT2IF CLC2IF CWG2IF — CCP2IF TMR4IF 144 PIR8 TMR5GIF TMR5IF — — — — — — 145 PIR9 — — — — — — — 145 PIR9 — — — — — — — 145 PIR0 — — — — — — — — 145 PIR0 — — — — — — — — 145 PIR10 — — — — — CLC3IF CWG3IF CCP3IF TMR6IF 145 IPR0 IOCIP CRCIP SCANIP NVMIP CSWIP OSFIP HLVDIP SWIP 157 IPR1 SMTPWAIP SMT1PAIP SMT1PAIP SMT1PAIP DMA1AIP DMA1DCNIP DMA1SCNTP DMA1SCNTP IDA1SCNTP	PIR6	TMR3GIF	TMR3IF	U2IF	U2EIF	U2TXIF	U2RXIF	I2C2EIF	I2C2IF	143
PIR8TMR5GIFTMR5IF——————145PIR9————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10—————CLC3IFCWG3IFCCP3IFTMR6IF145PIR10———————CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1IPC1IPADTPADIPZCDIPINT0IP158IPR2I2C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA10CNTIPDMA1SCNTIP159IPR3TMR0IPU11PU1EIPU1TXIPU1RXIPI2C1EIP12C1IP12C1TXIP160IPR4CLC1IPCWG1IPNCO1IP—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7——————————164IPR8TMR5GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIP12C1P164IPR8TMR5GIPTMS1P———————16	PIR7	-	-	INT2IF	CLC2IF	CWG2IF	—	CCP2IF	TMR4IF	144
PIR9CLC3IFCWG3IFCCP3IFTMR6IF145PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSM11PC1IPADTIPADIPZCDIPINT0IP158IPR212C1RIPSP11IPSP11TIPSP11RIPDMA1AIPDMA1ORIPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIP12C1EIP12C1IP12C1TXIP160IPR4CLC1PCWG1IPNC01IP-CCP1IPTMR2IPTMR1GIPTMR1IP161IPR512C2TXP12C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIP12C2EIP12C2IP163IPR7164IPR8TMR5GIPTMR5IP164IPR9165IPR10166NTBASEU166NTBASEU166NTBASEL167NTBASEL-<	PIR8	TMR5GIF	TMR5IF	-	—	-	—	—	—	145
PIR10CLC4IFCCP4IF146IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSP11IPSP11IPSP1RIPDMA1AIPDMA1ORIPDMA1DCNTPDMA1SCNTP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1IPCCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2DCNTIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7164IPR8TMR5GIPTMR3IP164IPR8TMR5GIPTMR5IP165IPR10166IVTBASEU166IVTBASEL167IVTADU167IVTADL167IVTADL167IVTADL<	PIR9	-	-	-	—	CLC3IF	CWG3IF	CCP3IF	TMR6IF	145
IPR0IOCIPCRCIPSCANIPNVMIPCSWIPOSFIPHLVDIPSWIP157IPR1SMT1PWAIPSMT1PRAIPSMT1PC1IPADTIPADIPZCDIPINTOIP158IPR2I2C1RIPSPI1IPSPI1TIPSPI1RIPDMA1AIPDMA1ORPDMA1DCNTIPDMA1SCNTIP159IPR3TMR0IPU1IPU1EIPU1TXIPU1RXIPI2C1EIPI2C1IPI2C1TXIP160IPR4CLC1IPCWG1IPNCO1P—CCP1IPTMR2IPTMR1GIPTMR1IP161IPR5I2C2TXPI2C2RXPDMA2AIPDMA2ORIPDMA2ORIPDMA2SCNTIPC2IPINT1IP162IPR6TMR3GIPTMR3IPU2IPU2EIPU2TXIPU2RXIPI2C2EIPI2C2IP163IPR7IMTSIPCLC2IPCWG2IP-CCP3IPTMR4IP164IPR8TMRSGIPTMRSIP164IPR8TMRSGIPTMRSIP166IPR10166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IPR8TMRSGIPTMRSIP166IFR8TMRSGIP	PIR10	_	-	-	—	-	—	CLC4IF	CCP4IF	146
IPR1 SMT1PWAIP SMT1PRAIP SMT1IP C1IP ADTIP ADIP ZCDIP INTOIP 158 IPR2 I2C1RIP SPI1IP SPI1TIP SPI1RIP DMA1AIP DMA1ORIP DMA1DCNTIP DMA1SCNTIP 159 IPR3 TMR0IP U1IP U1EIP U1TXIP U1RXIP I2C1EIP I2C1IP I2C1TXIP 160 IPR4 CLC1IP CWG1IP NC01IP — CCCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR4 CLC1IP CWG1IP NC01IP — CCCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR5 I2C2TXP I2C2RXP DMA2AIP DMA2ORIP DMA2CNTIP DMA2SCNTIP C2IP INT1IP 162 IPR6 TMR3GIP TMR3IP U2IP U2EIP U2TXIP U2RXIP I2C2EIP I2C2IP 163 IPR6 TMR5GIP TMR3IP — — — CC2G3IP TMR4IP 164 IPR9	IPR0	IOCIP	CRCIP	SCANIP	NVMIP	CSWIP	OSFIP	HLVDIP	SWIP	157
IPR2 I2C1RIP SPI1IP SPI1RIP DMA1AIP DMA1ORIP DMA1DCNTP DMA1SCNTIP 159 IPR3 TMR0IP U1IP U1EIP U1TXIP U1RXIP I2C1EIP I2C1IP I2C1TXIP 160 IPR4 CLC1IP CWG1IP NCO1IP — CCP1IP TMR2IP TMR1GIP TMR1IP 161 IPR4 I2C2TXP I2C2RXP DMA2AIP DMA2ORIP DMA2DCNTIP DM2SCNTIP C2IP INT1IP 162 IPR6 TMR3GIP TMR3IP U2IP U2EIP U2TXIP U2RXIP I2C2EIP I2C2IP 163 IPR7 — — INT2IP CLC2IP CWG2IP — CCP2IP TMR4IP 164 IPR8 TMR5GIP TMR5IP — — — — — 164 IPR9 — — — — CC3IP CWG3IP CCP3IP TMR6IP 165 IPR10 — — — —<	IPR1	SMT1PWAIP	SMT1PRAIP	SMT1IP	C1IP	ADTIP	ADIP	ZCDIP	INT0IP	158
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR2	I2C1RIP	SPI1IP	SPI1TIP	SPI1RIP	DMA1AIP	DMA10RIP	DMA1DCNTIP	DMA1SCNTIP	159
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	IPR3	TMR0IP	U1IP	U1EIP	U1TXIP	U1RXIP	I2C1EIP	I2C1IP	I2C1TXIP	160
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR4	CLC1IP	CWG1IP	NCO1IP	—	CCP1IP	TMR2IP	TMR1GIP	TMR1IP	161
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR5	I2C2TXP	I2C2RXP	DMA2AIP	DMA2ORIP	DMA2DCNTIP	DMA2SCNTIP	C2IP	INT1IP	162
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR6	TMR3GIP	TMR3IP	U2IP	U2EIP	U2TXIP	U2RXIP	I2C2EIP	I2C2IP	163
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	IPR7	-	-	INT2IP	CLC2IP	CWG2IP	—	CCP2IP	TMR4IP	164
IPR9 - - - CLC3IP CWG3IP CCP3IP TMR6IP 165 IPR10 - - - - - CLC3IP CCP3IP TMR6IP 165 IPR10 - - - - - CLC4IP CCP4IP 165 IVTBASEU - - - - BASE<20:16> 166 IVTBASEL - - BASE<15:8> 166 165 IVTBASEL - - BASE<7:0> 166 167 IVTADU Image: Comparison of the c	IPR8	TMR5GIP	TMR5IP	-	—	-	—	—	—	164
IPR10 - - - - CCP4IP 165 IVTBASEU - - - - - 166 IVTBASEH - - - BASE<15:8> 166 IVTBASEL BASE<15:8> 166 IVTBASEL BASE<7:0> 166 IVTADU Image: Comparison of the temperature of temper	IPR9	-	-	-	—	CLC3IP	CWG3IP	CCP3IP	TMR6IP	165
IVTBASEU — — — BASE BASE 166 IVTBASEH BASE<15:8> 166 166 IVTBASEL BASE<7:0> 166 IVTADU Image: Comparison of the system of the sys	IPR10	_	_	_	-	_	-	CLC4IP	CCP4IP	165
IVTBASEH BASE<15:8> 166 IVTBASEL BASE<7:0> 166 IVTADU AD 167 IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTBASEU	_	_	-			BASE<20:16>			166
IVTBASEL BASE<7:0> 166 IVTADU AD AD 167 IVTADH AD AD 167 IVTADL AD AD<7:0> 167	IVTBASEH				BAS	E<15:8>				166
IVTADU AD AD 167 IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTBASEL				BAS	SE<7:0>				166
IVTADH AD<15:8> 167 IVTADL AD<7:0> 167	IVTADU						AD<20:16>			167
IVTADL AD<7:0> 167	IVTADH				AD	<15:8>				167
	IVTADL				AE)<7:0>				167
IVTLOCK — — — — — — — IVTLOCKED 168	IVTLOCK	—	—	—	—	_	—	—	IVTLOCKED	168

TABLE 9-3:	SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for interrupts.

Example 12-3 shows the sequence to do a 16 x 16 unsigned multiplication. Equation 12-1 shows the algorithm that is used. The 32-bit result is stored in four registers (RES<3:0>).

EQUATION 12-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

RES3:RES0	=	ARG1H:ARG1L • ARG2H:ARG2L
	=	$(ARG1H \bullet ARG2H \bullet 2^{16}) +$
		$(ARG1H \bullet ARG2L \bullet 2^8) +$
		$(ARG1L \bullet ARG2H \bullet 2^8) +$
		(ARG1L • ARG2L)

EXAMPLE 12-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

	MOVF	ARG1L, W	; ARG1L * ARG2L->
	MULWF	ARG2L	; PRODH:PRODL
	MOVFF	PRODH, RES1	;
	MOVFF	PRODL, RES0	;
	MOVF	ARG1H, W	; ARG1H * ARG2H->
	MULWF	ARG2H	; PRODH:PRODL
	MOVFF	PRODH, RES3	;
	MOVFF	PRODL, RES2	;
	MOVF MULWF ADDWF ADDWF ADDWFC CLRF ADDWFC	ARG1L, W ARG2H PRODL, W RES1, F PRODH, W RES2, F WREG RES3, F	; ARG1L * ARG2H-> ; PRODH:PRODL ; ; Add cross ; products ; ;
i	MOVF MULWF ADDWF ADDWFC CLRF ADDWFC	ARG1H, W ARG2L PRODL, W RES1, F PRODH, W RES2, F WREG RES3, F	; ; ARG1H * ARG2L-> ; PRODH:PRODL ; ; Add cross ; products ; ;

Example 12-4 shows the sequence to do a 16 x 16 signed multiply. Equation 12-2 shows the algorithm used. The 32-bit result is stored in four registers (RES<3:0>). To account for the sign bits of the arguments, the MSb for each argument pair is tested and the appropriate subtractions are done.

EQUATION 12-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

RES3:RES0 = ARG1H:ARG1L • ARG2H:ARG2L
$= (ARG1H \bullet ARG2H \bullet 2^{16}) +$
$(ARG1H \bullet ARG2L \bullet 2^8) +$
$(ARG1L \bullet ARG2H \bullet 2^8) +$
$(ARG1L \bullet ARG2L) +$
$(-1 \bullet ARG2H < 7 > \bullet ARG1H: ARG1L \bullet 2^{16}) +$
$(-1 \bullet ARG1H < 7 > \bullet ARG2H:ARG2L \bullet 2^{16})$

EXAMPLE 12-4: 16 x 16 SIGNED MULTIPLY ROUTINE

MOVF	ARG1L, W	
MULWF	ARG2L	; ARG1L * ARG2L ->
		; PRODH:PRODL
MOVFF	PRODH, RES1	;
MOVFF	PRODL, RESO	;
;	ADC1U N	
MULTIME	ARGIH, W	· ADC111 + ADC211 >
MOLWE	AKGZN	, ARGIN " ARGZN ->
MOVEE	PRODH. RES3	; 110011.110001
MOVEE	PRODI, RES2	;
;	. , .	
MOVF	ARG1L, W	
MULWF	ARG2H	; ARG1L * ARG2H ->
		; PRODH:PRODL
MOVF	PRODL, W	;
ADDWF	RES1, F	; Add cross
MOVF	PRODH, W	; products
ADDWFC	RESZ, F	;
CLRF	WREG DEC2 E	;
ADDWFC .	RESS, F	,
MOVE	ARG1H W	
MULWE	ARG21	: ARG1H * ARG21 ->
		; PRODH:PRODL
MOVF	PRODL, W	;
ADDWF	RES1, F	; Add cross
MOVF	PRODH, W	; products
ADDWFC	RES2, F	;
CLRF	WREG	;
ADDWFC	RES3, F	;
;	ADC211 7	· ADCOULADCOL DOCO
BRA	SIGN ARG1	, ARGZAIARGZI HEG? • no check ARG1
MOVE	ARGIL. W	; no, check Akdi
SUBWF	RES2	;
MOVF	ARG1H, W	;
SUBWFB	RES3	
;		
SIGN_ARG1		
BTFSS	ARG1H, 7	; ARG1H:ARG1L neg?
BRA	CONT_CODE	; no, done
MOVE	AKGZL, W	;
SUBWE	RESZ ARC24 W	;
SUBWEB	RESS	,
:	1100	
, CONT CODE		
:		

13.0 NONVOLATILE MEMORY (NVM) CONTROL

Nonvolatile Memory (NVM) is separated into two types: Program Flash Memory (PFM) and Data EEPROM Memory.

PFM, Data EEPROM, User IDs and Configuration bits can all be accessed using the REG<1:0> bits of the NVMCON1 register.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

NVM can be protected in two ways, by either code protection or write protection. Code protection (CP and CPD bits in Configuration Word 5L) disables access, reading and writing to both PFM and Data EEPROM Memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all nonvolatile memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the PFM, as defined by the WRT bits of Configuration Word 4H. Write protection does not affect a device programmer's ability to read, write or erase the device.

	PC<20:0>	PC<20:0> Execution		User Access			
Memory	ICSP™ Addr<21:0> TBLPTR<21:0> NVMADDR<9:0>	CPU Execution	REG	TABLAT	NVMDAT		
Program Flash Memory (PFM)	00 0000h ••• 01 FFFFh	Read	10	Read/ Write ⁽¹⁾	(3)		
User IDs ⁽²⁾	20 0000h ••• 20 000Fh	No Access	x1	Read/ Write	(3)		
Reserved	20 0010h 2F FFFFh	No Access		(3)			
Configuration	30 0000h ••• 30 0009h	No Access	x1	Read/ Write ⁽¹⁾	(3)		
Reserved	30 000Ah 30 FFFFh	No Access		(3)			
User Data Memory (Data EEPROM)	31 0000h ••• 31 03FFh	No Access	00	(3)	Read/ Write ⁽¹⁾		
Reserved	31 0400h 3E FFFFh	No Access		(3)			
Device Information Area (DIA)	3F 0000h ••• 3F 003Fh	No Access	x1	Read	(3)		
Reserved	3F 0040h 3F FF09h	No Access		(3)			
Device Configuration Information (DCI)	3F FF00h ••• 3F FF09h	No Access	xl	Read	(3)		
Reserved	3F FF0Ah 3F FFFBh	No Access		(3)			
Revision ID/ Device ID	3F FFFCh ••• 3F FFFFh	No Access	xl	Read	(3)		

TABLE 13-1: NVM ORGANIZATION AND ACCESS INFORMATION

Note 1: Subject to Memory Write Protection settings.

2: User IDs are eight words ONLY. There is no code protection, table read protection or write protection implemented for this region.

3: Reads as '0', writes clear the WR bit and WRERR bit is set.

FIGURE 21-7:	TIMER1/3/5 GATE SING	BLE-PULSE AND TOGGLE COM	BINED MODE
TMRxGE			
TxGPOL			
TxGSPM			
TxGTM			
TxGG <u>O/</u>	Set by software	•	Cleared by hardware on falling edge of TxGVAL
DONE	Counting enabled o	n	
TxG_IN	rising edge of TXG		
ТхСКІ			
TxGV <u>AL</u>			
TIMER1/3/5	Ν	N + 1 N + 2 N + 3 N + 4	
TMRxGIF	 Cleared by software 	Set by hardware on falling edge of TxGVAL ──►	Cleared by software

21.11 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer1 (TMR1MD), Timer3 (TMR3MD) and Timer5 (TMR5MD) are in the respective PMD registers. See **Section 19.0 "Peripheral Module Disable (PMD)"** for more information.

23.5 Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown below. Refer to **Section 1.3.2.2 "Long Bit Names**" for more information.

Peripheral	Bit Name Prefix
CCP1	CCP1
CCP2	CCP2
CCP3	CCP3
CCP4	CCP4

REGISTER 23-1: CCPxCON: CCPx CONTROL REGISTER

R/W-0/0	U-0	R-x	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	FMT		MODE	<3:0>	
bit 7							bit 0

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			
bit 7 EN: CC	P Module Enable bit					
1 = CC	CP is enabled					
0 = C	CP is disabled					

- bit 6 Unimplemented: Read as '0'
- bit 5 OUT: CCPx Output Data bit (read-only)
- bit 4 FMT: CCPW (pulse-width) Alignment bit <u>MODE = Capture mode:</u> Unused <u>MODE = Compare mode:</u> Unused
 - MODE = PWM mode:
 - 1 = Left-aligned format
 - 0 = Right-aligned format
- bit 3-0 MODE<3:0>: CCPx Mode Select bits

MODE	Operating Mode	Operation	Set CCPxIF
11xx	PWM	PWM operation	Yes
1011		Pulse output; clear TMR1 ⁽²⁾	Yes
1010	Compara	Pulse output	Yes
1001	Compare	Clear output ⁽¹⁾	Yes
1000		Set output ⁽¹⁾	Yes
0111		Every 16th rising edge of CCPx input	Yes
0110		Every 4th rising edge of CCPx input	Yes
0101	Capture	Every rising edge of CCPx input	Yes
0100		Every falling edge of CCPx input	Yes
0011		Every edge of CCPx input	Yes
0010	Compare	Toggle output	Yes
0001	Compare	Toggle output; clear TMR1 ⁽²⁾	Yes
0000	Disabled		_

Note 1: The set and clear operations of the Compare mode are reset by setting MODE = 4'b0000 or EN = 0.

2: When MODE = 0001 or 1011, then the timer associated with the CCP module is cleared. TMR1 is the default selection for the CCP module, so it is used for indication purpose only.

25.6 Modes of Operation

The modes of operation are summarized in Table 25-1. The following sections provide detailed descriptions, examples of how the modes can be used. Note that all waveforms assume WPOL/SPOL/CPOL = 0. When WPOL/SPOL/CPOL = 1, all SMTSIGx, SMTWINx and SMT clock signals will have a polarity opposite to that indicated. For all modes, the REPEAT bit controls whether the acquisition is repeated or single. When REPEAT = 0 (Single Acquisition mode), the timer will stop incrementing and the GO bit will be reset upon the completion of an acquisition. Otherwise, the timer will continue and allow for continued acquisitions to overwrite the previous ones until the timer is stopped in software.

25.6.1 TIMER MODE

Timer mode is the simplest mode of operation where the SMT1TMR is used as a 16/24-bit timer. No data acquisition takes place in this mode. The timer increments as long as the GO bit has been set by software. No SMT window or SMT signal events affect the GO bit. Everything is synchronized to the SMT clock source. When the timer experiences a period match (SMT1TMR = SMT1PR), SMT1TMR is reset and the period match interrupt trips. See Figure 25-3.

MODE	Mode of Operation	Synchronous Operation	Reference
0000	Timer	Yes	Section 25.6.1 "Timer Mode"
0001	Gated Timer	Yes	Section 25.6.2 "Gated Timer Mode"
0010	Period and Duty Cycle Acquisition	Yes	Section 25.6.3 "Period and Duty Cycle Mode"
0011	High and Low Time Measurement	Yes	Section 25.6.4 "High and Low Measure Mode"
0100	Windowed Measurement	Yes	Section 25.6.5 "Windowed Measure Mode"
0101	Gated Windowed Measurement	Yes	Section 25.6.6 "Gated Windowed Measure Mode"
0110	Time of Flight	Yes	Section 25.6.7 "Time of Flight Measure Mode"
0111	Capture	Yes	Section 25.6.8 "Capture Mode"
1000	Counter	No	Section 25.6.9 "Counter Mode"
1001	Gated Counter	No	Section 25.6.10 "Gated Counter Mode"
1010	Windowed Counter	No	Section 25.6.11 "Windowed Counter Mode"
1011-1111	Reserved	—	—

TABLE 25-1: MODES OF OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
SMT1CON0	EN	—	STP	WPOL	SPOL	CPOL	SMT1PS	S<1:0>	394
SMT1CON1	GO	REPEAT	_	_		MODE	<3:0>		395
SMT1STAT	CPRUP	CPWUP	RST	_	—	TS	WS	AS	396
SMT1CLK	—	—	—	—	—	(CSEL<2:0>		397
SMT1SIG	_	SSEL<4:0>							399
SMT1WIN	— — — WSEL<4:0>							398	
SMT1TMRL		TMR<7:0>							
SMT1TMRH	TMR<15:8>								400
SMT1TMRU				TMR<2	23:16>				400
SMT1CPRL				CPR<	:7:0>				401
SMT1CPRH				CPR<	15:8>				401
SMT1CPRU				CPR<2	3:16>				401
SMT1CPWL				CPW<	<7:0>				402
SMT1CPWH				CPW<	15:8>				402
SMT1CPWU	CPW<23:16>							402	
SMT1PRL	PR<7:0>							403	
SMT1PRH	PR<15:8>							403	
SMT1PRU		PR<23:16>							403

TABLE 25-3: SUMMARY OF REGISTERS ASSOCIATED WITH SMT1

Legend: -= unimplemented read as '0'. Shaded cells are not used for SMT1 module.



32.5.6 MASTER MODE SPI CLOCK CONFIGURATION

32.5.6.1 SPI Clock Selection

The clock source for SPI master modes is selected by the SPIxCLK register. Selections include the following:

- Fosc
- HFINTOSC
- CLKREF
- Timer0_overflow
- Timer2_Postscaled
- Timer4_Postscaled
- Timer6_Postscaled
- SMT_match

The SPIxBAUD register allows for dividing this clock. The frequency of the SCK output is defined by Equation 32-1:

EQUATION 32-1: FREQUENCY OF SCK OUTPUT SIGNAL

 $F_{BAUD} = \frac{F_{CSEL}}{(2 \cdot (BAUD + 1))}$

where FBAUD is the baud rate frequency output on the SCK pin, FCSEL is the frequency of the input clock selected by the SPIxCLK register, and BAUD is the value contained in the SPIxBAUD register.

32.5.6.2 CKE, CKP and SMP

The CKP, CKE, and SMP bits control the relationship between the SCK clock output, SDO output data changes, and SDI input data sampling. The bit functions are as follows:

- CKP SCK output polarity
- CKE SDO output change relative to the SCK clock
- SMP SDI input sampling relative to the clock edges

The CKE bit, when set, inverts the low Idle state of the SCK output to a high Idle state.

Figure 32-7 through Figure 32-10 illustrate the eight possible combinations of the CKP, CKE, and SMP bit selections.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. When the CKE bit is cleared, the SDO data is undefined prior to the first SCK edge.

Note: All timing diagrams assume the LSBF bit of SPIxCON0 is cleared.

32.6.3 SLAVE MODE SLAVE SELECT

In Slave mode, an external Slave Select Signal can be used to synchronize communication with the Master device. The Slave Select line is held in its inactive state (high by default) until the master device is ready to communicate. When the Slave Select transitions to its active state, the slave knows that a new transmission is starting.

When the Slave Select goes false at the end of the transmission the receive function of the selected SPI Slave device returns to the inactive state. The slave is then ready to receive a new transmission when the Slave Select goes True again.

The Slave Select signal is received on the \overline{SS} input pin. This pin is remappable with the SPIxSSPPS register (see Section 17.1 "PPS Inputs"). When the input on this pin is true, transmission and reception are enabled, and the SDO pin is driven. When the input on this pin is false, the SDO pin is either tri-stated (if the TRIS bit associated with the SDO pin is set) or driven to the value of the LAT bit associated with the SDO pin (if the TRIS bit associated with the SDO pin is cleared). In addition, the SCK input is ignored.

If the SS input goes False, while a data transfer is still in progress, it is considered a slave select fault. The SSFLT bit of SPIxCON2 indicates whether such an event has occurred. The transfer counter value determines the number of bits in a valid data transfer (see Section 32.4 "Transfer Counter" for more details).

The Slave Select polarity is controlled by the SSP bit of SPIxCON1. When SSP is set (its default state), the Slave Select input is active-low, and when it is cleared, the Slave Select input is active-high.

The Slave Select for the SPI module is controlled by the SSET bit of SPIxCON2. When the bit is cleared (its default state), the slave select will act as described above. When the bit is set, the SPI module will behave as if the SS input was always in its active state.

Note: When SSET is set, the effective SS(in) signal is always active. Hence, the SSFLT bit may be disregarded.

32.6.4 SLAVE MODE CLOCK CONFIGURATION

In Slave Mode, SCK is an input, and must be configured to the same polarity and clock edge as the master device. As in Master mode, the polarity of the clock input is controlled by the CKP bit of SPIxCON1 and the clock edge used for transmitting data is controlled by the CKE bit of SPIxCON1.

32.6.5 DAISY-CHAIN CONFIGURATION

The SPI bus can be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device connected to all slave devices (alternately, the slave devices can be configured to ignore the slave select line by setting the SSET bit). In a typical Daisy-Chain configuration, the SCK signal from the master is connected to each of the slave device SCK inputs. However, the SCK input and output are separate signals selected by the PPS control. When the PPS selection is made to configure the SCK input and SCK output on separate pins then, the SCK output will follow the SCK input, allowing for SCK signals to be daisy-chained like the SDO/SDI signals.

Figure 32-12 shows the block diagram of a typical daisy-chain connection, and Figure 32-13 shows the block diagram of a daisy-chain connection possible using this SPI module.

asserting the Start condition. The action of the SDA being driven low while SCL is high is the Start condition,

causing the SCIF bit to be set. One TSCL later the SCL

is asserted low, ending the start sequence. Figure 33-

15 shows the Start condition timing.

33.5.5 I²C MASTER MODE START CONDITION TIMING

The user can initiate a Start condition by either writing to the Start bit (S) of the I2CxCON0 register or by writing to the I2CxTXB register based on the ABD bit setting. Master hardware waits for BFRE = 1, before

FIGURE 33-15: START CONDITION TIMING



33.5.6 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the Start bit of the I2CxCON0 register is set and the master module is waiting from a Restart clock stretch event (RSEN = 1 and I2CxCNT = 0).

When the Start bit is set, the SDA pin is released high for TscL/2. Then the SCL pin is released floated high) for TscL/2. If the SDA pin is detected low, bus collision flag (BCLIF) is set and the master goes idle. If SDA is detected high, the SDA pin will be pulled low (Start condition) for TscL. Last, SCL is asserted low and I2CxADB0/1 is loaded into the shift register. As soon as a Restart condition is detected on the SDA and SCL pins, the RSCIF bit is set. Figure 33-16 shows the timings for repeated Start Condition.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
3D6Ch	I2C1CNT		CNT							586
3D6Bh	I2C1TXB				Tک	(B				
3D6Ah	I2C1RXB		RXB							
3D69h - 3D67h	—				Unimple	emented				
3D66h	I2C2BTO		BTO						582	
3D65h	I2C2CLK		CLK						581	
3D64h	I2C2PIE	CNTIE	ACKTIE	—	WRIE	ADRIE	PCIE	RSCIE	SCIE	588
3D63h	I2C2PIR	CNTIF	ACKTIF	—	WRIF	ADRIF	PCIF	RSCIF	SCIF	587
3D62h	I2C2STAT1	TXWE	_	—	—	RXRE	CLRBF	—	RXBF	584
3D61h	I2C2STAT0	BFRE	_	MMA	—	D	—	—	—	583
3D60h	I2C2ERR	—	BTOIF	BCLIF	NACKIF	—	BTOIE	BCLIE	NACKIE	585
3D5Fh	I2C2CON2	ACNT	GCEN	FME	ABD	SD	AHT	BI	FRET	580
3D5Eh	I2C2CON1	ACKCNT	ACKDT	ACKSTAT	ACKT	—	RXO	TXU	CSD	579
3D5Dh	I2C2CON0	EN	RSEN	S	CSTR	MDR		MODE		577
3D5Ch	I2C2ADR3				ADR				—	592
3D5Bh	I2C2ADR2				AD)R				591
3D5Ah	I2C2ADR1				ADR				—	590
3D59h	I2C2ADR0		ADR							589
3D58h	I2C2ADB1		ADB							594
3D57h	I2C2ADB0				AD)В				593
3D56h	I2C2CNT				CN	NT				586
3D55h	I2C2TXB				Tک	(B				
3D54h	I2C2RXB				R۷	КB				
3D53h - 3D1Dh	_				Unimple	emented				
3D1Ch	SPI1CLK				CLK	SEL				542
3D1Bh	SPI1INTE	SRMTIE	TCZIE	SOSIE	EOSIE		RXOIE	TXUIE	—	536
3D1Ah	SPI1INTF	SRMTIF	TCZIF	SOSIF	EOSIF		RXOIF	TXUIF	—	535
3D19h	SPI1BAUD				BA	UD				538
3D18h	SPI1TWIDTH	—		—	—			TWIDTH		537
3D17h	SPI1STATUS	TXWE		TXBE	—	RXRE	CLRBF	_	RXBF	541
3D16h	SPI1CON2	BUSY	SSFLT	—	—	_	SSET	TXR	RXR	540
3D15h	SPI1CON1	SMP	CKE	CKP	FST		SSP	SDIP	SDOP	539
3D14h	SPI1CON0	EN		—	—		LSBF	MST	BMODE	538
3D13h	SPI1TCNTH	TCNTH						537		
3D12h	SPI1TCNTL				TCN	NTL				536
3D11h	SPI1TXB	ТХВ						542		
3D10h	SPI1RXB	RXB						541		
3D0Fh - 3CFFh	_	Unimplemented								
3CFEh	MD1CARH	—	_	—			CH			471
3CFDh	MD1CARL	—	_	—			CL			471
3CFCh	MD1SRC	_		_			MS			472
3CFBh	MD1CON1	_		CHPOL	CHSYNC	_		CLPOL	CLSYNC	470
3CFAh	MD1CON0	EN	_	OUT	OPOL	_	_	_	BIT	469
3CF9h - 3CE7h	_				Unimple	mented				

TABLE 42-1: REGISTER FILE SUMMARY FOR PIC18(L)F26/27/45/46/47/55/56/57K42 DEVICES

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

Note 1: Unimplemented in LF devices.

2: Unimplemented in PIC18(L)F26/27K42.

3: Unimplemented on PIC18(L)F26/27/45/46/47K42 devices.

4: Unimplemented in PIC18(L)F45/55K42.





Standa	Standard Operating Conditions (unless otherwise stated)								
Param No.	Sym.	Characteristic	Min.	Typt	Max.	Units	Conditions		
IO1*	T _{CLKOUTH}	CLKOUT rising edge delay (rising edge Fosc (Q1 cycle) to falling edge CLKOUT	/	-	70	ns			
IO2*	T _{CLKOUTL}	CLKOUT falling edge delay (rising edge Fosc (Q3 cycle) to rising edge CLKQUT			72	ns			
IO3*	T _{IO_VALID}	Port output valid time (rising edge Fosc (Q1 cycle) to port valid)		50	70	ns			
IO4*	T _{IO_SETUP}	Port input setup time (Setup time before rising edge Fosc – Q2 cxcle)	20			ns			
IO5*	T _{IO_HOLD}	Port input hold time (Hold time after rising edge Fosc – Q2 cycle)	50	_	—	ns			
IO6*	T _{IOR_SLREN}	Port I/O rise time, slew rate enabled	—	25	_	ns	VDD = 3.0V		
107*	T_{IOR_SLRDIS}	Port I/O rise time, slew rate disabled	—	5	_	ns	VDD = 3.0V		
IO8*	T _{IOF_SLREN}	Port I/O fall time, slew rate enabled	—	25	_	ns	VDD = 3.0V		
IO9*	TIOF_SLRDIS	Port //O fall time, slew rate disabled	—	5		ns	VDD = 3.0V		
IO10*	T _{INT}	INT pin high or low time to trigger an interrupt	25	—		ns			
IO11*	TIOC	Interrupt-on-Change minimum high or low time to trigger interrupt	25	—		ns			

*These parameters are characterized but not tested.



Package Marking Information (Continued)

Legen	d: XXX Y YY WW NNN @3 *	Customer-specific information or Microchip part number Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC [®] designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package.
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